Triple 1800 mA Buck Regulators With Precision Enables and Power Good Outputs

Preliminary Data Sheet

ADP5135

FEATURES

Main input voltage range: 3.0 V to 5.5 V
Three 1800 mA buck regulators
24-lead, 4 mm × 4 mm LFCSP package
Regulator accuracy: ±1.8%
Factory programmable or external adjustable VOUTx
Precision Enables for easier power sequencing
Power Good Pins for monitoring of each regulator
3 MHz buck operation with forced PWM and auto PWM/PSM modes
BUCK1/BUCK2/BUCK3: output voltage range from 0.8 V to 3.8 V

APPLICATIONS

Power for processors, ASICS, FPGAs, and RF chipsets
Portable instrumentation and medical devices
Space constrained devices

GENERAL DESCRIPTION

The ADP5135 combines three high performance buck regulators. It is available in a 24-lead 4 mm × 4 mm LFCSP.

The high switching frequency of the buck regulators enables tiny multilayer external components and minimizes the board space. When the MODE pin is set to high, the buck regulators operate in forced PWM mode. When the MODE pin is set to low, the buck regulators operate in PWM mode only when the load is above a predefined threshold. When the load current falls below this predefined threshold, the regulator operates in power save mode (PSM), improving the light load efficiency.

Table 1. Family Models

Model	Channels	Max Current	Package
ADP5023	2 Bucks,1 LDO	800mA, 300mA	LFCSP (CP-24-10)
ADP5024	2 Bucks,1 LDO	1.2A, 300mA	LFCSP (CP-24-10)
ADP5034	2 Bucks,2 LDOs	1.2A, 300mA	LFCSP (CP-24-10), TSSOP (RE-28-1)
ADP5037	2 Bucks,2 LDOs	800mA, 300mA	LFCSP (CP-24-10)
ADP5033	2 Bucks,2 LDOs with 2 EN pins	800mA, 300mA	WLCSP (CB-16-8)
ADP5040	1 Buck, 2 LDOs	1.2A, 300mA	LFCSP (CP-20-10)
ADP5041	1 Buck, 2 LDOs w/ Supevisory, Watchdog, Manual Reset	1.2A, 300mA	LFCSP (CP-20-10)
ADP5133	2 Bucks with 2 EN pins	800mA	WLFCSP (CB-16-8)
ADP5134	2 Bucks,2 LDOs w/ PE and PG	1.2A, 300mA	LFCSP (CP-24-10)

Buck1 and Buck2 operate in sync and Buck3 operates out of phase to reduce the input capacitor requirement.

Regulators in the ADP5135 are activated through dedicated enable pins. The default output voltages can be externally set in the adjustable version, or factory programmable to a wide range of preset values in the fixed voltage version.

TYPICAL APPLICATION CIRCUIT

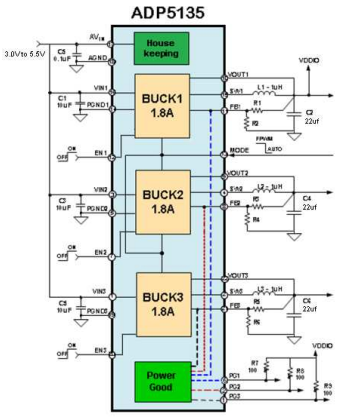

Figure 1.

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SPECIFICATIONS

GENERAL SPECIFICATIONS

$V_{AVIN} = V_{IN1} = V_{IN2} = V_{IN3}$ = 3.0 V to 5.5 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{AVIN}, V_{IN1}, V_{IN2}, V_{IN3}		3.0		5.5	V
THERMAL SHUTDOWN						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			20		°C
START-UP TIME[1]						
BUCK1	t_{START1}			650		µs
BUCK2	t_{START2}			750		µs
BUCK3	t_{START3}			750		µs
START-UP TIME, BUCK3 first						
BUCK3	t_{START4}			750		µs
BUCK1	t_{START5}			300		µs
BUCK2	t_{START6}			400		µs
SHUTDOWN CONTROL		All ENx pins below V_{IL_EN} level to achive $I_{SHUTDOWN}$				
Level High	V_{IH_EN}		0.9			V
Level Low	V_{IL_EN}	T_J = −40°C to +85°C			0.35	V
PRECISION ENABLE PINS		Regulator(s) activation/deactivation thresholds				V
Analog Activation Threshold	V_{ENR}	Device out of shutdown (VENx > V_{IH_EN})	0.94	0.97	1	
Hysteresis (Regulator Deactivation)	V_{ENH}			80		mV
Input Leakage Current	$V_{I-LEAKAGE}$			0.05	1	uA
POWER GOOD PINS		Monitors Vout falling out of regulation				
Power Good Falling Threshold	V_{PGLOW}			85		%Vout
Power Good Rising Threshold	V_{PGHYS}		91	94	97	%Vout
Power Good Delay	t_{PGDLY}			20		us
Power Good Leakage Current	I_{PGIQ}	$V_{PG} = V_{IN}$			1	uA
Power Good Output Voltage Low	V_{PGOL}	Load current = 1mA		0.1	0.2	V
MODE PIN						
Level High	V_{IH_MOD}		1.1			V
Level Low	V_{IL_MOD}				0.4	V
INPUT CURRENT		No load, no buck switching				
All Channels Enabled	$I_{STBY-NOSW}$			85	108	µA
All Channels Disabled	$I_{SHUTDOWN}$	T_J = −40°C to +85°C		0.3	1	µA
VIN1 UNDERVOLTAGE LOCKOUT						
Mid UVLO Input Voltage Rising	$UVLO_{VIN1RISE}$				2.95	V
Mid UVLO Input Voltage Falling	$UVLO_{VIN1FALL}$		2.5			V

[1] Start-up time is defined as the time from EN1 = EN2 = EN3 from 0 V to V_{AVIN} to VOUT1, VOUT2, and VOUT3 reaching 90% of their nominal level. Start-up times are shorter for individual channels if another channel is already enabled. See the Typical Performance Characteristics section for more information.

BUCK1, BUCK2 AND BUCK3 SPECIFICATIONS

$V_{AVIN} = V_{IN1} = V_{IN2} = V_{IN3} = 3.0$ V to 5.5 V; $T_J = -40°C$ to $+125°C$ for minimum/maximum specifications, and $T_A = 25°C$ for typical specifications, unless otherwise noted.[1]

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	$\Delta V_{OUT1}/V_{OUT1}$, $\Delta V_{OUT2}/V_{OUT2}$, $\Delta V_{OUT3}/V_{OUT3}$	PWM mode; $I_{LOAD1} = I_{LOAD2} = I_{LOAD3} = 0$ mA	−1.8		+1.8	%
Line Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta V_{IN1}$, $(\Delta V_{OUT2}/V_{OUT2})/\Delta V_{IN2}$, $(\Delta V_{OUT3}/V_{OUT3})/\Delta V_{IN3}$	PWM mode		−0.05		%/V
Load Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta I_{OUT1}$, $(\Delta V_{OUT2}/V_{OUT2})/\Delta I_{OUT2}$, $(\Delta V_{OUT3}/V_{OUT3})/\Delta I_{OUT3}$	I_{LOAD} = 0 mA to 1800 mA, PWM mode		-0.1		%/A
VOLTAGE FEEDBACK	V_{FB1}, V_{FB2}	Models with adjustable outputs	0.491	0.5	0.509	V
OPERATING SUPPLY CURRENT		MODE = ground				
BUCK1 Only	I_{IN1}	I_{LOAD1} = 0 mA, device not switching, all other channels disabled		42		µA
BUCK2 Only	I_{IN2}	I_{LOAD2} = 0 mA, device not switching, all other channels disabled		52		µA
BUCK3 Only	I_{IN3}	I_{LOAD3} = 0 mA, device not switching, all other channels disabled		52		
BUCK1, BUCK2 and BUCK3	I_{IN}	$I_{LOAD1} = I_{LOAD2} = I_{LOAD3} = 0$ mA, device not switching		85		µA
PSM CURRENT THRESHOLD	I_{PSM}	PSM to PWM operation		100		mA
SW CHARACTERISTICS						
SW On Resistance	R_{NFET}	$V_{IN1} = V_{IN2} = V_{IN3} = 3.6$ V; LFCSP package		140	225	mΩ
	R_{PFET}	$V_{IN1} = V_{IN2} = V_{IN3} = 3.6$ V; LFCSP package		190	295	mΩ
	R_{NFET}	$V_{IN1} = V_{IN2} = V_{IN3} = 5.5$ V; LFCSP package		122	189	mΩ
	R_{PFET}	$V_{IN1} = V_{IN2} = V_{IN3} = 5.5$ V; LFCSP package		147	228	mΩ
Current Limit	I_{LIMIT1}, I_{LIMIT2}, I_{LIMIT3}	pFET switch peak current limit	2250	2600	2950	mA
ACTIVE PULL-DOWN	R_{PDWN-B}	VIN1 = VIN2 = VIN3 = 3.6 V; Channel disabled		75		Ω
OSCILLATOR FREQUENCY	f_{SW}		2.5	3.0	3.5	MHz

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

$T_A = -40°C$ to $+125°C$, unless otherwise specified.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
NOMINAL INPUT AND OUTPUT CAPACITOR RATINGS					
BUCK1, BUCK2 and BUCK3 Input Capacitor Ratings	C_{MIN1}, C_{MIN2}, C_{MIN3}	4.7		40	µF
BUCK1, BUCK2 and BUCK3 Output Capacitor Ratings	C_{MIN4}, C_{MIN5}, C_{MIN6}	10		40	µF
CAPACITOR ESR	R_{ESR}	0.001		1	Ω

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVIN to AGND	−0.3 V to +6 V
VIN1, VIN2, VIN3 to AVIN	−0.3 V to +0.3 V
PGND1, PGND2, PGND3 to AGND	−0.3 V to +0.3 V
VOUT1, VOUT2, VOUT3, FB1, FB2, FB3, EN1, EN2, EN3, MODE, PG1, PG2, PG3 to AGND	−0.3 V to (AVIN + 0.3 V)
SW1 to PGND1	−0.3 V to (VIN1 + 0.3 V)
SW2 to PGND2	−0.3 V to (VIN2 + 0.3 V)
SW3 to PGND3	−0.3 V to (VIN3 + 0.3 V)
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For detailed information on power dissipation, see the Power Dissipation and Thermal Consideration section.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead, 0.5 mm pitch LFCSP	35	3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

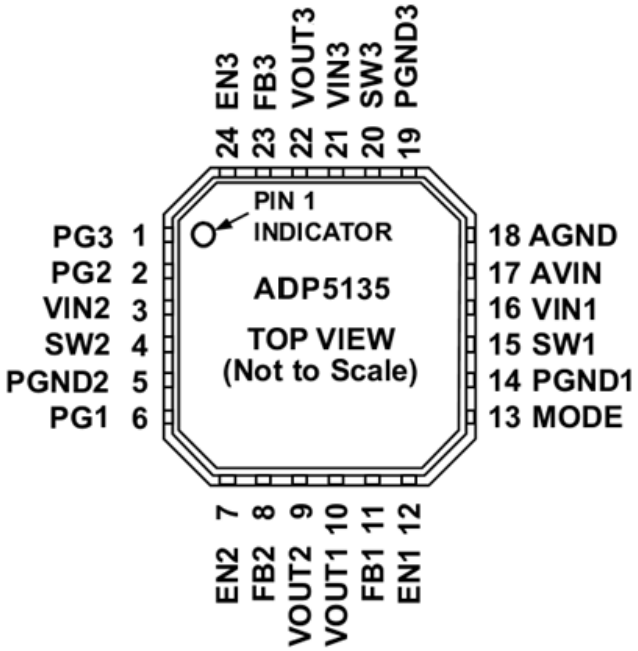


Figure 2. Pin Configuration—View from the Top of the Die

Table 7. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PG3	Open drain Power Good pin output to monitor the output voltage of BUCK3.
2	PG2	Open drain Power Good pin output to monitor the output voltage of BUCK2.
3	VIN2	BUCK2 Input Supply (3.0 V to 5.5 V). Connect VIN2 to VIN1, VIN3 and AVIN.
4	SW2	BUCK2 Switching Node.
5	PGND2	Dedicated Power Ground for BUCK2.
6	PG1	Open drain Power Good pin output to monitor the output voltage of BUCK1.
7	EN2	BUCK2 Enable Pin. High level turns on this regulator, and low level turns it off.
8	FB2	BUCK2 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the BUCK2 resistor divider. For device models with a fixed output voltage, leave this pin unconnected.
9	VOUT2	BUCK2 Output Voltage Sensing Input. Connect VOUT2 to the top of the capacitor on VOUT2.
10	VOUT1	BUCK1 Output Voltage Sensing Input. Connect VOUT1 to the top of the capacitor on VOUT1.
11	FB1	BUCK1 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the BUCK1 resistor divider. For device models with a fixed output voltage, leave this pin unconnected.
12	EN1	BUCK1 Enable Pin. High level turns on this regulator, and low level turns it off.
13	MODE	BUCK1/BUCK2 Operating Mode. MODE = high: forced PWM operation. MODE = low: auto PWM/PSM operation.
14	PGND1	Dedicated Power Ground for BUCK1.
15	SW1	BUCK1 Switching Node.

16	VIN1	BUCK1 Input Supply (3.0 V to 5.5 V). Connect VIN1 to VIN2, VIN3 and AVIN.
17	AVIN	Analog Input Supply (3.0 V to 5.5 V). Connect AVIN to VIN1, VIN2 and VIN3.
18	AGND	Analog Ground.
19	PGND3	Dedicated Power Ground for BUCK3.
20	SW3	BUCK3 Switching Node.
21	VIN3	BUCK3 Input Supply (3.0 V to 5.5 V). Connect VIN3 to VIN1, VIN2 and AVIN.
22	VOUT3	BUCK3 Output Voltage Sensing Input. Connect VOUT3 to the top of the capacitor on VOUT3.
23	FB3	BUCK3 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the BUCK3 resistor divider. For device models with a fixed output voltage, leave this pin unconnected.
24	EN3	BUCK3 Enable Pin. High level turns on this regulator, and low level turns it off.
EPAD	EP	Exposed Pad. It is recommended that the exposed pad be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN1} = V_{IN2} = V_{IN3} = 3.6$ V, $T_A = 25°C$, unless otherwise noted.

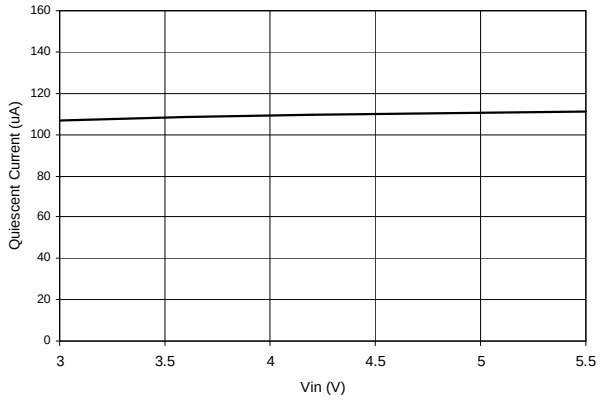


Figure 3. System Quiescent Current vs. Input Voltage, $V_{OUT1} = 3.3$ V, $V_{OUT2} = 1.8$ V, $V_{OUT3} = 1.2$ V, All Channels Unloaded

Figure 4. BUCK1 Startup, $V_{OUT1} = 1.2$V, $I_{OUT1} = 10$ mA

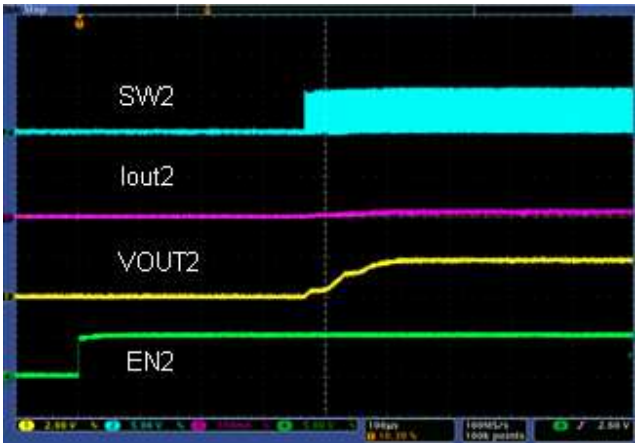


Figure 5. BUCK2 Startup, $V_{OUT2} = 1.8$ V, $I_{OUT2} = 10$ mA

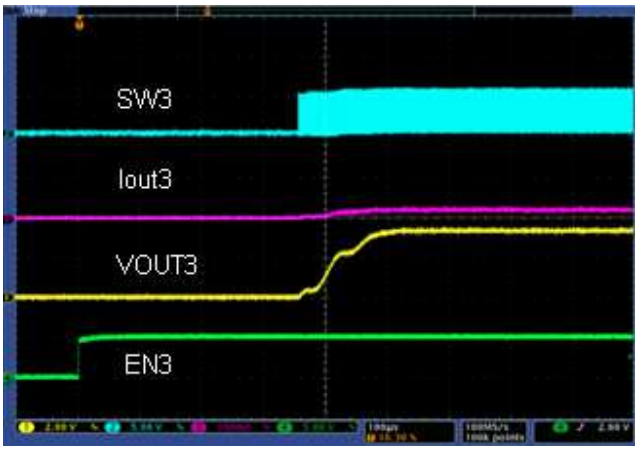


Figure 6. BUCK3 Start-up, $V_{OUT3} = 3.3$ V, $I_{OUT3} = 20$ mA

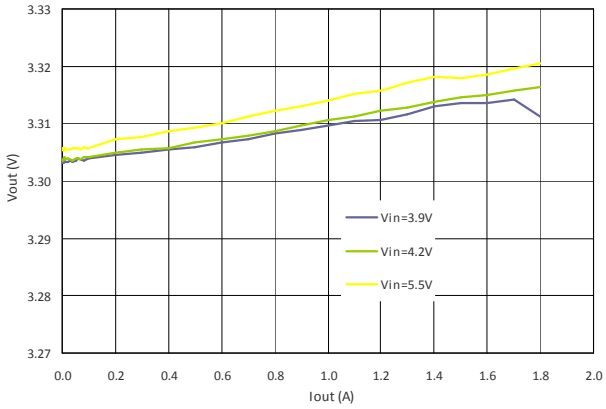


Figure 7. BUCK1 Load Regulation Across Vin, $V_{OUT1} = 3.3$ V, PWM Mode

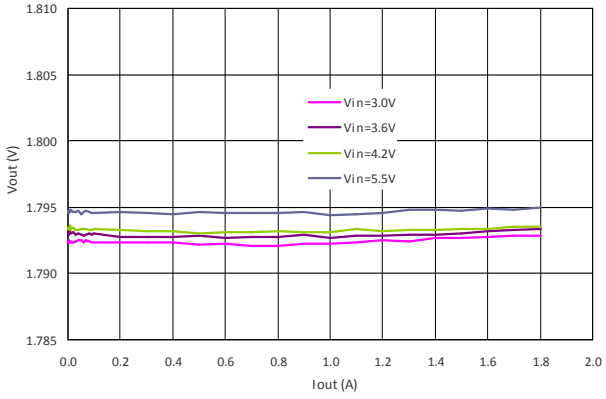


Figure 8. BUCK2 Load Regulation Across Vin, $V_{OUT2} = 1.8$ V, PWM Mode

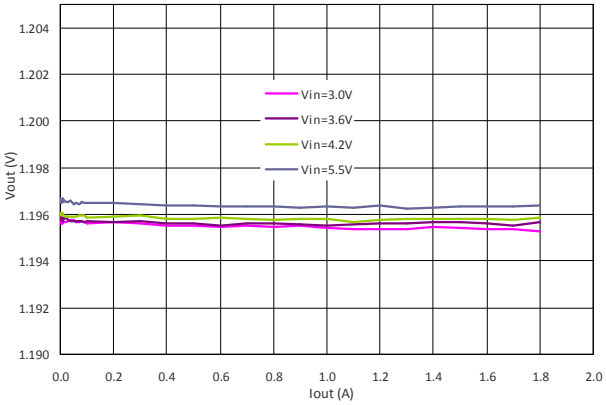


Figure 9. BUCK3 Load Regulation Across Vin, V_{OUT3} = 1.2 V, PWM Mode

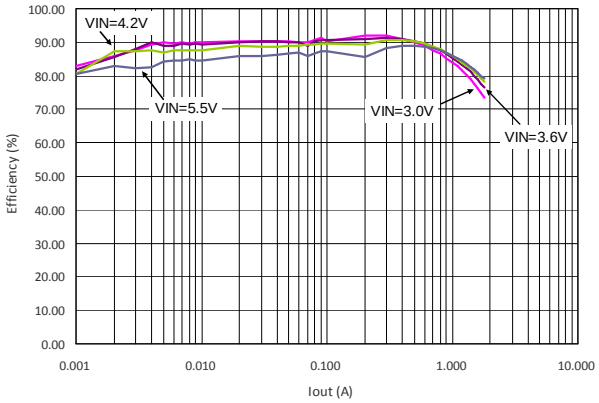


Figure 12. BUCK2 Efficiency vs Load Current, Across Input Voltage, V_{OUT2} = 1.8V, Auto Mode

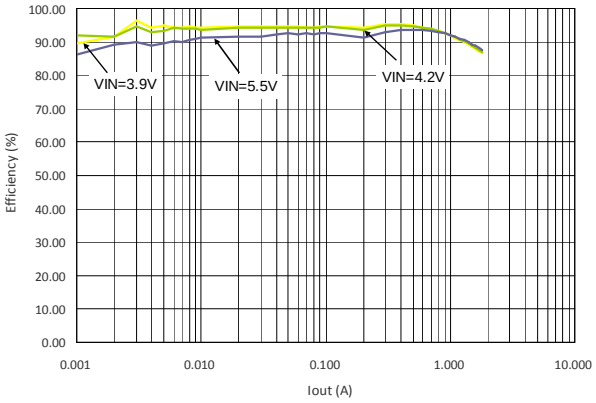


Figure 10. BUCK1 Efficiency vs Load Current, Across Input Voltage, V_{OUT1} = 3.3V, Auto Mode

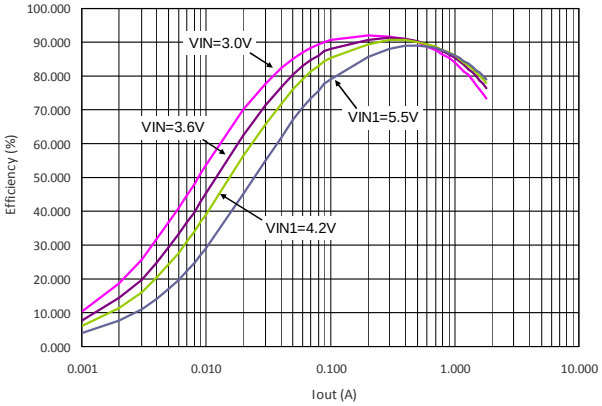


Figure 13. BUCK2 Efficiency vs Load Current, Across Input Voltage, V_{OUT2} = 1.8V, PWM Mode

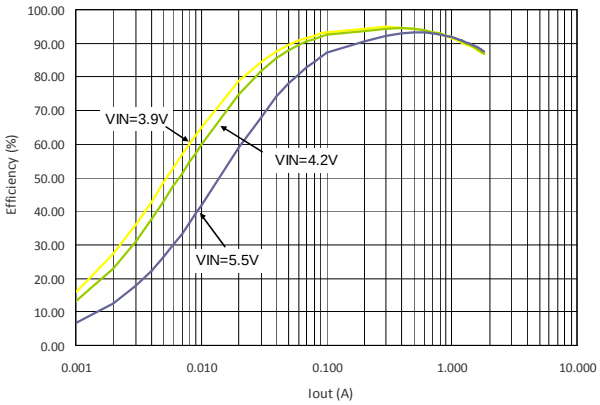


Figure 11. BUCK1 Efficiency vs Load Current, Across Input Voltage, V_{OUT1} = 3.3V, PWM Mode

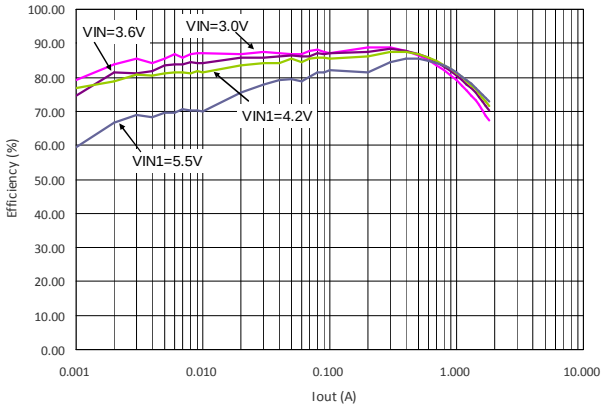


Figure 14. BUCK3 Efficiency vs Load Current, Across Input Voltage, V_{OUT3} = 1.2V, Auto Mode

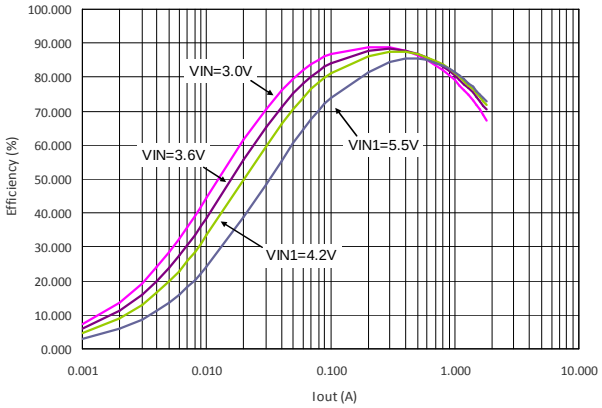


Figure 15. BUCK3 Efficiency vs Load Current, Across Input Voltage, V_{OUT3} = 1.2V, PWM Mode

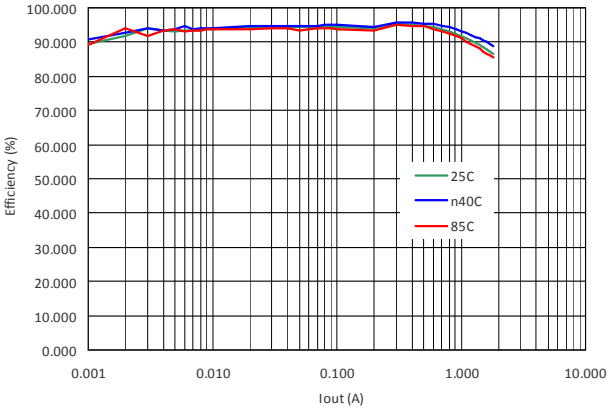


Figure 16. BUCK1 Efficiency vs Load Current, Across Temperature, V_{OUT1} = 3.3V, Auto Mode

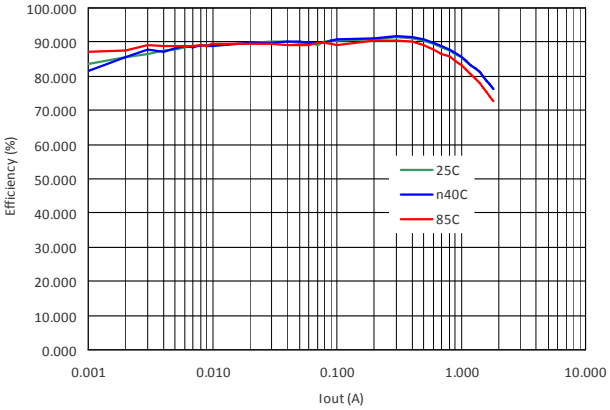


Figure 17. BUCK2 Efficiency vs Load Current, Across Temperature, V_{OUT2} = 1.8V, Auto Mode

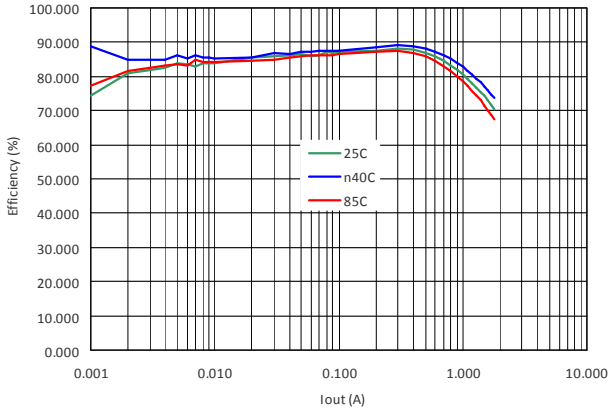


Figure 18. BUCK3 Efficiency vs Load Current, Across Temperature, V_{OUT3} = 1.2V, Auto Mode

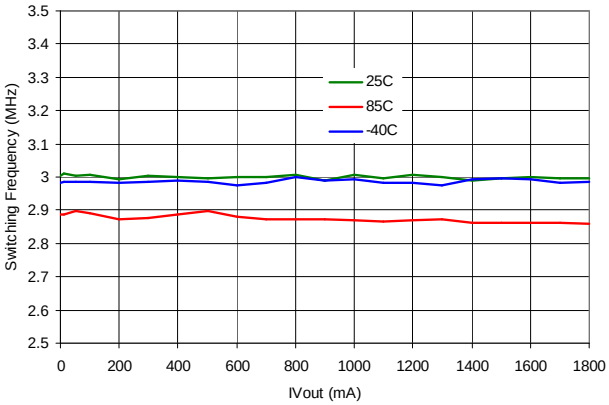


Figure 19. BUCK2 Switching Frequency vs. Load Current, Across Temperature, V_{OUT2} = 1.8V, PWM Mode

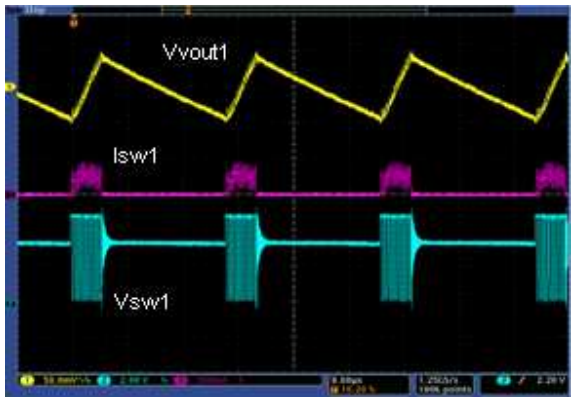


Figure 20. Typical Waveforms, V_{OUT1} = 3.3V, Load current=50mA, Auto Mode

Figure 21. Typical Waveforms, V_{OUT2} = 1.8V, Load current=50mA, Auto Mode

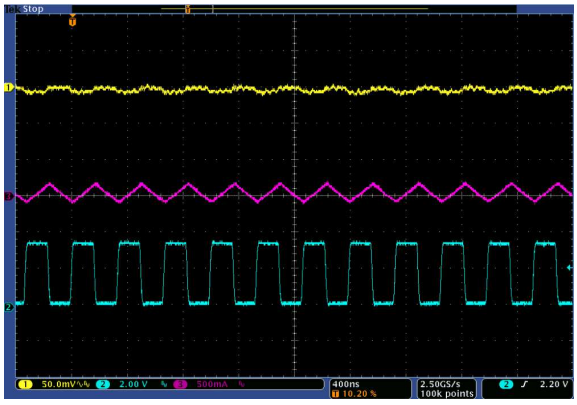


Figure 24. Typical Waveforms, V_{OUT2} = 1.8V, Load current=50mA, PWM Mode

Figure 22. Typical Waveforms, V_{OUT3} = 1.2V, Load current=50mA, Auto Mode

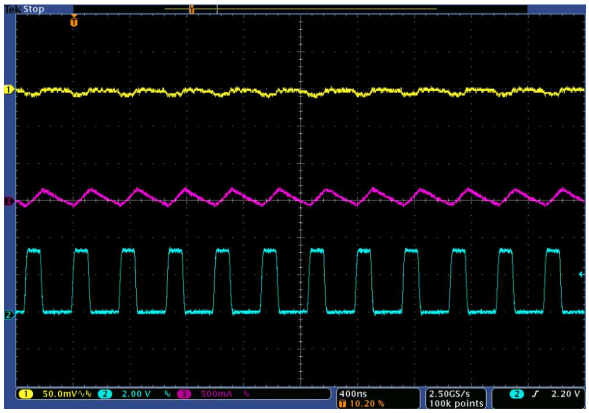


Figure 25. Typical Waveforms, V_{OUT3} = 1.2V, Load current=50mA, PWM Mode

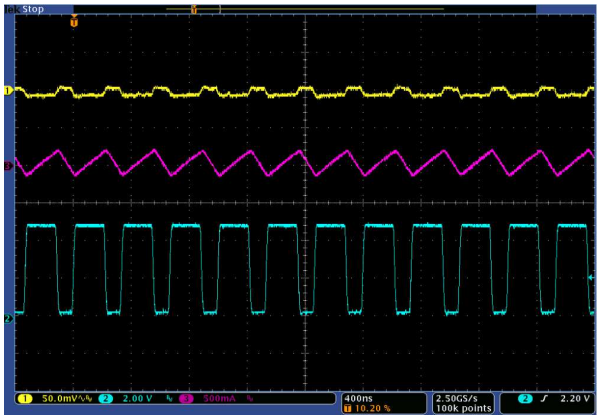


Figure 23. Typical Waveforms, V_{OUT1} = 3.3V, Load current=50mA, PWM Mode

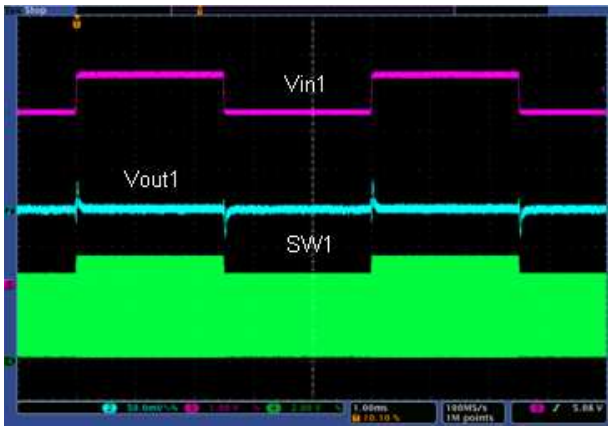


Figure 26. BUCK1 Response to Line Transient, Input Voltage from 4.5V to 5.5V, V_{OUT1} = 3.3V, Load current=50mA, PWM Mode

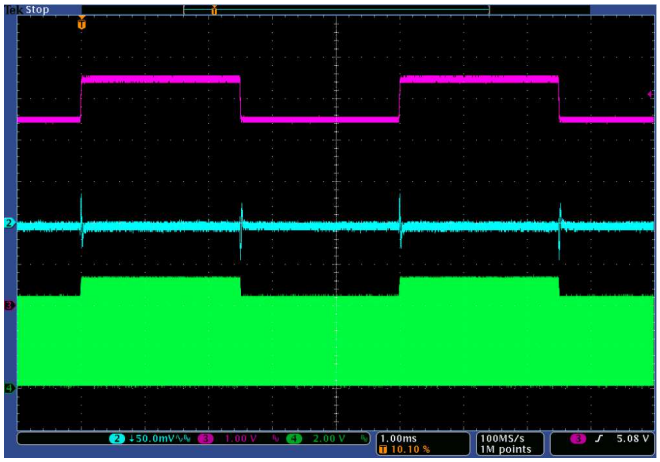


Figure 27. BUCK2 Response to Line Transient, Input Voltage from 4.5V to 5.5V, V_{OUT2} = 1.8V, Load current=50mA, PWM Mode

Figure 28. BUCK3 Response to Line Transient, Input Voltage from 4.0V to 5.0V, V_{OUT3} = 1.2V, Load current=50mA, PWM Mode

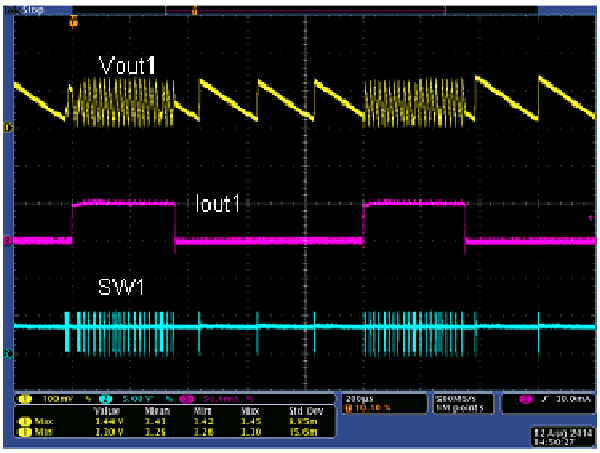


Figure 29. BUCK1 Response to Load Transient, Load current from 1mA to 50mA, V_{OUT1} = 3.3V, Auto Mode

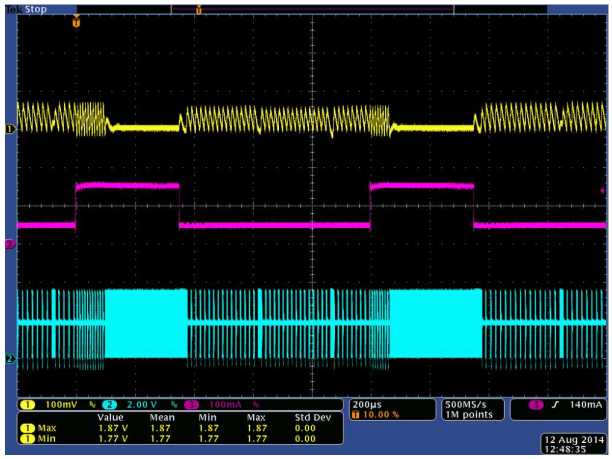


Figure 30. BUCK2 Response to Load Transient, Load current from 50mA to 200mA, V_{OUT2} = 1.8V, Auto Mode

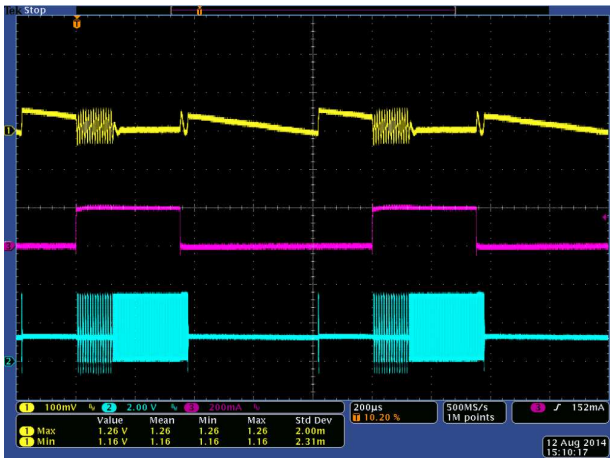


Figure 31. BUCK3 Response to Load Transient, Load current from 1mA to 200mA, V_{OUT3} = 1.2V, Auto Mode

Figure 32. BUCK2 Response to Load Transient, Load current from 1mA to 200mA, V_{OUT3} = 1.2V, PWM Mode

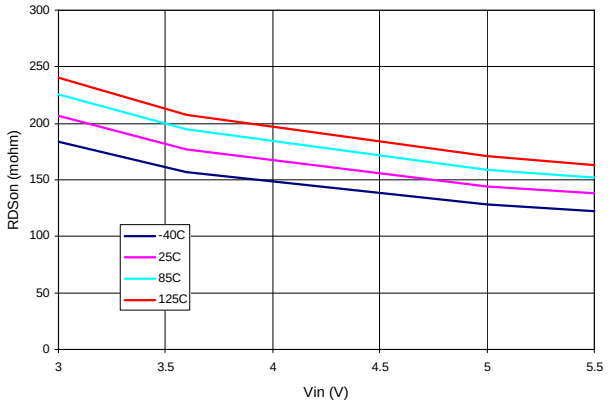


Figure 33. LFCSP PMOS RDson vs Input Voltage Across Temperature

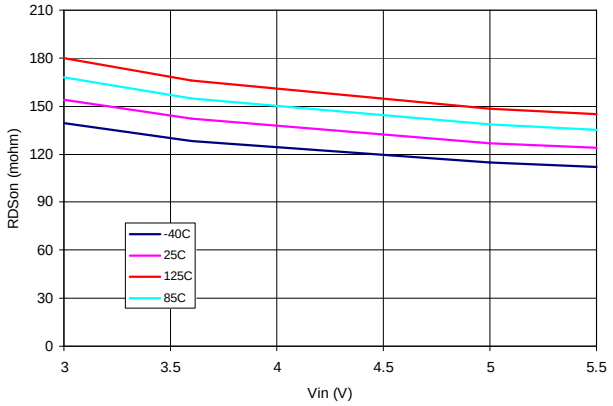


Figure 34. LFCSP NMOS RDson vs Input Voltage Across Temperature

THEORY OF OPERATION

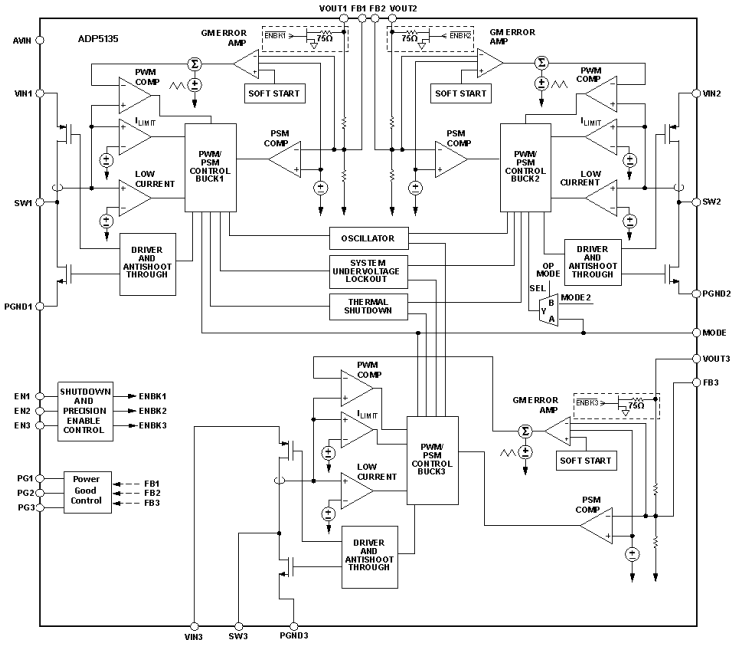


Figure 35. Functional Block Diagram

POWER MANAGEMENT UNIT

The ADP5135 is a micropower management unit (micro PMU) combining three step-down (buck) dc-to-dc converters. The high switching frequency and tiny 24-lead LFCSP package allow for a small power management solution.

To combine these high performance regulators into the micro PMU, there is a system controller allowing them to operate together.

The buck regulators can operate in forced PWM mode if the MODE pin is at a logic high level. In forced PWM mode, the buck switching frequency is always constant and does not change with the load current. If the MODE pin is at logic low level, the switching regulators operate in auto PWM/PSM mode. In this mode, the regulators operate at fixed PWM frequency when the load current is above the PSM current threshold. When the load current falls below the PSM current threshold, the regulator in question enters PSM, where the switching occurs in bursts. The burst repetition rate is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses. The auto PWM/PSM mode transition is controlled independently for each buck regulator. BUCK1 and BUCK2 operate in phase with the internal clock, BUCK3 operates out of phase from it.

The ADP5135 has individual enable pins (EN1 to EN3) controlling the activation of each regulator. The regulators are activated by a logic level high applied to the respective EN pin. EN1 controls BUCK1, EN2 controls BUCK2, EN3 controls BUCK3.

Regulator output voltages are set through external resistor dividers or can be optionally factory programmed to default values (see the Ordering Guide section).

When a regulator is turned on, the output voltage ramp rate is controlled through a soft start circuit to avoid a large inrush current due to the charging of the output capacitors.

Power Good Output

Power good outputs are available for each Buck channel to monitor their respective output voltages. The PGx pin can connect to a pull-up current to drive external regulators or other circuits. In this configuration, the PGx pin goes high when the channel being monitored is in regulation and goes low when the output voltage falls below 85% of the nominal VOUTx level. The PGx pin can also drive an LED for fault monitoring. In this configuration, a red LED for example is biased and current sinks into the PGx pin when the output voltage falls below 85% of the nominal VOUTx level thereby turning ON the LED, and turns off when the output voltage is in regulation.

Thermal Protection

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off all the regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the regulators do not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, all regulators restart with soft start control.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated into the system. If the input voltage on AVIN drops below the UVLO threshold, 2.5V minimum, all channels shut down. In the buck channels, both the power switch and the synchronous rectifier turn off. When the voltage on AVIN rises above the UVLO threshold, the part is enabled once more.

Alternatively, the user can request a new device model with a UVLO set at a higher level, suitable for 5 V supply applications. For these models, the device reaches the turn-off threshold when the input supply drops to 3.65 V typical. The UVLO settings can also be set to a lower level, suitable for low voltage operations. To order a device with options other than the default options listed in the ordering guide section, please contact your local Analog Devices sales or distribution representative.

In case of a thermal or UVLO event, the active pull-downs (if factory enabled) are enabled to discharge the output capacitors quickly. The pull-down resistors remain engaged until the thermal fault event is no longer present or the input supply voltage falls below the V_{POR} voltage level. The typical value of V_{POR} is approximately 1 V.

Precision Enable and Shutdown Control

The ADP5135 has an individual enable control pin for each regulator. A voltage input to the ENx pin above the V_{IH_EN} level puts the part out of shutdown and turns on the housekeeping block of the ADP5135. As the VENx level continues to rise above the precision enable threshold (V_{ENR}), the regulators activate.

When all the VENx goes 80mV typical below the V_{ENR} level, the regulators deactivate, and as all the VENx level continues to go down below the V_{IL_EN} level, the part goes into shutdown mode. In this mode, the current consumption of the part drops to below 1uA.

Figure 36 shows the activation timings for the ADP5135 when regulators are in sequence, Vout1 controlling EN2, and Vout2 controlling EN3. Also shown are the individual power good signals monitoring all regulators.

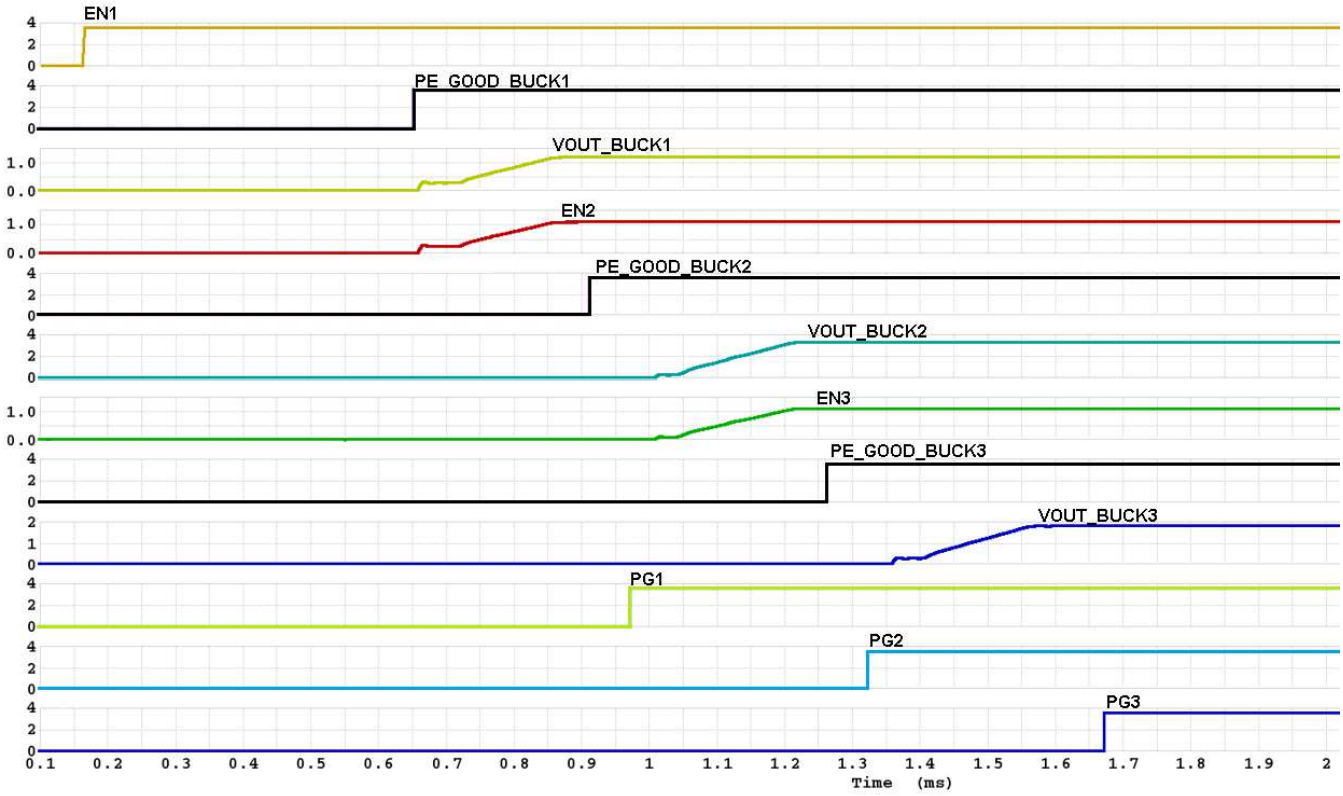


Figure 36. Regulator Sequencing on the ADP5135, showing precision enable thresholds, with PG

BUCK1, BUCK2 AND BUCK3

The buck uses a fixed frequency and high speed current mode architecture. The buck operates with an input voltage of 3.0 V to 5.5 V.

The buck regulator output voltage is resistor programmable from 0.8V up to 3.8V, shown in Figure 37 for BUCK1. The ratio of R1 and R2 multiplied by the feedback voltage determines the voltage level at the output. If for example, R1 and R2 were chosen to have equal resistance values, the output voltage is set to 1.0V. The output voltage can optionally be factory programmed to default values as indicated in the Ordering Guide section. In this event, R1 and R2 are not needed, and FB1 can be left unconnected. In all cases, VOUT1 must be connected to the output capacitor. FB1 is 0.5 V.

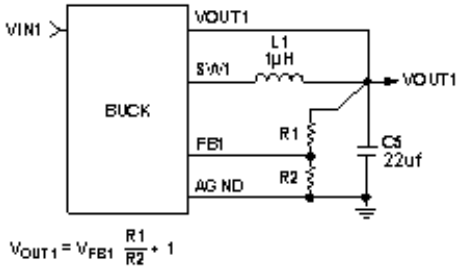


Figure 37. BUCK1 External Output Voltage Setting

Control Scheme

The bucks operate with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency but shift to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner, with higher output voltage ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM Mode

In PWM mode, the bucks operate at a fixed frequency of 3 MHz set by an internal oscillator. At the start of each oscillator cycle, the pFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the pFET switch and turns on the nFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

The bucks smoothly transition to PSM operation when the load current decreases below the PSM current threshold. When any of the bucks enters PSM, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck enters an idle mode. The output capacitor discharges until the output voltage falls to the PWM regulation voltage, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current is below the PSM current threshold.

The ADP5135 has a dedicated MODE pin controlling the PSM and PWM operations. A high logic level applied to the MODE pin forces all bucks to operate in PWM mode. A logic level low sets the bucks to operate in auto PSM/PWM.

PSM Current Threshold

The PSM current threshold is set to100 mA. The bucks employ a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to and exit from the PSM. The PSM current threshold is optimized for excellent efficiency over all load currents.

Oscillator/Phasing of Inductor Switching

The ADP5135 ensures that all three bucks operate at the same switching frequency when all bucks are in PWM mode.

Additionally, the ADP5135 ensures that when all bucks are in PWM mode, BUCK3 operates out of phase with BUCK1 and BUCK2, whereby the BUCK3 pFET starts conducting exactly half a clock period after the BUCK1 and BUCK2 pFETs start conducting.

Short-Circuit Protection

The bucks include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Buck Soft Start

The bucks have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

Each buck has protection circuitry to limit the amount of positive current flowing through the pFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Operation

With a drop in input voltage, or with an increase in load current, the buck may reach a limit where, even with the pFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck transitions to a mode where the pFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

Active Pull-Downs

All regulators have optional, factory programmable, active pull-down resistors discharging the respective output capacitors when the regulators are disabled. The pull-down resistors are connected between VOUTx and AGND. Active pull-downs are disabled when the regulators are turned on. The typical value of the pull-down resistor is 75 Ω.

APPLICATIONS INFORMATION

BUCK EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Feedback Resistors

For the adjustable model, referring to Figure 37 the total combined resistance for R1 and R2 is not to exceed 400 kΩ.

Inductor

The high switching frequency of the ADP5135 bucks allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Suggested inductors are shown in Tables 8 and 9.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the bucks are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low EMI.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 9.2 µF at 1.8 V, as shown in Figure38.

Substituting these values in the equation yields

$$C_{EFF} = 9.2\ \mu F \times (1 - 0.15) \times (1 - 0.1) \approx 7.0\ \mu F$$

To guarantee the performance of the bucks, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

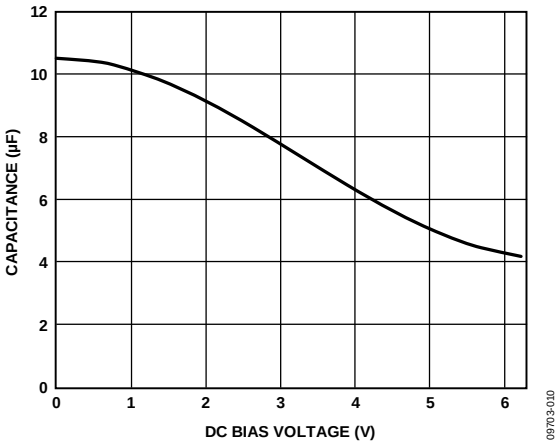


Figure 38. Capacitance vs. Voltage Characteristic

Table 8. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM2HPN1R0MJHL	2.5 × 2.0 × 1.2	3500	50
Wurth Electronics	74438323010	2.5 × 2.0 × 1.0	4000	75
Coilcraft®	XFL4020-102ME	4.0 × 4.0 × 2.1	5100	11.9

Table 9. Suggested 2.2 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Wurth Electronics	74438335022	3.0 × 3.0 × 1.5	3500	108
TDK	VLCF5020T-2R2N2R6-1	5.0 × 5.0 × 2.0	2620	71
Taiyo Yuden	NP04SZB2R2N	5.0 × 5.0 × 2.0	2700	42
Coilcraft	XFL4020-222ME	4.0 × 4.0 × 2.1	3500	23.5

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \approx \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times C_{OUT}}$$

Capacitors with lower effective series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \le \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective Cout needed for stability, which includes temperature and dc bias effects, is a minimum of 7 µF and a maximum of 40 µF.

The buck regulators require typically 10 µF output capacitors to guarantee stability and response to rapid load variations and to transition into and out of the PWM/PSM modes, a 22uF output capacitor can also be used for applications that require larger load steps. A list of suggested capacitors is shown in Table 10. In certain applications where one or all buck regulators power a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 µF to 4.7 µF because the regulator does not expect a large load variation when working in PSM mode.

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \ge I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close as possible to the VINx pin of the buck. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 µF and a maximum of 10 µF. A list of suggested capacitors is shown in Table 10 and Table 11.

Table 10. Suggested 10 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3
Taiyo Yuden	X5R	JMK107BJ106MA-T	0603	6.3
Panasonic	X5R	ECJ1VB0J106M	0603	6.3

Table 11. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475ME19D	0402	6.3
Taiyo Yuden	X5R	JMK107BJ475	0402	6.3
Panasonic	X5R	ECJ-0EB0J475M	0402	6.3

Table 12. Suggested 1.0 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM155B30J105K	0402	6.3
Murata	X5R	GRM155R61A105KE15D	0402	10.0
TDK	X5R	C1005JB0J105KT	0402	6.3
Panasonic	X5R	ECJ0EB0J105K	0402	6.3
Taiyo Yuden	X5R	LMK105BJ105MV-F	0402	10.0

Table 13. Suggested 22.0 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60G226MEA0D	0603	6.3
TDK	X5R	C1608X5R0J226M080AC	0603	6.3
Taiyo Yuden	X5R	LMK212BJ226MG-T	0805	10.0

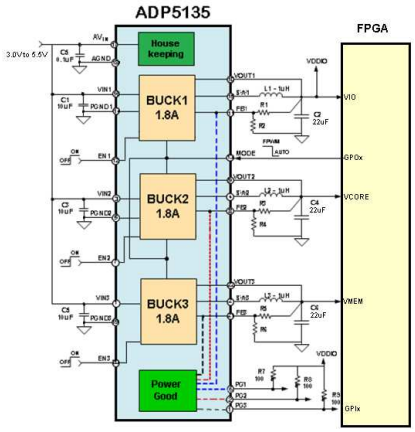


Figure 39. Processor System Power Management with PSM/PWM Control and PG

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The ADP5135 is a highly efficient µPMU, and, in most cases, the power dissipated in the device is not a concern. However, if the device operates at high ambient temperatures and maximum loading condition, the junction temperature can reach the maximum allowable operating limit (125°C).

When the temperature exceeds 150°C, the ADP5135 turns off all the regulators, allowing the device to cool down. When the die temperature falls below 130°C, the ADP5135 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device and ensure that the ADP5135 operates below the maximum allowable junction temperature.

The efficiency for each regulator on the ADP5135 is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (1)$$

where:
η is the efficiency.
P_{IN} is the input power.
P_{OUT} is the output power.

Power loss is given by

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (2a)$$

or

$$P_{LOSS} = P_{OUT}(1-\eta)/\eta \quad (2b)$$

Power dissipation can be calculated in several ways. The most intuitive and practical is to measure the power dissipated at the input and all the outputs. Perform the measurements at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is dissipated in the device and the inductor. Use Equation 4 to derive the power lost in the inductor and, from this, use Equation 3 to calculate the power dissipation in the ADP5135 buck converter.

A second method to estimate the power dissipation uses the efficiency curves provided for the buck regulator. When the buck efficiency is known, use Equation 2b to derive the total power lost in the buck regulator and inductor, use Equation 4 to derive the power lost in the inductor, and then calculate the power dissipation in the buck converter using Equation 3. Add the power dissipated in the three bucks to find the total dissipated power.

Note that the buck efficiency curves are typical values and may not be provided for all possible combinations of V_{IN}, V_{OUT}, and I_{OUT}. To account for these variations, it is necessary to include a safety margin when calculating the power dissipated in the buck.

A third way to estimate the power dissipation is analytical and involves modeling the losses in the buck circuit provided by Equation 8 to Equation 11.

BUCK REGULATOR POWER DISSIPATION

The power loss of the buck regulator is approximated by

$$P_{LOSS} = P_{DBUCK} + P_L \quad (3)$$

where:
P_{DBUCK} is the power dissipation on one of the ADP5135 buck regulators.
P_L is the inductor power losses.

The inductor losses are external to the device, and they do not have any effect on the die temperature.

The inductor losses are estimated (without core losses) by

$$P_L \approx I_{OUT1(RMS)}^2 \times DCR_L \quad (4)$$

where:
DCR_L is the inductor series resistance.
$I_{OUT1(RMS)}$ is the rms load current of the buck regulator.

$$I_{OUT1(RMS)} = I_{OUT1} \times \sqrt{1 + \frac{r}{12}} \quad (5)$$

where r is the normalized inductor ripple current.

$$r = V_{OUT1} \times (1 - D)/(I_{OUT1} \times L \times f_{SW}) \quad (6)$$

where:
L is the inductance.
f_{SW} is the switching frequency.
D is the duty cycle.

$$D = V_{OUT1}/V_{IN1} \quad (7)$$

ADP5135 buck regulator power dissipation, P_{DBUCK}, includes the power switch conductive losses, the switch losses, and the transition losses of each channel. There are other sources of loss, but these are generally less significant at high output load currents, where the thermal limit of the application is. Equation 8 captures the calculation that must be made to estimate the power dissipation in the buck regulator.

$$P_{DBUCK} = P_{COND} + P_{SW} + P_{TRAN} \quad (8)$$

The power switch conductive losses are due to the output current, I_{OUT1}, flowing through the P-MOSFET and the N-MOSFET power switches that have internal resistance, RDS_{ON-P} and RDS_{ON-N}. The amount of conductive power loss is found by

$$P_{COND} = [RDS_{ON-P} \times D + RDS_{ON-N} \times (1 - D)] \times I_{OUT1(RMS)}^2 \quad (9)$$

where RDS_{ON-P} is approximately 0.19 Ω, and RDS_{ON-N} is approximately 0.14 Ω at 25°C junction temperature and VIN1 = VIN2 = 3.6 V. At VIN1 = VIN2 = 3.0 V, these values change to TBDΩ and TBD Ω, respectively, and at VIN1 = VIN2 = 5.5 V, the values are 0.15 Ω and 0.12 Ω, respectively.

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. The amount of switching power loss is given by

$$P_{SW} = (C_{GATE-P} + C_{GATE-N}) \times V_{IN1}^2 \times f_{SW} \quad (10)$$

where:
C_{GATE-P} is the P-MOSFET gate capacitance.
C_{GATE-N} is the N-MOSFET gate capacitance.

For the ADP5135, the total of (C_{GATE-P} + C_{GATE-N}) is approximately 150 pF.

The transition losses occur because the P-channel power MOSFET cannot be turned on or off instantaneously, and the SW node takes some time to slew from near ground to near V_{OUT1} (and from V_{OUT1} to ground). The amount of transition loss is calculated by

$$P_{TRAN} = V_{IN1} \times I_{OUT1} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (11)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node, SW. For the ADP5135, the rise and fall times of SW are in the order of 5 ns.

If the preceding equations and parameters are used for estimating the converter efficiency, it must be noted that the equations do not describe all of the converter losses, and the parameter values given are typical numbers. The converter performance also depends on the choice of passive components and board layout; therefore, a sufficient safety margin should be included in the estimate.

The total power dissipation in the ADP5135 simplifies to

$$P_D = P_{DBUCK1} + P_{DBUCK2} + P_{DBUCK3} \quad (12)$$

JUNCTION TEMPERATURE

In cases where the board temperature, T_A, is known, the thermal resistance parameter, θ_{JA}, can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (13)$$

Refer to Table 6 for the thermal resistance values of the LFCSP package. A very important factor to consider is that θ_{JA} is based on a 4-layer 4 in × 3 in, 2.5 oz copper, as per JEDEC standard, and real applications may use different sizes and layers. It is important to maximize the copper used to remove the heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. The exposed pad should be connected to the ground plane with several vias.

If the case temperature can be measured, the junction temperature is calculated by

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (14)$$

where T_C is the case temperature and θ_{JC} is the junction-to-case thermal resistance provided in Table 6.

When designing an application for a particular ambient temperature range, calculate the expected ADP5135 power dissipation (P_D) due to the losses of all channels by using the Equation 8 to Equation 12. From this power calculation, the junction temperature, T_J, can be estimated using Equation 13.

The reliable operation of the converter can be achieved only if the estimated die junction temperature of the ADP5135 (Equation 14) is less than 125°C. Reliability and mean time between failures (MTBF) are highly affected by increasing the junction temperature. Additional information about product reliability can be found from the *ADI Reliability Handbook*, which can be found at www.analog.com/reliability_handbook.

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5135 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines. Also, refer to the UG-765 user guide.

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Connect VIN1, VIN2, VIN3, and AVIN together close to the IC using short tracks.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- For best performance, connect the input caps very close to the dut pins, place the Avin cap between the AVIN and AGND pins, place the VIN1 cap between VIN1 and PGND1 pins, VIN2 cap between VIN2 and PGND2 pins, and place VIN3 cap between VIN3 and PGND3.

TYPICAL APPLICATION SCHEMATICS

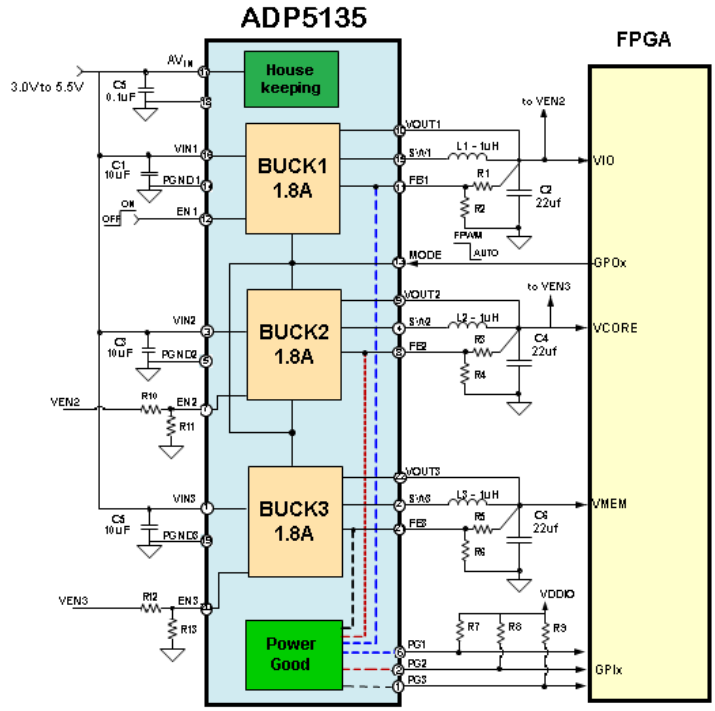


Figure 40. Typical Application, ADP5135 Adjustable Output Voltages with Precision Enable Pins

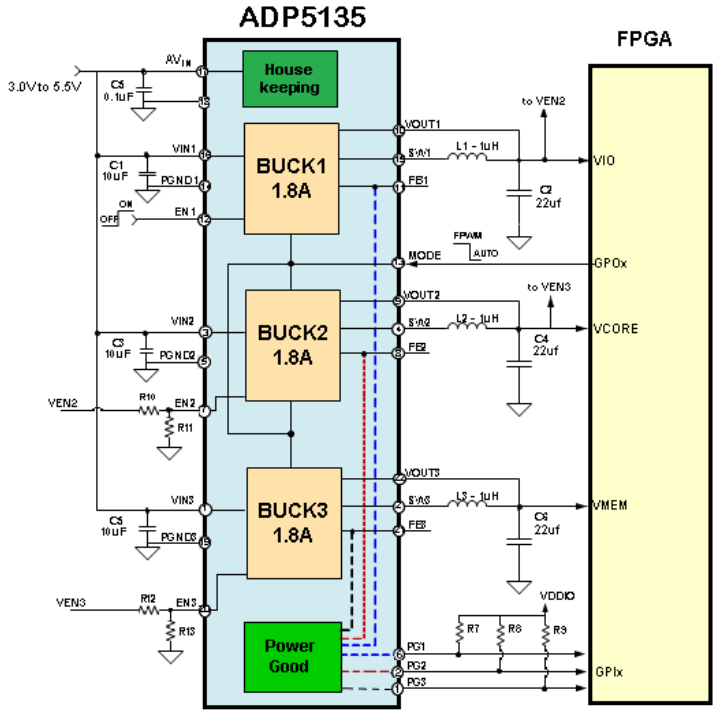
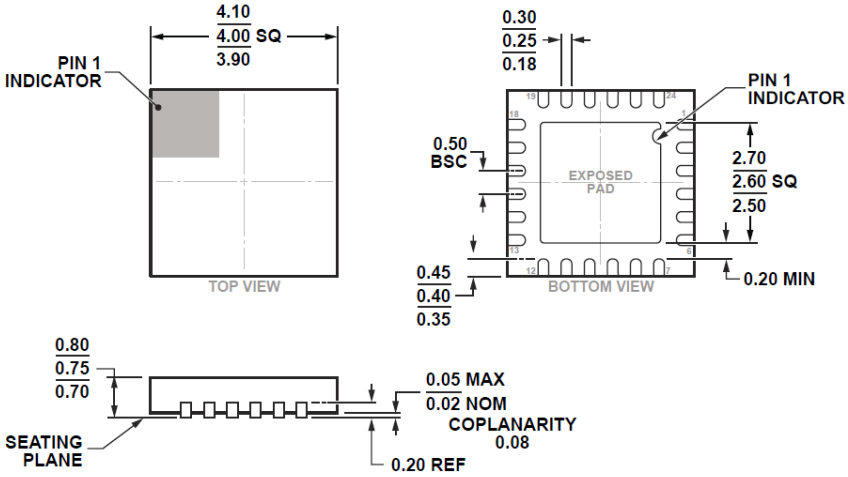


Figure 41. Typical Application, ADP5135 Fixed Output Voltages with Precision Enable Pins

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 42. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-15)
Dimensions shown in millimeters

PR12604-0-9/14(PrA)