REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 15-06-26	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, LINEAR, DUAL CHANNEL DIGITAL ISOLATOR, ENHANCED SYSTEM LEVEL ESD RELIABILITY, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14627**
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AMSC N/A

5962-V068-15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a dual channel digital isolator, enhanced system level electrostatic discharge (ESD) reliability microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14627	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADUM3210TRZ-EP	Dual channel digital isolator, enhanced system level ESD reliability

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltages range (V_{DD1}, V_{DD2}) ..... -0.5 V to +7.0 V 2/
Input voltage (V_{IA}, V_{IB}) ..... -0.5 V to V_{DDI} + 0.5 V 2/ 3/
Output voltage (V_{OA}, V_{OB}) ..... -0.5 V to V_{DDO} + 0.5 V 2/ 3/
Average output current per pin (I_O) ..... -22 mA to +22 mA 4/
Common mode transients (CM_H, CM_L) ..... -100 kV/μs to +100 kV/μs 5/
Storage temperature range (T_{STG}) ..... -55°C to +150°C

1.4 Recommended operating conditions. 6/

Supply voltages (V_{DD1}, V_{DD2}) ..... 3 V to 5.5 V 7/
Maximum input signal rise and fall times ..... 1 ms
Start-up current (I_{DD1}, I_{DD2}) ..... 20 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Package characteristics.

Resistance (input to output) (R_{I-O}) ..... 10^{12} Ω typical 8/
Capacitance (input to output) (C_{I-O}) (f = 1 MHz) ..... 1.0 pF typical 8/
Input capacitance (C_I) ..... 4.0 pF typical
Thermal resistance, junction to case (θ_{JCI}) side 1 ..... 46°C/W typical
Thermocouple located at center of package underside
Thermal resistance, junction to case (θ_{JCO}) side 2 ..... 41°C/W typical

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Each voltage is relative to its respective ground.
3/ V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
4/ See figure 4 for maximum allowable current values for various temperatures.
5/ Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum rating can cause latch up or permanent damage.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ All voltages are relative to their respective ground.
8/ The device is considered a 2 terminal device. Pin 1 through pin 4 are shorted together, and pin 5 through pin 8 are shorted together.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ V_{DD1} = V_{DD2} = 5 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current	I_{DD1}	1 Mbps	-55°C to +125°C	01		1.7	mA
			+25°C		1.3 typical		
		10 Mbps	-55°C to +125°C			4.8	
			+25°C		3.5 typical		
		25 Mbps	-55°C to +125°C			9.9	
			+25°C		7.6 typical		
	I_{DD2}	1 Mbps	-55°C to +125°C			1.6	
			+25°C		1.0 typical		
		10 Mbps	-55°C to +125°C			2.8	
			+25°C		2.0 typical		
		25 Mbps	-55°C to +125°C			5.1	
			+25°C		3.8 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	t_{PHL}, t_{PLH}	50% input to 50% output	-55°C to +125°C	01	20	50	ns
Pulse width distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	-55°C to +125°C	01		3	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	t_{PSK}	Between any two units	-55°C to +125°C	01		18	ns
Channel matching: codirectional	t_{PSKCD}		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	t_{PSKOD}		-55°C to +125°C	01		18	ns
Output rise/fall time	t_R / t_F	10% to 90%	+25°C	01	2.5 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $V_{DD1} = V_{DD2} = 5$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V_{IH}		-55°C to +125°C	01	0.7 V_{DDx}		V
Logic low input threshold	V_{IL}		-55°C to +125°C	01		0.3 V_{DDx}	V
Logic high output voltages	V_{OH}	I_{Ox} = -20 μA, VIx = VIxH	-55°C to +125°C	01	V_{DDx} – 0.1		V
			+25°C		V_{DDX} typical		
		I_{Ox} = -4 mA, VIx = VIxH	-55°C to +125°C		V_{DDx} – 0.5		
			+25°C		V_{DDX} – 0.2 typical		
Logic low output voltages	V_{OL}	I_{Ox} = 20 μA, VIx = VIxL	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I_{Ox} = 4 mA, VIx = VIxL	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I_I	0 V ≤ V_{Ix} ≤ V_{DDx}	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	$I_{DDI(Q)}$		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		
Quiescent output supply current	$I_{DDO(Q)}$		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $V_{DD1} = V_{DD2} = 5$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	$I_{DDI(D)}$		+25°C	01	0.19 typical		mA/ Mbps
Dynamic output supply current	$I_{DDO(D)}$		+25°C	01	0.05 typical		mA/ Mbps
AC specifications.							
Common mode 3/ transient immunity	|CM|	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/µs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.2 typical		Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/ V_{DD1} = V_{DD2} = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current	I_{DD1}	1 Mbps	-55°C to +125°C	01		1.3	mA
			+25°C		0.8 typical		
		10 Mbps	-55°C to +125°C			3.2	
			+25°C		2.1 typical		
		25 Mbps	-55°C to +125°C			6.1	
			+25°C		4.6 typical		
	I_{DD2}	1 Mbps	-55°C to +125°C			1.0	
			+25°C		0.7 typical		
		10 Mbps	-55°C to +125°C			1.9	
			+25°C		1.3 typical		
		25 Mbps	-55°C to +125°C			3.4	
			+25°C		2.4 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	t_{PHL}, t_{PLH}	50% input to 50% output	-55°C to +125°C	01	20	60	ns
Pulse width distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	-55°C to +125°C	01		4	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	t_{PSK}	Between any two units	-55°C to +125°C	01		22	ns
Channel matching: codirectional	t_{PSKCD}		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	t_{PSKOD}		-55°C to +125°C	01		20	ns
Output rise/fall time	t_R / t_F	10% to 90%	+25°C	01	3.0 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/ $V_{DD1} = V_{DD2} = 3.3$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V_{IH}		-55°C to +125°C	01	0.7 V_{DDx}		V
Logic low input threshold	V_{IL}		-55°C to +125°C	01		0.3 V_{DDx}	V
Logic high output voltages	V_{OH}	I_{Ox} = -20 μA, VIx = VIxH	-55°C to +125°C	01	V_{DDx} – 0.1		V
			+25°C		V_{DDX} typical		
		I_{Ox} = -2 mA, VIx = VIxH	-55°C to +125°C		V_{DDx} – 0.5		
			+25°C		V_{DDX} – 0.2 typical		
Logic low output voltages	V_{OL}	I_{Ox} = 20 μA, VIx = VIxL	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I_{Ox} = 2 mA, VIx = VIxL	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I_I	0 V ≤ V_{Ix} ≤ V_{DDx}	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	$I_{DDI(Q)}$		-55°C to +125°C	01		0.5	mA
			+25°C		0.3 typical		
Quiescent output supply current	$I_{DDO(Q)}$		-55°C to +125°C	01		0.5	mA
			+25°C		0.3 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/ V_{DD1} = V_{DD2} = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	$I_{DDI(D)}$		+25°C	01	0.10 typical		mA/ Mbps
Dynamic output supply current	$I_{DDO(D)}$		+25°C	01	0.03 typical		mA/ Mbps
AC specifications.							
Common mode 3/ transient immunity	|CM|	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/µs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.1 typical		Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5/ V_{DD1} = 5 V, V_{DD2} = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current	I_{DD1}	1 Mbps	-55°C to +125°C	01		1.7	mA
			+25°C		1.3 typical		
		10 Mbps	-55°C to +125°C			4.8	
			+25°C		3.5 typical		
		25 Mbps	-55°C to +125°C			9.9	
			+25°C		7.6 typical		
	I_{DD2}	1 Mbps	-55°C to +125°C			1.0	
			+25°C		0.7 typical		
		10 Mbps	-55°C to +125°C			1.9	
			+25°C		1.3 typical		
		25 Mbps	-55°C to +125°C			3.4	
			+25°C		2.4 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	t_{PHL}, t_{PLH}	50% input to 50% output	-55°C to +125°C	01	15	55	ns
Pulse width distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	-55°C to +125°C	01		3	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	t_{PSK}	Between any two units	-55°C to +125°C	01		22	ns
Channel matching: codirectional	t_{PSKCD}		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	t_{PSKOD}		-55°C to +125°C	01		20	ns
Output rise/fall time	t_R / t_F	10% to 90%	+25°C	01	3.0 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5/ V_{DD1} = 5 V, V_{DD2} = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V_{IH}		-55°C to +125°C	01	0.7 V_{DDx}		V
Logic low input threshold	V_{IL}		-55°C to +125°C	01		0.3 V_{DDx}	V
Logic high output voltages	V_{OH}	I_{Ox} = -20 μA, VIx = VIxH	-55°C to +125°C	01	V_{DDx} – 0.1		V
			+25°C		V_{DDX} typical		
		I_{Ox} = -2 mA, VIx = VIxH	-55°C to +125°C		V_{DDx} – 0.5		
			+25°C		V_{DDX} – 0.2 typical		
Logic low output voltages	V_{OL}	I_{Ox} = 20 μA, VIx = VIxL	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I_{Ox} = 2 mA, VIx = VIxL	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I_I	0 V ≤ V_{Ix} ≤ V_{DDx}	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	$I_{DDI(Q)}$		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		
Quiescent output supply current	$I_{DDO(Q)}$		-55°C to +125°C	01		0.5	mA
			+25°C		0.3 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5/ V_{DD1} = 5 V, V_{DD2} = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	$I_{DDI(D)}$		+25°C	01	0.19 typical		mA/ Mbps
Dynamic output supply current	$I_{DDO(D)}$		+25°C	01	0.03 typical		mA/ Mbps
AC specifications.							
Common mode 3/ transient immunity	|CM|	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V,	-55°C to +125°C	01	25		kV/µs
		transient magnitude = 800 V	+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.2 typical		Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/ V_{DD1} = 3.3 V, V_{DD2} = 5.0 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current	I_{DD1}	1 Mbps	-55°C to +125°C	01		1.3	mA
			+25°C		0.8 typical		
		10 Mbps	-55°C to +125°C			3.2	
			+25°C		2.1 typical		
		25 Mbps	-55°C to +125°C			6.1	
			+25°C		4.6 typical		
	I_{DD2}	1 Mbps	-55°C to +125°C			1.6	
			+25°C		1.0 typical		
		10 Mbps	-55°C to +125°C			2.8	
			+25°C		2.0 typical		
		25 Mbps	-55°C to +125°C			5.1	
			+25°C		3.7 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	t_{PHL}, t_{PLH}	50% input to 50% output	-55°C to +125°C	01	15	55	ns
Pulse width distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	-55°C to +125°C	01		4	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	t_{PSK}	Between any two units	-55°C to +125°C	01		22	ns
Channel matching: codirectional	t_{PSKCD}		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	t_{PSKOD}		-55°C to +125°C	01		20	ns
Output rise/fall time	t_R / t_F	10% to 90%	+25°C	01	2.5 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/ V_{DD1} = 3.3 V, V_{DD2} = 5.0 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V_{IH}		-55°C to +125°C	01	0.7 V_{DDx}		V
Logic low input threshold	V_{IL}		-55°C to +125°C	01		0.3 V_{DDx}	V
Logic high output voltages	V_{OH}	I_{Ox} = -20 μA, VIx = VIxH	-55°C to +125°C	01	V_{DDx} – 0.1		V
			+25°C		V_{DDX} typical		
		I_{Ox} = -2 mA, VIx = VIxH	-55°C to +125°C		V_{DDx} – 0.5		
			+25°C		V_{DDX} – 0.2 typical		
Logic low output voltages	V_{OL}	I_{Ox} = 20 μA, VIx = VIxL	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I_{Ox} = 2 mA, VIx = VIxL	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I_I	0 V ≤ V_{Ix} ≤ V_{DDx}	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	$I_{DDI(Q)}$		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		
Quiescent output supply current	$I_{DDO(Q)}$		-55°C to +125°C	01		0.8	mA
			+25°C		0.5 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/ V_{DD1} = 3.3 V, V_{DD2} = 5.0 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	$I_{DDI(D)}$		+25°C	01	0.10 typical		mA/ Mbps
Dynamic output supply current	$I_{DDO(D)}$		+25°C	01	0.05 typical		mA/ Mbps
AC specifications.							
Common mode 3/ transient immunity	|CM|	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V,	-55°C to +125°C	01	25		kV/µs
		transient magnitude = 800 V	+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.1 typical		Mbps

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and -55°C ≤ T_A ≤ +125°C.
Unless otherwise specified, switching specifications are tested with C_L = 15 pF and CMOS signal levels.

3/ |CM| is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

4/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and -55°C ≤ T_A ≤ +125°C.
Unless otherwise specified, switching specifications are tested with C_L = 15 pF and CMOS signal levels.

5/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and -55°C ≤ T_A ≤ +125°C.
Unless otherwise specified, switching specifications are tested with C_L = 15 pF and CMOS signal levels.

6/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and -55°C ≤ T_A ≤ +125°C.
Unless otherwise specified, switching specifications are tested with C_L = 15 pF and CMOS signal levels.

Case X

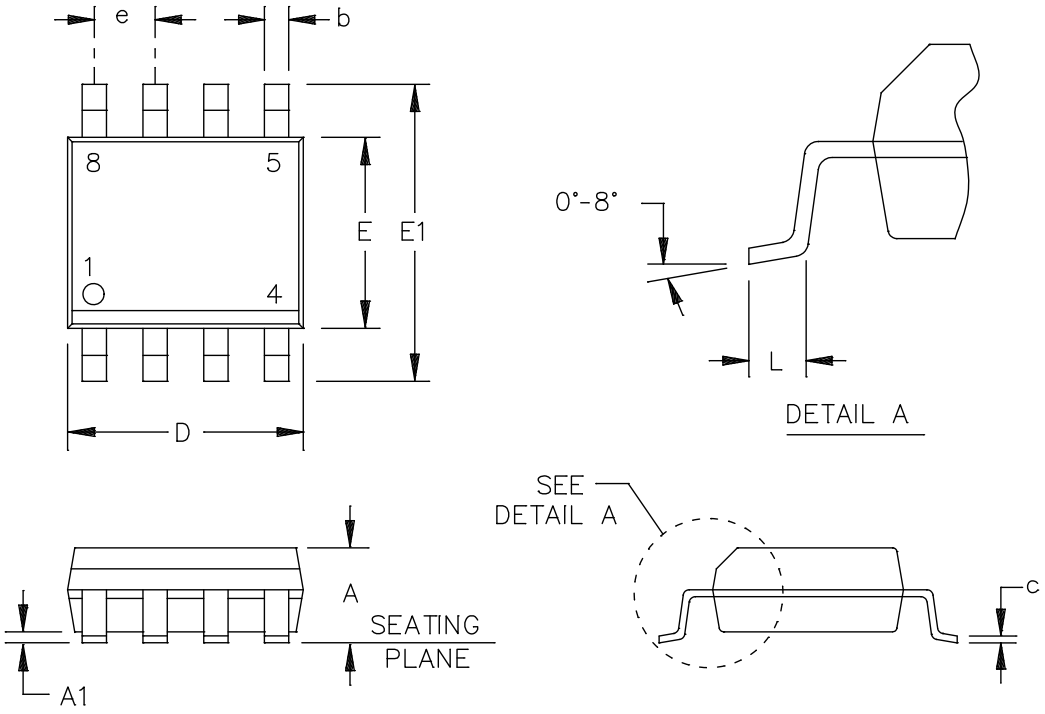

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14627
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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
b	0.0122	0.0201	0.31	0.51
c	0.0067	0.0098	0.17	0.25
D	0.1890	0.1968	4.80	5.00
e	0.0500 BSC		1.27 BSC	
E	0.1497	0.1574	3.80	4.00
E1	0.2284	0.2441	5.80	6.20
L	0.0157	0.0500	0.40	1.27
n	8 leads		8 leads	

NOTE:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only and are not appropriate for use in design.
2. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD1}	Supply voltage for isolator side 1, 3.0 V to 5.5 V
2	V_{IA}	Logic input A.
3	V_{IB}	Logic input B.
4	GND_1	Ground 1. Ground reference for isolator side 1.
5	GND_2	Ground 2. Ground reference for isolator side 2.
6	V_{OB}	Logic output B
7	V_{OA}	Logic output A.
8	V_{DD2}	Supply voltage for isolator side 2, 3.0 V to 5.5 V

FIGURE 2. Terminal connections.

Positive logic

V_{IA} input See note 1	V_{IB} input See note 1	V_{DD1} state	V_{DD2} state	V_{OA} output See note 1	V_{OB} output See note 1	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

NOTE 1. H is logic high, L is logic low, and X is don't care.

FIGURE 3. Truth table.

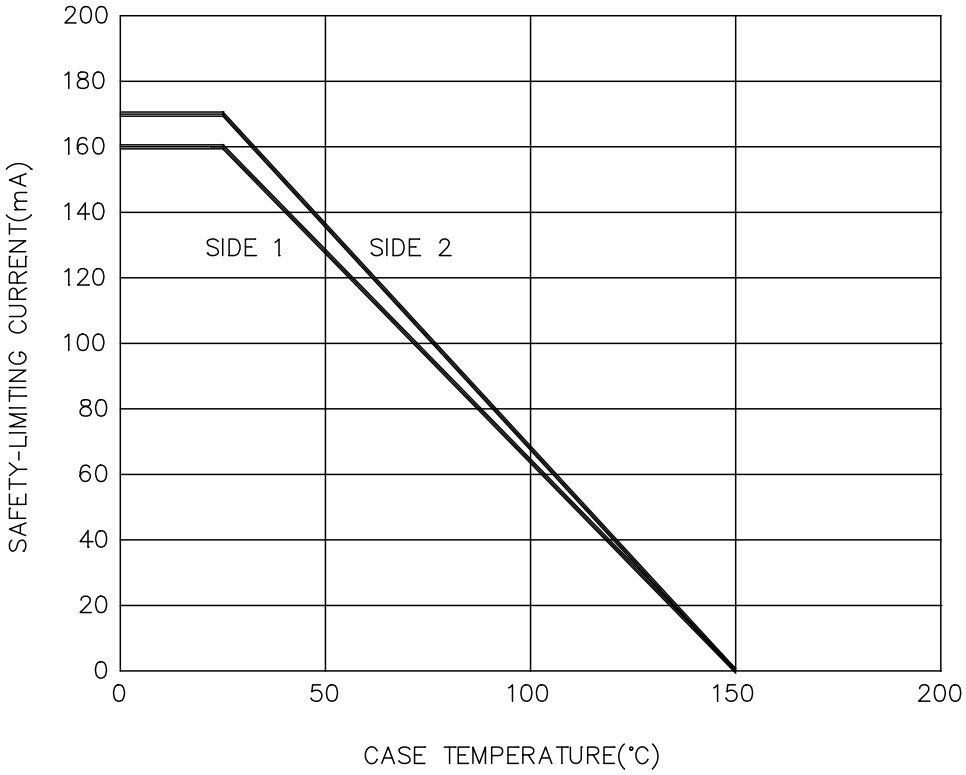

FIGURE 4. Thermal derating curve.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/14627-01XE	24355	ADUM3210TRZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland