

### General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low RDS(on) at 4.5V<sub>GS</sub>
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

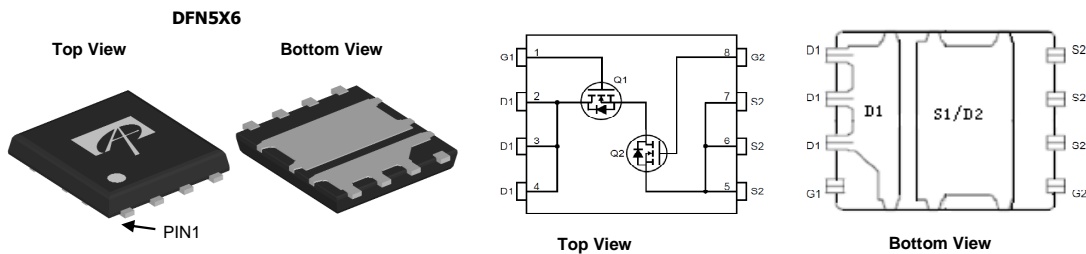
### Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

### Product Summary

	Q1	Q2
V <sub>DS</sub>	30V	30V
I <sub>D</sub> (at V <sub>GS</sub> =10V)	28A	42A
R <sub>DS(ON)</sub> (at V <sub>GS</sub> =10V)	<5mΩ	<2.4mΩ
R <sub>DS(ON)</sub> (at V <sub>GS</sub> = 4.5V)	<8.5mΩ	<3.2mΩ

100% UIS Tested  
 100% Rg Tested



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units	
Drain-Source Voltage	V <sub>DS</sub>	30		V	
Gate-Source Voltage	V <sub>GS</sub>	±20	±20	V	
Continuous Drain Current <sup>G</sup>	I <sub>D</sub>	T <sub>C</sub> =25°C	28	42	A
		T <sub>C</sub> =100°C	22	33	
Pulsed Drain Current <sup>C</sup>	I <sub>DM</sub>	112	168	A	
Continuous Drain Current	I <sub>DSM</sub>	T <sub>A</sub> =25°C	22	36	A
		T <sub>A</sub> =70°C	17	29	
Avalanche Current <sup>C</sup>	I <sub>AS</sub>	32	70	A	
Avalanche Energy L=0.05mH <sup>C</sup>	E <sub>AS</sub>	26	123	mJ	
V <sub>DS</sub> Spike	V <sub>SPIKE</sub>	36	36	V	
Power Dissipation <sup>B</sup>	P <sub>D</sub>	T <sub>C</sub> =25°C	31	78	W
		T <sub>C</sub> =100°C	12	31	
Power Dissipation <sup>A</sup>	P <sub>DSM</sub>	T <sub>A</sub> =25°C	3.6	4.3	W
		T <sub>A</sub> =70°C	2.3	2.7	
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150		°C	

### Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units	
Maximum Junction-to-Ambient <sup>A</sup>	R <sub>θJA</sub>	t ≤ 10s	29	24	35	29	°C/W
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	56	50	67	60	°C/W
Maximum Junction-to-Case	R <sub>θJC</sub>	3.3	1.2	4	1.6	°C/W	

**Q1 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.8	2.2	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		4.1	5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		6.7	8.5	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		91		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				28	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			951		pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		373		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			62		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.7	1.5	2.3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		15.7	22.5	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			7.5	10.5	nC
Q <sub>gs</sub>	Gate Source Charge			2.8		nC
Q <sub>gd</sub>	Gate Drain Charge			3.2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		6.25		ns
t <sub>r</sub>	Turn-On Rise Time			2.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			18.5		ns
t <sub>f</sub>	Turn-Off Fall Time			4		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		10.2		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		13.6		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> =25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

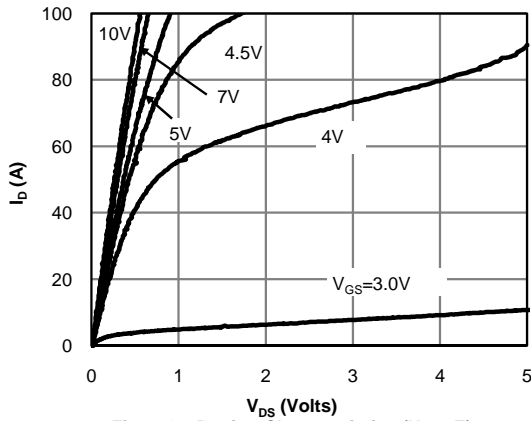
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

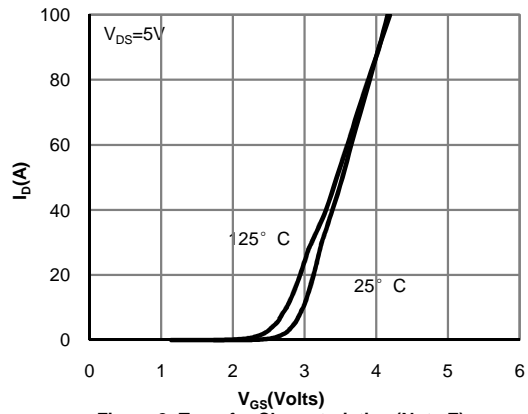
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

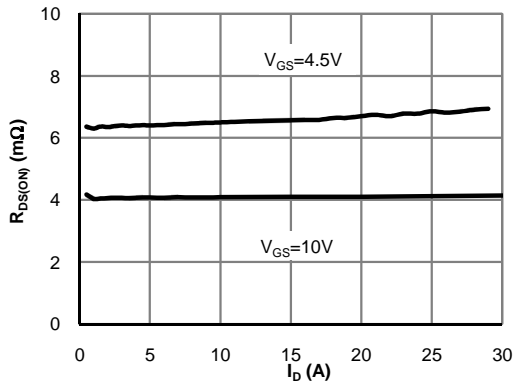
**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



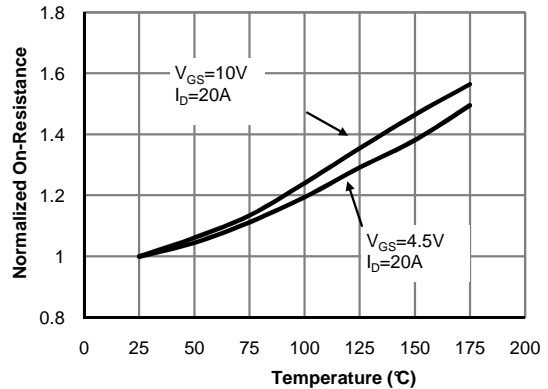
**Figure 1: On-Region Characteristics (Note E)**



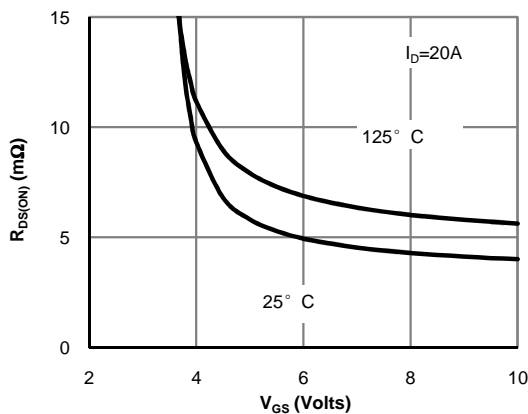
**Figure 2: Transfer Characteristics (Note E)**



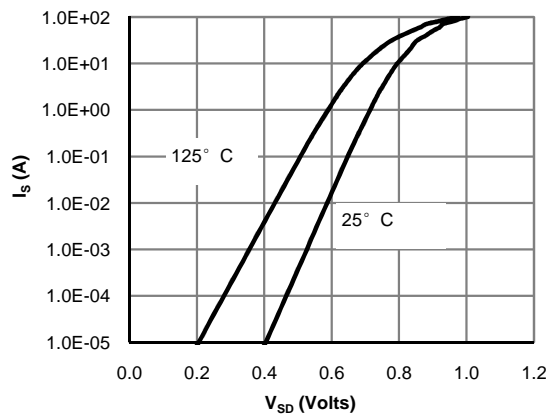
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

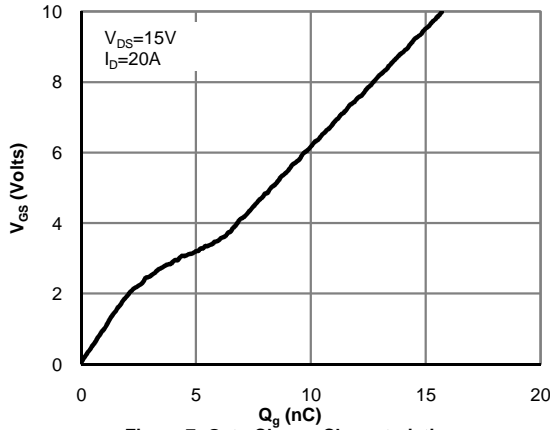


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

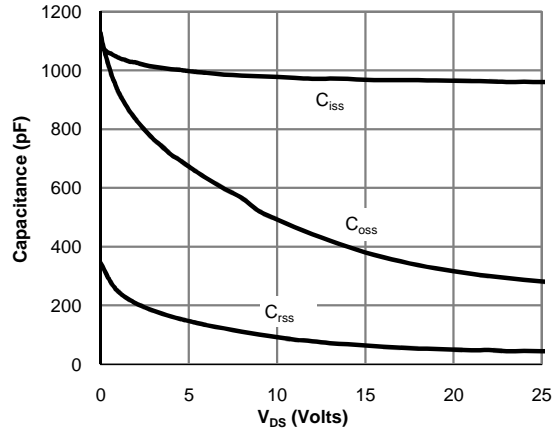


**Figure 6: Body-Diode Characteristics (Note E)**

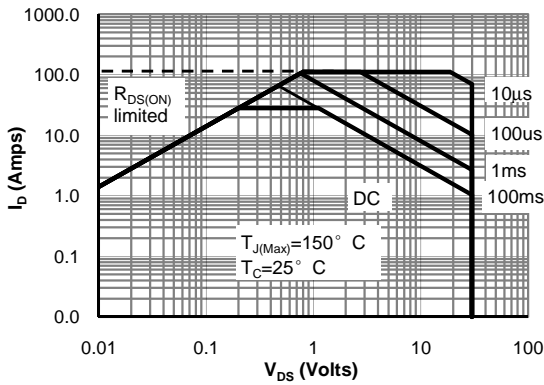
**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



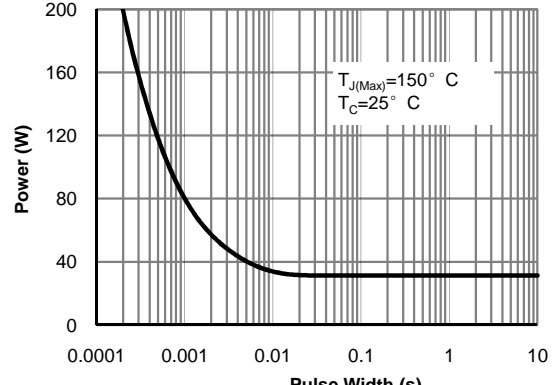
**Figure 7: Gate-Charge Characteristics**



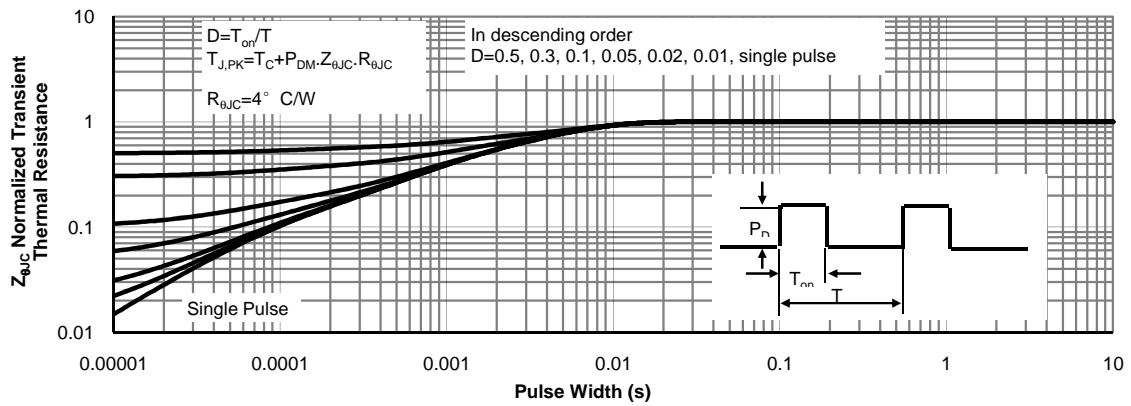
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

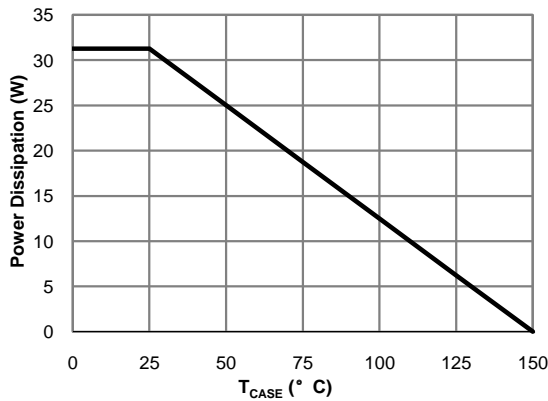


Figure 12: Power De-rating (Note F)

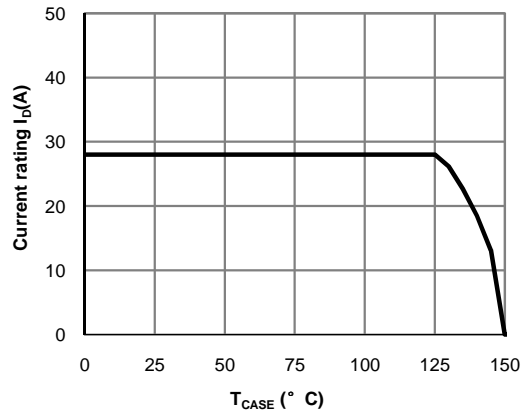


Figure 13: Current De-rating (Note F)

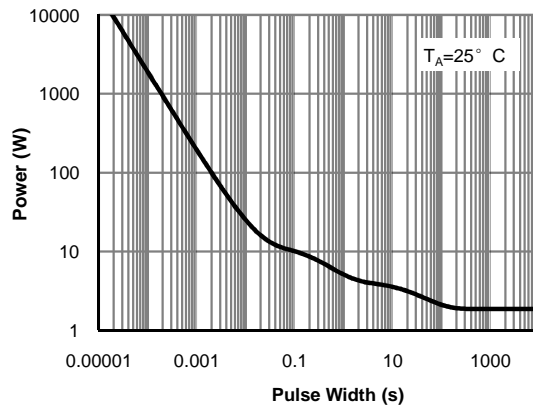


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

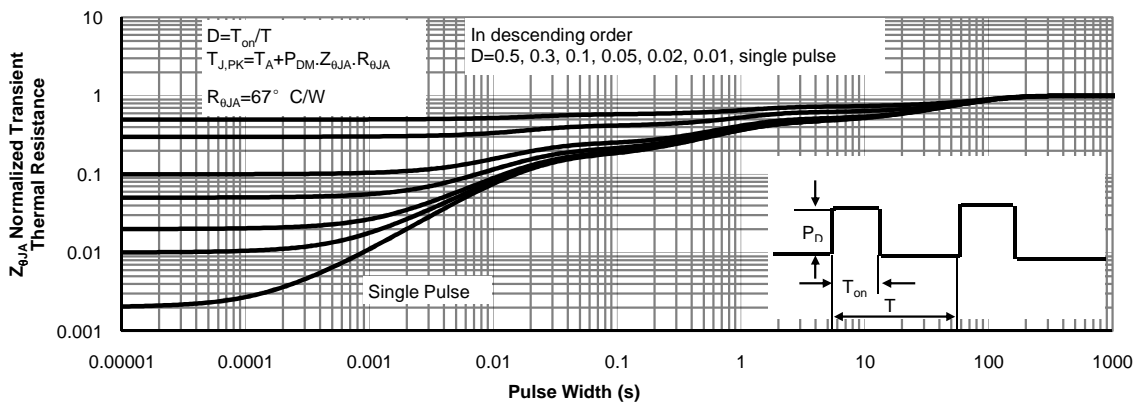


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

**Q2 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.5	2	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		1.7	2.4	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		2.2	3	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		85		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				42	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			3430		pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		1327		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			175		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.3	0.7	1.1	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		53	64	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			25	30	nC
Q <sub>gs</sub>	Gate Source Charge			7.8		nC
Q <sub>gd</sub>	Gate Drain Charge			10.3		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		7.5		ns
t <sub>r</sub>	Turn-On Rise Time			5.0		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			33.8		ns
t <sub>f</sub>	Turn-Off Fall Time			9.8		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		22		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		58		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> =25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

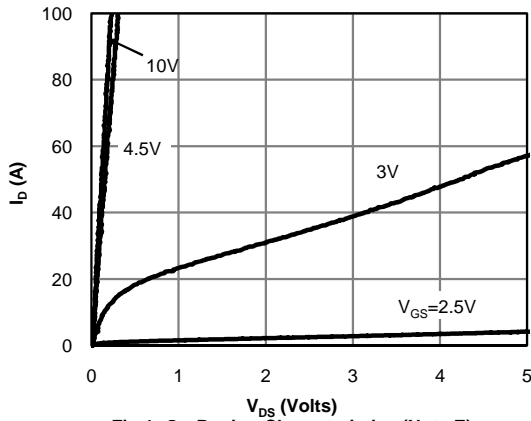
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

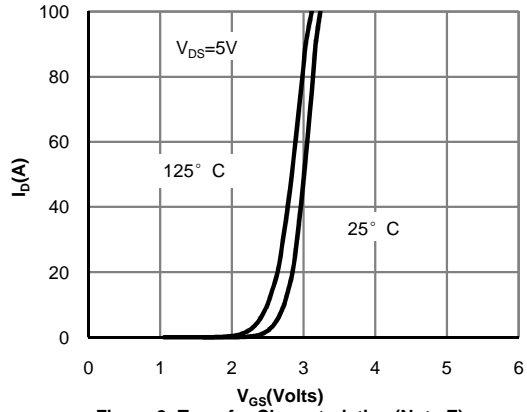
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

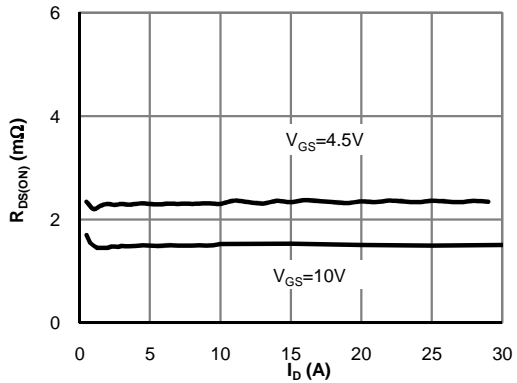
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



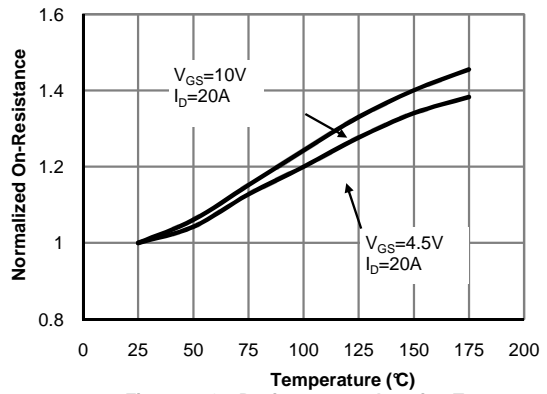
**Fig 1: On-Region Characteristics (Note E)**



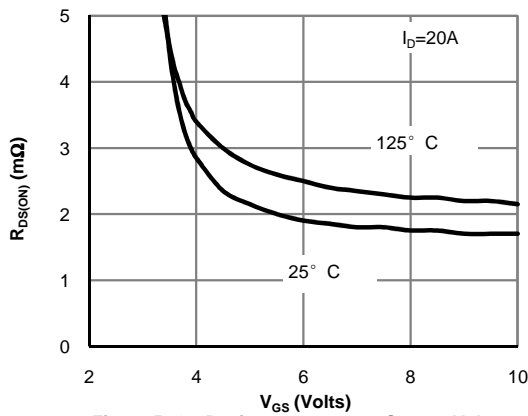
**Figure 2: Transfer Characteristics (Note E)**



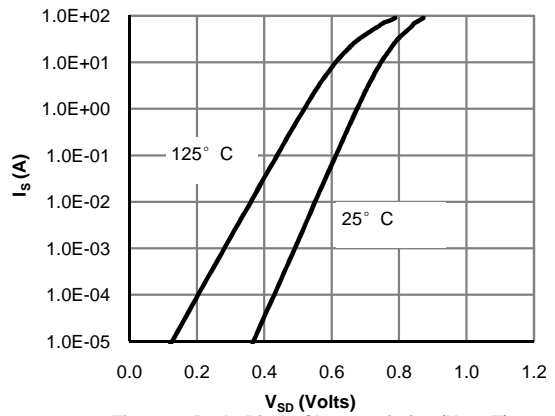
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

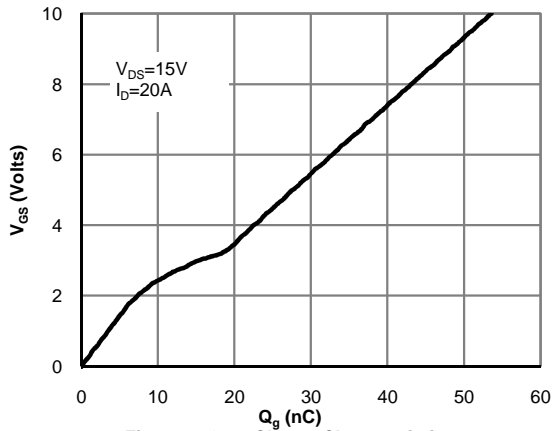


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

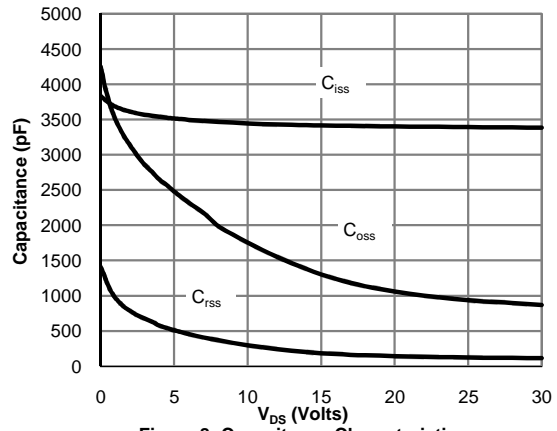


**Figure 6: Body-Diode Characteristics (Note E)**

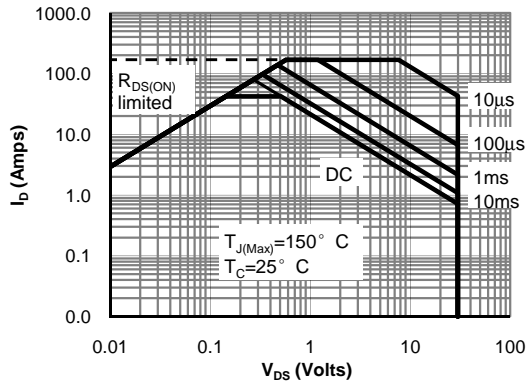
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



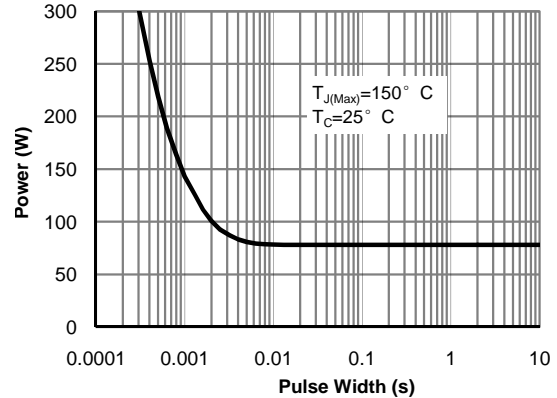
**Figure 7: Gate-Charge Characteristics**



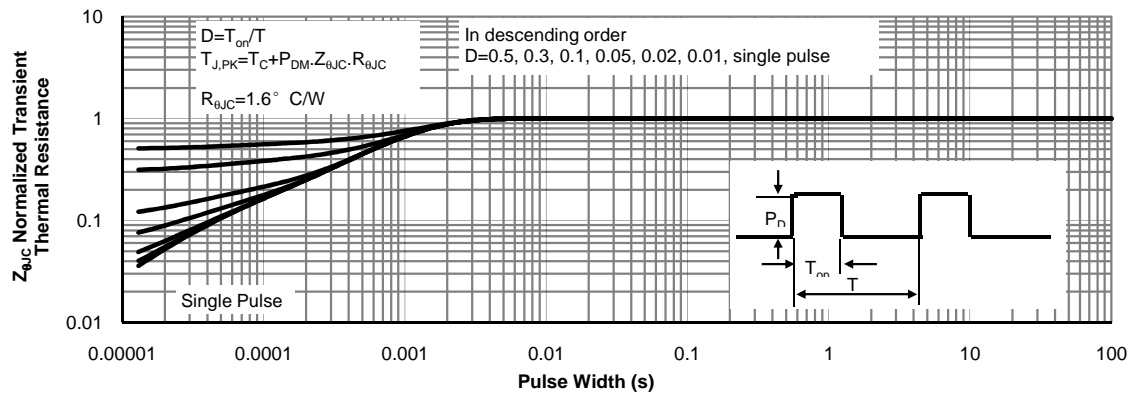
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**



**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

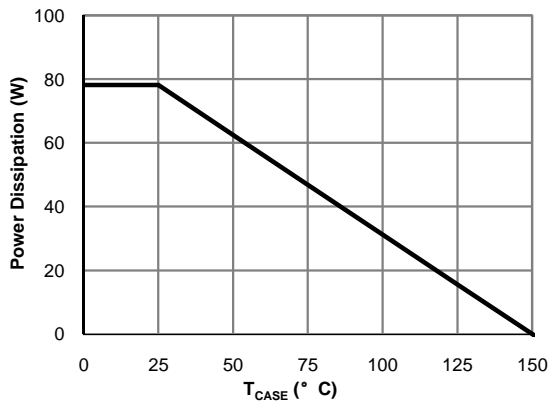


Figure 12: Power De-rating (Note F)

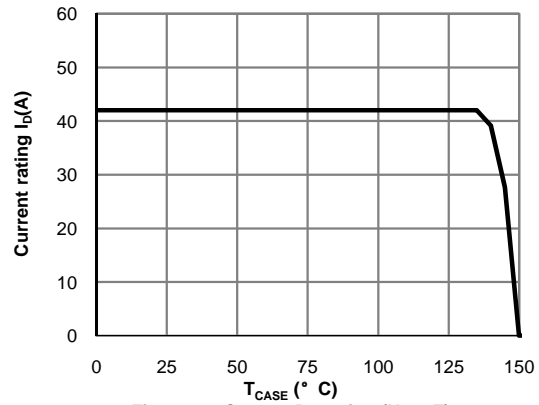


Figure 13: Current De-rating (Note F)

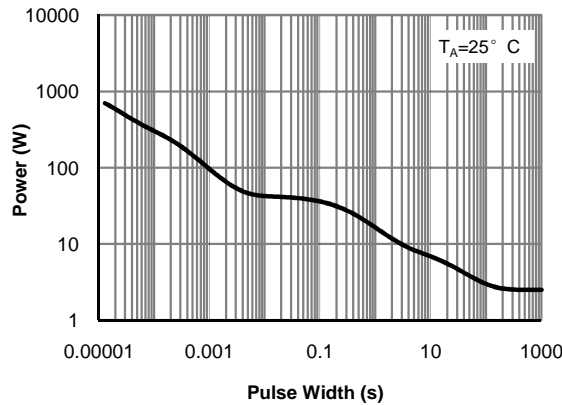


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

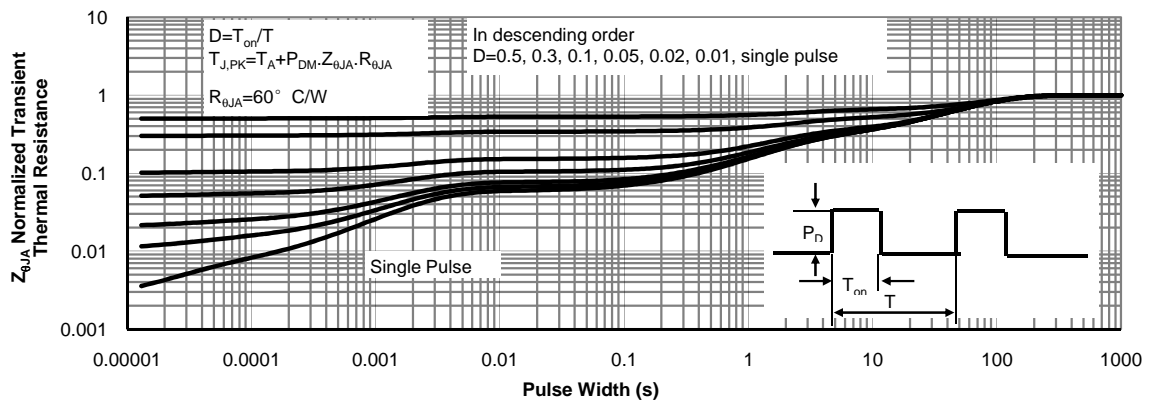
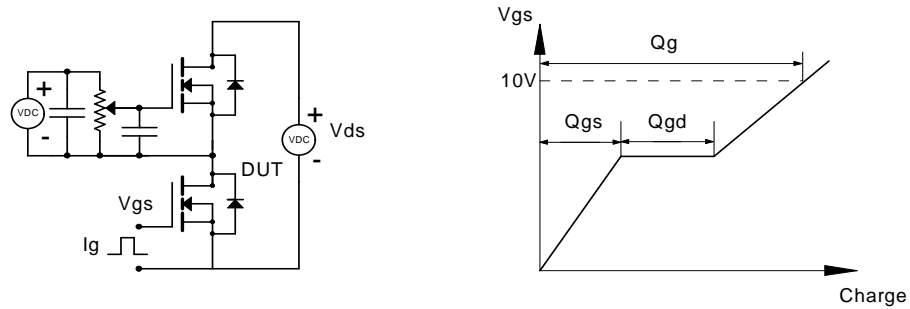
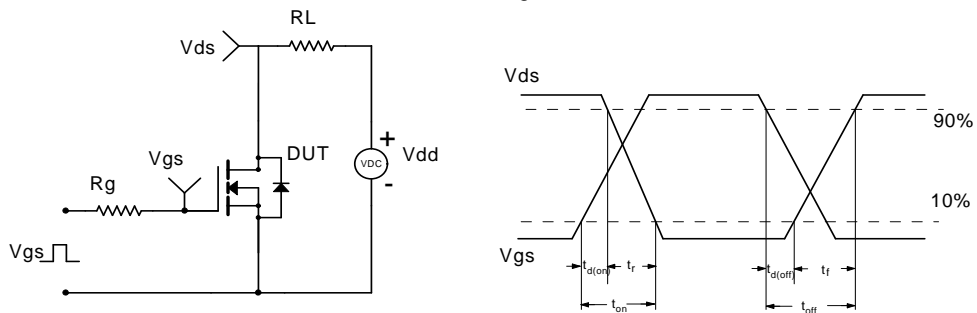


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

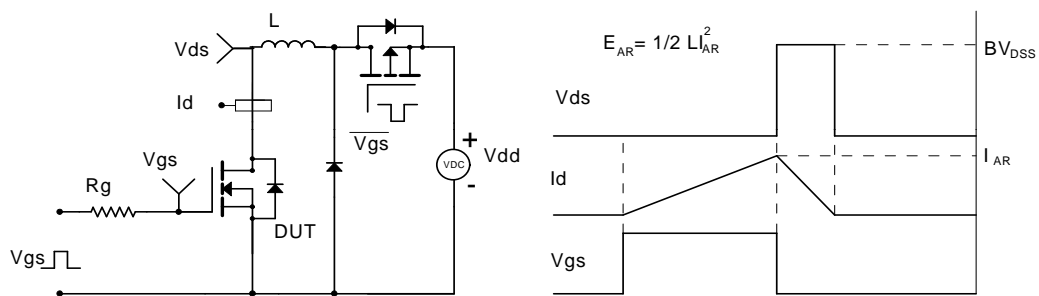
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

