



Plasma Display Modules

128 x 32 Graphics Display with Drive Electronics and TTL Level Data Interface



The APD-128G032 has been designed to offer high brightness and superior viewing aesthetics in a package that is very affordable. This display is ideal for low to medium level information content messages and would be ideal for applications such as arcade games, process control, POS terminals, medical equipment, message centers and ATM machines.

The APD-128G032 DC plasma display offers viewing qualities designers seek such as high contrast, viewing angle of 150° minimum and long distance readability. Its bright (50 foot Lambert minimum) with characters and graphics figures presented in a pleasing neon orange color against a black background. Plasma is much more readable and eyepleasing than liquid crystal or vacuum fluorescent displays and is filterable to red, amber or neutral density.

These plasma display panels are driven in a standard row-column refresh method much like a CRT display. The designer need only supply TTL level signals for SERIAL DATA, DOT CLOCK, COLUMN LATCH, ROW DATA, ROW CLOCK and DISPLAY ENABLE. The SERIAL DATA is entered with the DOT CLOCK up to frequencies as high as 8MHz. After a row of 128 pixels is clocked in, the COLUMN LATCH signal is toggled and the data is latched. At the time the data is latched, the display is briefly disabled using the DISPLAY ENABLE signal, then the row pointer is advanced with the ROW CLOCK signal. Once each frame the ROW DATA must be asserted to synchronize the column serial data with the beginning row. The recommended scanning frequency is approximately 70Hz, but may be as high as 200Hz. The high clock rate on the data clock allows for rapid refresh and maximum access time to the refresh ram.

STANDARD ELECTRICAL SPECIFICATIONS*							
DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNITS		
Logic Supply	Vcc	+ 4.5	+ 5.0	+ 5.5	VDC		
Logic Current	Icc	_	25	100	mADC		
Anode Supply	Vsp	_	+ 75	+ 80	VDC		
Anode Current	Isp	_	200	250	mADC		
(Fully Lit)							
Cathode Supply	Vsn	_	- 110	- 125	VDC		
Cathode Current	Isn	_	200	250	mADC		
(Fully Lit)							
Cathode Control**	Vrw	+ 10.8	+12	+ 15	VDC		
Cathode Control	Irw	_	10	20	mADC		
Current							
Total V _{sp} and V _{sn}	Vtot	170	185	205	VDC		
Logic 1 Input	Vih	2.0	_	_	VDC		
Logic 0 Input	Vil	_	_	0.8	VDC		

^{*}Recommended operating voltages . All maximums are absolute maximum.

FEATURES

- · TTL level video interface
- · Large characters
- · Highly visible for long distance viewing
- > 30:1 contrast ratio
- · Bright and pleasant neon orange color
- · Slim profile
- Very affordable

ELECTRICAL SPECIFICATIONS

Voltage(s) Required: + 75VDC, Vsp. - 110VDC, Vsn.

+ 5VDC, Vcc. + 12VDC (- 98 VDC), Vrw (12VDC to be referenced to - 110VDC.)

Power Required: Typical =12 watts. Maximum = 45 watts

OPTICAL SPECIFICATIONS

Viewing Area: 12.75" [323.8mm] W x 3.15" [80.01mm] L

Character Array: 8 x 8: 16 x 4. 6 x 8: 21 x 4

Character Size: 0.65" [16.51mm] H x 0.45" [11.43mm] W

Pixel Size: 0.050" [1.27mm] Pixel Pitch: 0.100" [2.54mm] Luminance: 50 foot lamberts

Color: Neon Orange

ENVIRONMENTAL SPECIFICATIONS

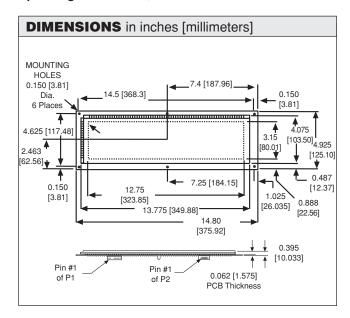
Operating Temperature: 0° C to + 70° C Storage Temperature: - 40° C to + 85° C

Relative Operating Humidity: To 95% non-condensing

Mechanical Shock: 30G

Vibration: 3G

Operating Altitude: 10,000 feet



^{**}Vrw is referenced to Vsn.

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PIN DESCRIPTION						
P1 - POWER CONNECTOR						
AMP #640445-8 or equivalent.						
Mates with AMP 640428-8, MOLEX 09-50-3081 or equivalent.						
PIN	SIGNAL	DESCRIPTION				
1	Vsn	Cathode supply				
2	Vrw		Cathode control			
3	KEY		Used to key connector			
4	GND		Vsn and Vsp			
5	GND	GND				
6	Vcc	V _{cc} Logic supply				
7	NOT USED					
8	Vsp	Anode supply				
P2 - DATA CONNECTOR						
AMP #103309-2 or equivalent. Mates with AMP 746195-2, MOLEX 39-27-1146 or equivalent.						
PIN	DESCRIPTION	PIN	DESCRIPTION			
1	DISPLAY ENABLE	2	GROUND			
3	ROW DATA	4	GROUND			
5	ROW CLOCK	6	GROUND			
7	COLUMN LATCH	8	GROUND			
9	DOT CLOCK	10	GROUND			
11	SERIAL DATA	12	GROUND			
13	No connect	14	GROUND			

INTERFACE SIGNAL DESCRIPTION

DOT CLOCK - This signal enters the SERIAL DATA on each low to high transition. A total of 128 DOT CLOCK transitions must be present for each line of column/anode data.

SERIAL DATA - This signal presents the pixel data in positive logic format. A logic one represents a lit pixel and a logic zero represents an extinguished pixel. Data is entered from right to left. The first pixel data entered will represent the left most pixel in the row.

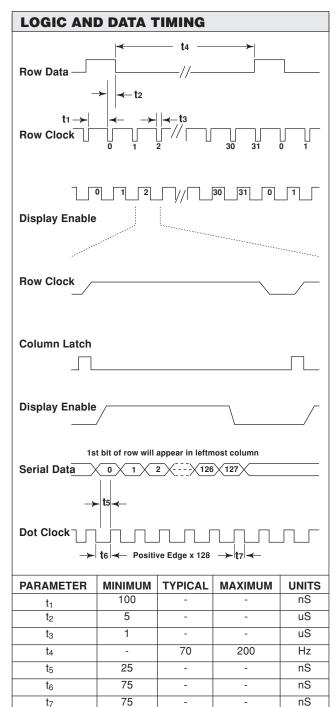
COLUMN LATCH - This signal latches the pixel data into the driver outputs. When the COLUMN LATCH signal goes to logic one the data entered previously will fall through to the driver outputs. When the signal returns to a logic zero the data is latched and the shift register is now ready to accept the next row of data. Must be held low while entering new SERIAL DATA.

DISPLAY ENABLE - This signal enables the output drivers. Using a duty cycle control, this signal may also be used for intensity control. The DISPLAY ENABLE must be at logic zero before the COLUMN LATCH signal transitions. To avoid display blurring, the ROW CLOCK signal should also transition while DISPLAY ENABLE is a logic zero.

ROW DATA - This signal is the first line marker for the scan. This input should be held high to correspond to the first row of pixel data.

ROW CLOCK - This signal clocks ROW DATA on the falling edge. The ROW CLOCK signal is repetitive and must be present for proper scanning of the display module.

The APD-128G032 has an unique input protection circuit that assures the column drivers stay blanked on power up. The protection circuit unblanks the column drivers when the ROW CLOCK signal begins (i.e the display begins scanning.)



ORDERING INFORMATION					
DESCRIPTION	PART NUMBER				
Display, Driver Electronics and TTL Interface APD-128G032					
Data Connector Kit	280105-05				
Power Connector Kit	280108-12				
DC/DC Converter Assembly	280961-03				



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