ACPL-335J

2.5 Amp MOSFET Gate Drive Optocoupler with Integrated Desat Over Current Sensing, Active Miller Current Clamping, FAULT and UVLO Status Feedback

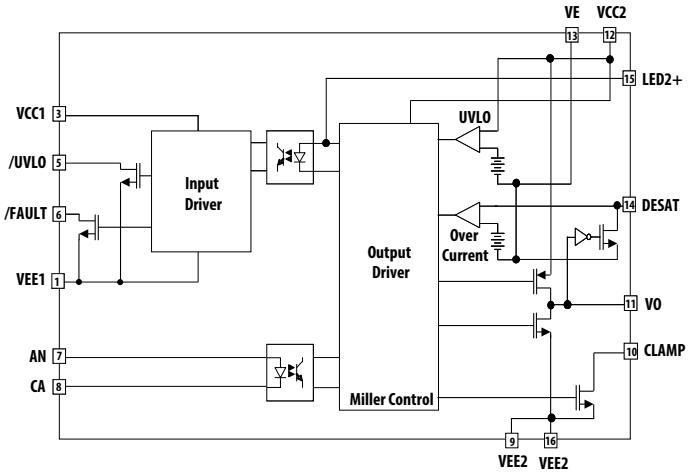
Data Sheet

Description

The Avago ACPL-335J is a 2.5A smart gate drive optocoupler device featuring fast propagation delay with excellent timing skew performance. The device supports a full set of fail-safe MOSFET diagnostics, protection and fault reporting. This full-featured and easy-to-implement gate drive optocoupler comes in a compact, surface-mountable SO-16 package.

The ACPL-335J is designed for driving power MOSFETs used in DC-DC converter, switching power supplies and battery chargers, and provides the reinforced insulation and reliability needed for critical high voltage industrial applications.

Functional Diagram



Features

- Peak output current: 2.5 A max.
- Miller Clamp Sinking Current: 1.9 A max.
- Wide Operating Voltage: 12V to 20V
- Propagation delay: 250 ns max.
- Dead Time Distortion: -100 ns to +20 ns
- Integrated fail-safe MOSFET protection
- Desat over current sensing, turn-off protection and Fault Feedback
- Under Voltage Lock-Out protection (UVLO) with Feedback
- SO-16 package with 8mm clearance and creepage
- Temperature range: -40°C to +105°C
- Common Mode Rejection (CMR): >50kV/µs at V_{CM} = 1500 V
- High Noise Immunity
  - Miller Current Clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative Gate Bias
- Regulatory approvals:
  - UL1577, CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

- Isolated MOSFET gate drive
- DC-DC Converter
- Switching Power Supplies
- Battery Charging

CAUTION *It s advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.*

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-335J	-000E	SO-16	X		X	45 per tube
ACPL-335J	-500E		X	X	X	850 per reel

To order, choose a part number from the Part Number column and combine with the desired option from the RoHS Complaint column to form an order entry.

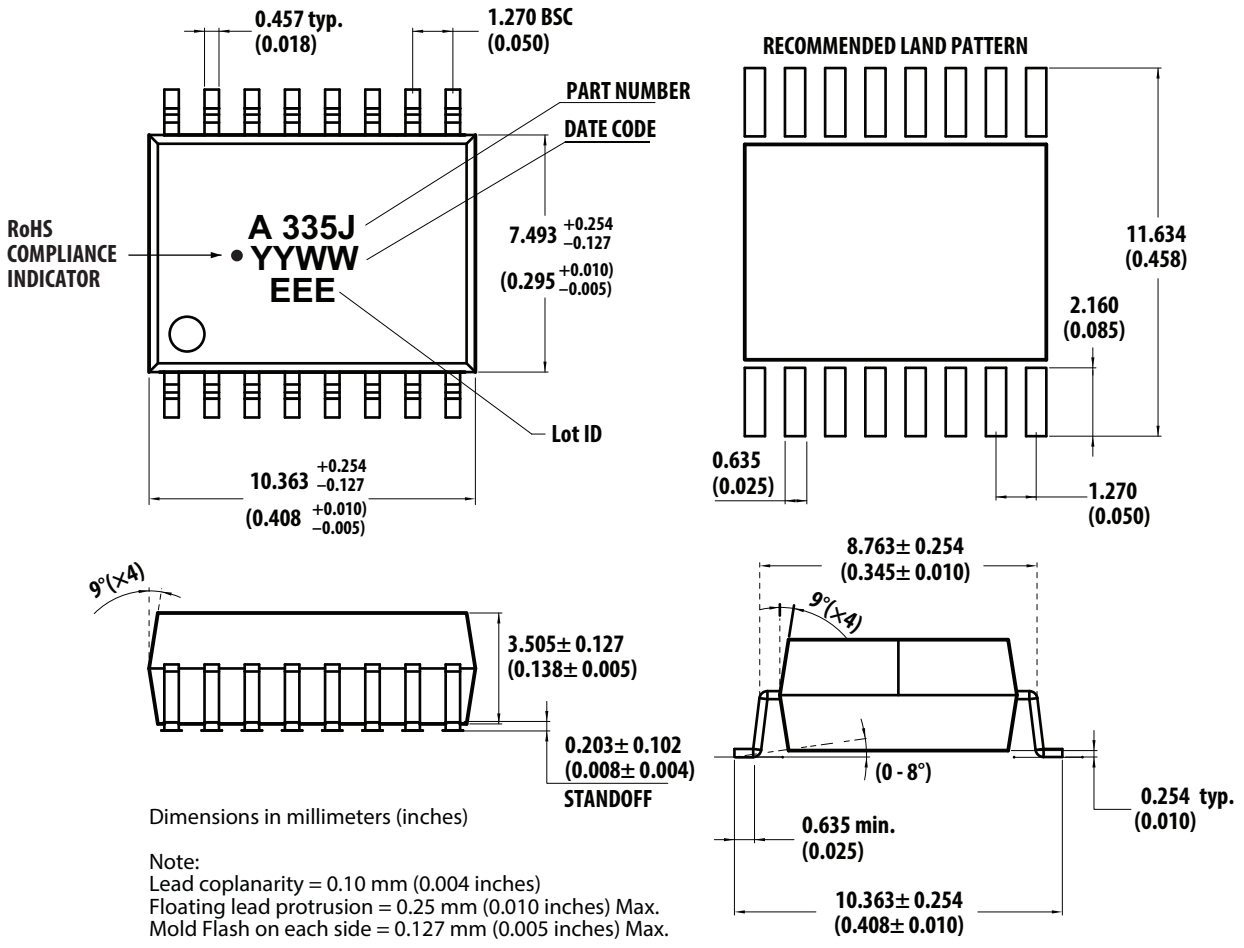
Example 1:

ACPL-335J-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

16-Lead Surface Mount



Dimensions in millimeters (inches)

Note:
Lead coplanarity = 0.10 mm (0.004 inches)
Floating lead protrusion = 0.25 mm (0.010 inches) Max.
Mold Flash on each side = 0.127 mm (0.005 inches) Max.

Recommended Lead-free IR Profile

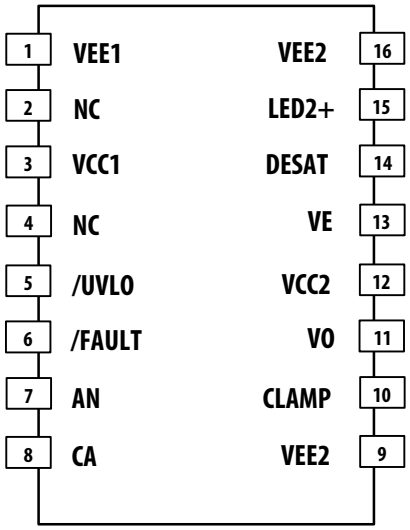
Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Non-halide flux should be used.

Product Overview Description

The ACPL-335J (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated MOSFET gate drive circuit. It features desaturation sensing with shutdown protection and fault feedback, under voltage lock-out and feedback and active Miller current clamping in a SO-16 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increased its noise immunity.

Package Pin Out



Pin Description

Pin Name	Function	Pin Name	Function
VEE1	Input common	VEE2	Negative power supply
NC	No connection	LED2+	No connection, for testing only
VCC1	Input power supply	DESAT	Desat over current sensing
NC	No connection	VE	MOSFET Source reference
/UVLO	VCC2 under voltage lock-out feedback	VCC2	Positive power supply
/FAULT	Over current fault feedback	VO	Driver output to MOSFET gate
AN	Input LED anode	CLAMP	Miller current clamping output
CA	Input LED cathode	VEE2	Negative power supply

Regulatory Information

The ACPL-335J is approved by the following organizations:

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}
CSA	Approved under CSA Component Acceptance Notice #5, File CA 88324.
IEC/EN/DIN EN 60747-5-5	Approved under IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150Vrms for rated mains voltage ≤ 300Vrms for rated mains voltage ≤ 600Vrms for rated mains voltage ≤ 1000Vrms		 I – IV I – IV I – IV I – III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1sec, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Power Output Power	 T_S $P_{S,INPUT}$ $P_{S,OUTPUT}$	 175 400 1200	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	> 10^9	Ohm

Notes:
Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Avago Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
IC Junction Temperature	T_J		125	°C	1
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Transient Input Current (<1us pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		6	V	
/Fault Output Current (Sinking)	$I_{/FAULT}$		10	mA	
/Fault Pin Voltage	$V_{/FAULT}$	-0.5	6	V	
/UVLO Output Current (Sinking)	$I_{/UVLO}$		10	mA	
/UVLO Pin Voltage	$V_{/UVLO}$	-0.5	6	V	
Positive Input Supply Voltage	V_{CC1}	-0.5	26	V	
Total Output Supply Voltage	V_{CC2}	-0.5	30	V	
Negative Output Supply Voltage	$V_{EE2} - V_E$	-10	0.5	V	2
Positive Output Supply Voltage	$V_{CC2} - V_E$	-0.5	30	V	
Gate Drive Output Voltage	$V_{O(peak)}$	-0.5	V_{CC2}+0.5	V	
Peak Output Current	$\|I_{O(peak)}\|$		2.5	A	3
Peak Clamping Sinking Current	I_{CLAMP}		2	A	3
Miller Clamping Pin Voltage	$V_{CLAMP} - V_{EE2}$	-0.5	V_{CC2}+0.5	V	
Desat Voltage	$V_{DESAT} - V_E$	V_E - 0.5	V_{CC2}+0.5	V	4
Desat Discharging Current (Continuous)	I_{DSCHG}		5	mA	
Output IC Power Dissipation	P_O		580	mW	1
Input IC Power Dissipation	PI		150	mW	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	-40	105	°C	
Input Supply Voltage	V_{CC1} - V_{EE1}	8	18	V	
Total Output Supply Voltage	V_{CC2} - V_{EE2}	12	20	V	5
Negative Output Supply Voltage	V_{EE2} - V_E	-8	0	V	3
Positive Output Supply Voltage	V_{CC2} - V_E	12	20	V	
Input LED Current	$I_{F(ON)}$	10	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-5.5	0.8	V	
Input pulse width	$t_{ON(LED)}$	500		ns	

Electrical and Switching Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions. All typical values at T_A = 25°C, V_{CC1} = 12 V, V_{CC2}-V_{EE2}=13V, V_E-V_{EE2}=0V. All voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
IC Supply Current								
Input Supply Current	I_{CCI}		3.7	6.0	mA		3	
Output Low Supply Current	I_{CC2L}		10.5	13.2	mA	I_F=0mA	4	
Output High Supply Current	I_{CC2H}		10.6	13.6	mA	I_F=10mA	4	
Logic Input and Output								
LED Forward Voltage	V_F	1.25	1.55	1.85	V	I_F=10mA	5	
LED Reverse Breakdown Voltage	V_{BR}	6			V	I_F= -10µA		
Input Capacitance	C_{IN}		90		pF			
LED Turn on Current Threshold Low to High	I_{TH+}		2.7	6.6	mA	V_O=5V	6	
LED Turn on Current Threshold High to Low	I_{TH-}		2.1	6.4	mA	V_O=5V	6	
LED Turn on Current Hysteresis	I_{TH_HYS}		0.6		mA			
/FAULT Logic Low Output Current	I_{FAULT_L}	4.0	9.0		mA	$V_{/FAULT}$ = 0.4V		
/FAULT Logic High Output Current	I_{FAULT_H}			20	µA	$V_{/FAULT}$ = 5V		
/UVLO Logic Low Output Current	I_{UVLO_L}	4.0	9.0		mA	$V_{/UVLO}$ = 0.4V		
/UVLO Logic High Output Current	I_{UVLO_H}			20	µA	$V_{/UVLO}$ = 5V		
Gate Driver								
High Level Output Current	I_{OH}		-2.0	-0.75	A	V_O = V_{CC2}-3V	7	4
Low Level Output Current	I_{OL}	1.0	2.2		A	V_O = V_{EE2}+2.5V	8	4
High Level Output Voltage	V_{OH}	V_{CC2}–0.5	V_{CC2}–0.2		V	I_O = -100 mA		6 – 8
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA		

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
VIN to High Level Output Propagation Delay Time	t_{PLH}	50	110	250	ns	Vsource = 3.3V Rf = 140 Ω, Rg = 10 Ω Cload = 1 nF f = 200 kHz Duty Cycle = 50%	9, 12	9
VIN to Low Level Output Propagation Delay Time	t_{PHL}	50	150	250	ns			10
Pulse Width Distortion (t_{PHL}-t_{PLH})	PWD	-20		100	ns			11,12
Dead Time Distortion (t_{PLH}-t_{PHL})	DTD	-100		20	ns			12,13
10% to 90% Rise Time	t_R		60		ns			
90% to 10% Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50	>70		kV/µs	T_A=25°C, V_{CM} =1500V, V_{CC2} =20V	13	14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50	>70		kV/µs	T_A = 25°C, V_{CM}=1500V V_{CC2} =20V	14	15
Active Miller Clamp								
Clamp Threshold Voltage	V_{TH_CLAMP}		2.0	3.0	V			
Clamp Low Level Sinking Current	I_{CLAMP}	0.75	1.9		A	V_{CLAMP} = V_{EE2} +2.5 V		
V_{CC2} UVLO Protection (UVLO voltage V_{UVLO} reference to V_E)								
V_{CC2} UVLO Threshold Low to High	V_{UVLO+}	8.8	10	11.2	V	V_O > 5 V		8, 16
V_{CC2} UVLO Threshold High to Low	V_{UVLO-}	7.8	9	10.2	V	V_O < 5 V		8, 17
V_{CC2} UVLO Hysteresis	V_{UVLO_HYS}		1		V			
V_{CC2} to UVLO High Delay	t_{PLH_UVLO}		10		µs			18
V_{CC2} to UVLO Low Delay	t_{PHL_UVLO}		10		µs			19
V_{CC2} UVLO to V_{OUT} High Delay	t_{UVLO_ON}		10		µs			20
V_{CC2} UVLO to V_{OUT} Low Delay	t_{UVLO_OFF}		10		µs			21
V_{CC2} UVLO Threshold Low to High	V_{UVLO+}	8.8	10	11.2	V	V_O > 5 V		8, 16
Desaturation Protection (Desat voltage V_{DESAT} reference to V_E)								
Desat Sensing Threshold	V_{DESAT}	3.4	3.9	4.4	V		10	8
Desat Discharging Current (Pulsed)	I_{DSCHG}	20	53		mA	V_{DESAT} = 5V	11	
Internal Desat Blanking Time	$t_{DESAT(BLANKING)}$	0.2	0.4	0.6	µs	Cload =1 nF	6	22
Desat Sense to 90% VO Delay	$t_{DESAT(90\%)}$		0.15	0.5	µs		6	23
Desat to Low Level FAULT Signal Delay	$t_{DESAT(/FAULT)}$			7	µs		6	24
Output Mute Time due to Desat	$t_{DESAT(MUTE)}$	2.3	3.2	5	ms		6	25
Time for Input Kept Low Before Fault Reset to High	$t_{DESAT(RESET)}$	2.3	3.2	5	ms		6	26

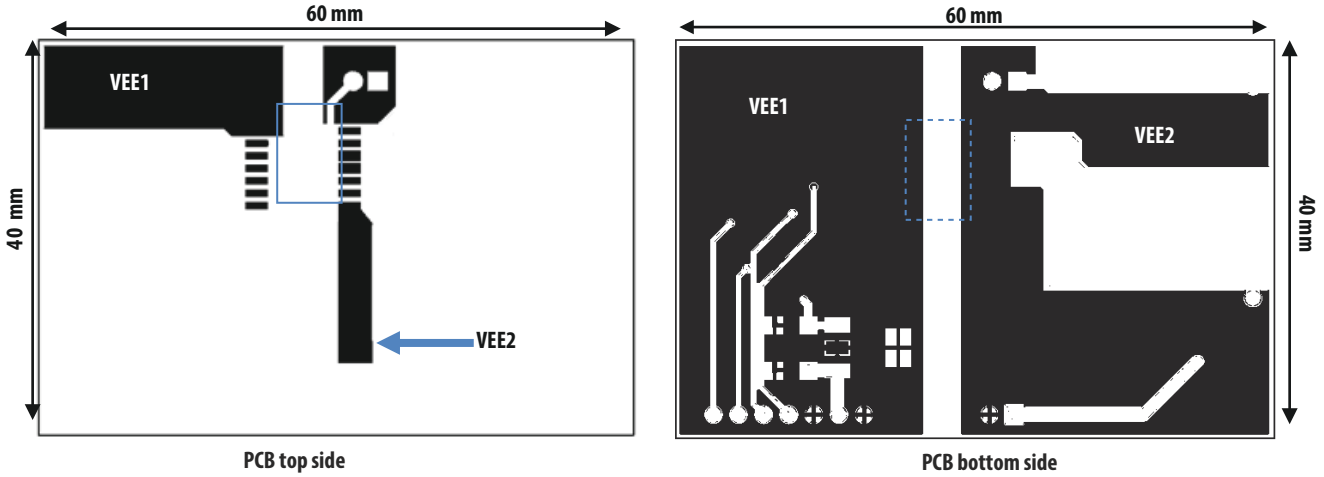
Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min. T_A = 25°C	27, 28, 29
Resistance (Input-Output)	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V_{DC}	29
Capacitance (Input-Output)	C_{I-O}		1.3		pF	f = 1 MHz	
Thermal coefficient between LED and input IC	A_{EI}		35.4		°C/W		
Thermal coefficient between LED and output IC	A_{EO}		33.1		°C/W		
Thermal coefficient between input IC and output IC	A_{IO}		25.6		°C/W		
Thermal coefficient between LED and Ambient	A_{EA}		176.1		°C/W		
Thermal coefficient between input IC and Ambient	A_{IA}		92		°C/W		
Thermal coefficient between output IC and Ambient	A_{OA}		76.7		°C/W		

Notes:
1. Output IC power dissipation is derated linearly above 95 °C from 580 mW to 380 mW at 105 °C based on the thermal characteristic on page 11.
2. This supply is optional. Required only when negative gate drive is implemented.
3. Maximum pulse width = 1 µs, maximum duty cycle = 1%.
4. Maximum 500 ns pulse width if peak V_{DESAT} > 10 V.
5. 12 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 11.2 V.
6. For High Level Output Voltage testing, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero.
7. Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.
8. Once V_O of the ACPL-335J is allowed to go high (V_{CC2} - V_E > V_{UVLO}), the DESAT detection feature of the ACPL-335J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{CC2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the DESAT detection and UVLO features of the ACPL-335J work in conjunction to ensure constant IGBT protection.
9. t_{PLH} is defined as propagation delay from 50% of LED input I_F to 50% of High level output.
10. t_{PHL} is defined as propagation delay from 50% of LED input I_F to 50% of Low level output.
11. Pulse Width Distortion (PWD) is defined as (t_{PHL} – t_{PLH}) of any given unit.
12. As measured from I_F to V_O.
13. Dead Time Distortion (DTD) is defined as (t_{PLH} - t_{PHL}) between any two ACPL-335J parts under the same test conditions.
14. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 12 V).
15. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V).
16. This is the “increasing” (i.e., turn-on or “positive going” direction) of V_{CC2} - V_E.
17. This is the “decreasing” (i.e., turn-off or “negative going” direction) of V_{CC2} - V_E.
18. The delay time when V_{CC2} exceeds UVLO+ threshold to UVLO High – 50% of UVLO positive-going edge.
19. The delay time when V_{CC2} falls below UVLO- threshold to UVLO Low – 50% of UVLO negative-going edge.
20. The delay time when V_{CC2} exceeds UVLO+ threshold to 50% of High level output.
21. The delay time when V_{CC2} falls below UVLO- threshold to 50% of Low level output.
22. The delay time for ACPL-335J to respond to a DESAT fault condition without any external DESAT capacitor.
23. The amount of time from when DESAT threshold is exceeded to 90% of VGATE at mentioned test conditions.
24. The amount of time from when DESAT threshold is exceeded to FAULT output Low – 50% of V_{CC1} voltage.
25. The amount of time when DESAT threshold is exceeded, Output is mute to LED input.
26. The amount of time when DESAT Mute time is expired, LED input must be kept Low for Fault status to return to High.
27. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.
28. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.
29. Device considered a two terminal device: pins 1 - 8 shorted together and pins 9 - 16 shorted together.

Thermal Characteristics

Thermal Characteristics are based on the ground planes layout of the evaluation PCB.



Notes on Thermal Calculation

Application and environmental design for ACPL-335J needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 125°C. The following equations calculate the maximum power dissipation and corresponding effect on junction temperatures and can only be used as a reference for thermal performance comparison under specified PCB layout as shown above. The thermal resistance model shown here is not meant to and will not predict the performance of a package in an application-specific environment.

LED Junction Temperature = $A_{EA}*P_E + A_{EI}*P_I + A_{EO}*P_O + T_A$
Input IC Junction Temperature = $A_{EI}*P_E + A_{IA}*P_I + A_{IO}*P_O + T_A$
Output IC Junction Temperature = $A_{EO}*P_E + A_{IO}*P_I + A_{OA}*P_O + T_A$

P_E - LED Power Dissipation
P_I - Input IC Power Dissipation
P_O - Output IC Power Dissipation

Calculation of LED Power Dissipation

LED Power Dissipation, $P_E = I_{F(LED)}$ (Recommended Max) * $V_{F(LED)}$ * Duty Cycle
Example: P_E = 16mA * 1.25 * 50% duty cycle = 10mW

Calculation of Input IC Power Dissipation

Input IC Power Dissipation, $P_I = I_{CC1}$ (Max) * V_{CC1} (Recommended Max)
Example: P_I = 6mA * 18V = 108mW

Calculation of Output IC Power Dissipation

Output IC Power Dissipation, $P_O = V_{CC2}$ (Recommended Max) * I_{CC2} (Max) + P_{HS} + P_{LS}

P_{HS} - High Side Switching Power Dissipation
P_{LS} - Low Side Switching Power Dissipation

$P_{HS} = (V_{CC2} * Q_G * f_{PWM}) * R_{OH(MAX)} / (R_{OH(MAX)} + R_{GH}) / 2$
$P_{LS} = (V_{CC2} * Q_G * f_{PWM}) * R_{OL(MAX)} / (R_{OL(MAX)} + R_{GL}) / 2$

Q_G - Gate Charge at Supply Voltage
f_{PWM} - LED Switching Frequency
$R_{OH(MAX)}$ - Maximum High Side Output Impedance - $V_{OH(MIN)} / I_{OH(MIN)}$
R_{GH} - Gate Charging Resistance
$R_{OL(MAX)}$ - Maximum Low Side Output Impedance - $V_{OL(MIN)} / I_{OL(MIN)}$
R_{GL} - Gate Discharging Resistance

Example:
$R_{OH(MAX)} = (V_{CC2} - V_{OH(MIN)}) / I_{OH(MIN)} = 3\ V / 0.75\ A = 4\ \Omega$
$R_{OL(MAX)} = V_{OL(MIN)} / I_{OL(MIN)} = 2.5\ V / 1\ A = 2.5\ \Omega$
$P_{HS} = (20\ V * 100nC * 200\ kHz) * 4\ \Omega / (4\ \Omega + 10\ \Omega) / 2 = 57.14\ mW$
$P_{LS} = (20\ V * 100nC * 200\ kHz) * 2.5\ \Omega / (2.5\ \Omega + 10\Omega) / 2 = 40\ mW$
$P_O = 20\ V * 13.6\ mA + 57.14\ mW + 40\ mW = 360.14\ mW$

Calculation of Junction Temperature

LED Junction Temperature = 176.1 °C/W *10 mW + 35.4 °C/W *108 mW + 33.1 * 360.14 mW + T_A = 17.5°C + T_A
Input IC Junction Temperature = 35.4 °C/W * 10 mW + 92 °C/W *108 mW + 25.6 * 360.14 mW + T_A = 19.5°C + T_A
Output IC Junction Temperature = 33.1 °C/W * 10 mW + 25.6 °C/W *108 mW + 76.7 * 360.14 mW + T_A = 30.7°C + T_A

Typical Performance Plots

Figure 1 I_{CC1} across temperature

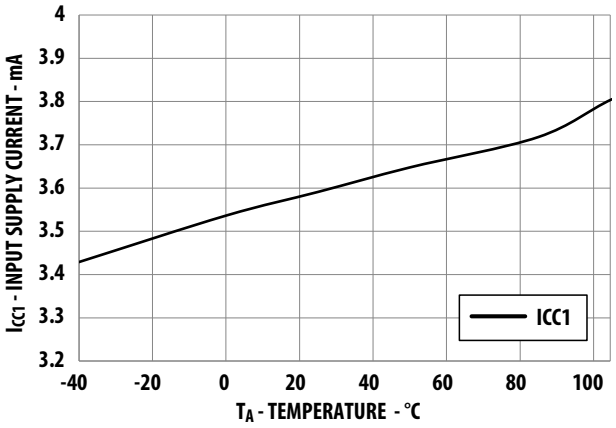


Figure 2 I_{CC2} across temperature

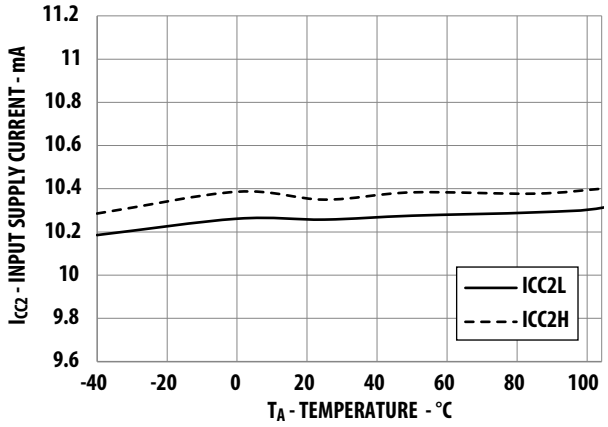


Figure 3 I_F vs V_F

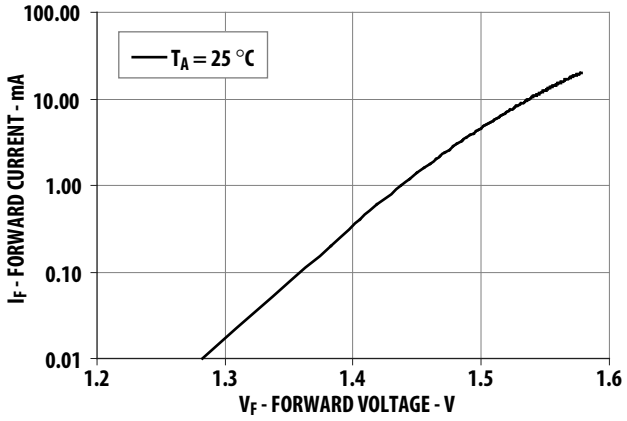


Figure 4 I_{TH} across temperature

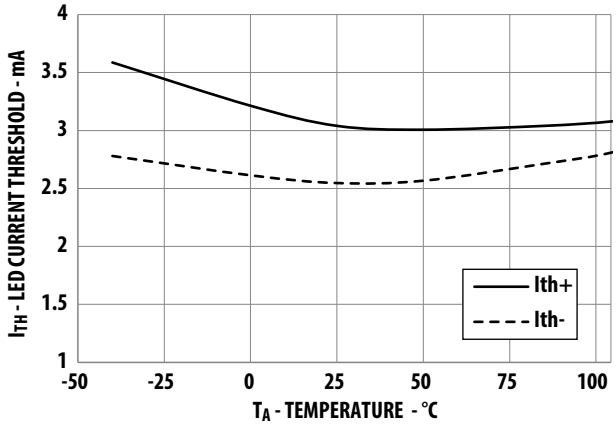


Figure 5 V_{OH} vs I_{OH}

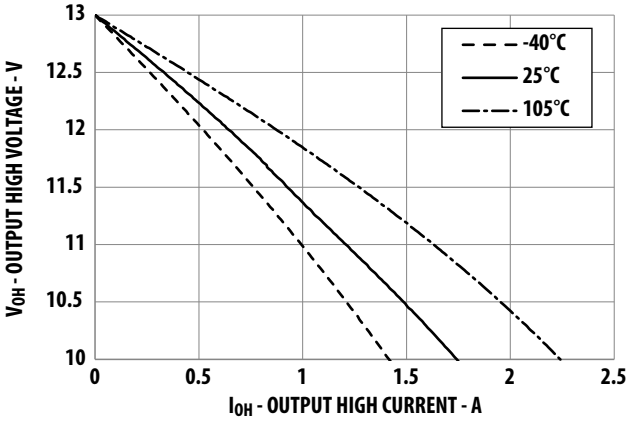


Figure 6 V_{OL} vs I_{OL}

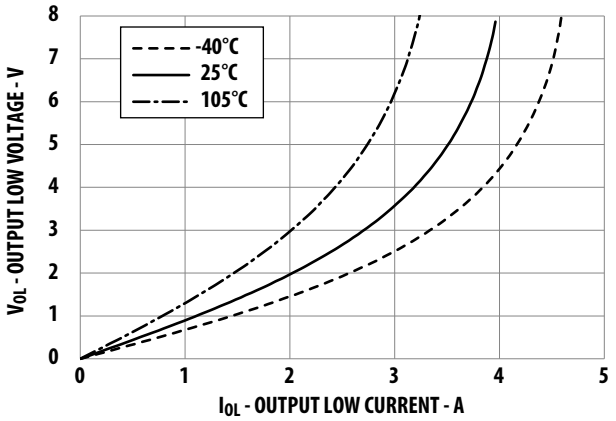


Figure 7 T_P across temperature

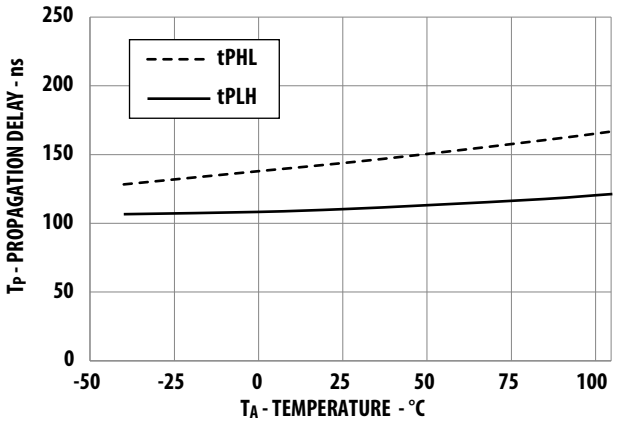


Figure 8 V_{DESAT} Threshold across temperature

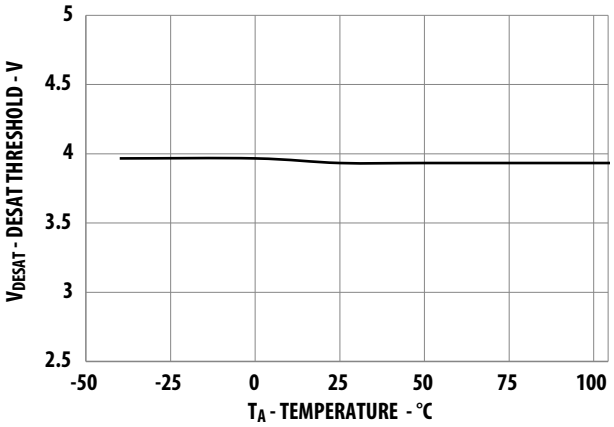


Figure 9 I_{DSCHG} across temperature

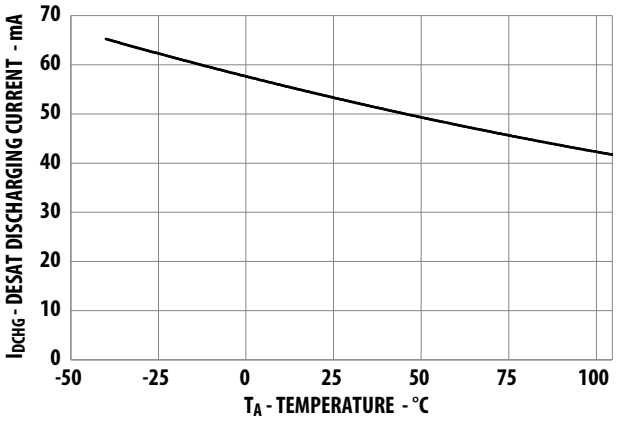


Figure 10 Propagation Delay Test Circuit and Timing Diagram

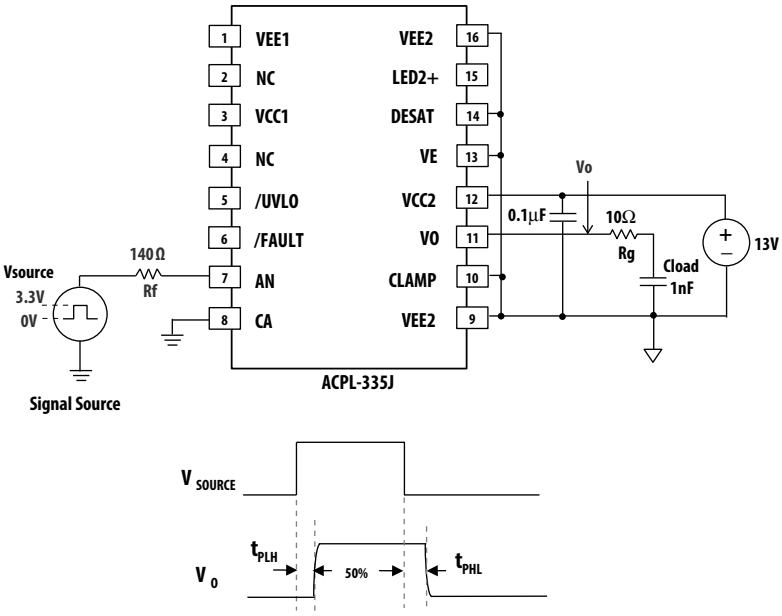


Figure 11 CMR Vo High Test Circuit

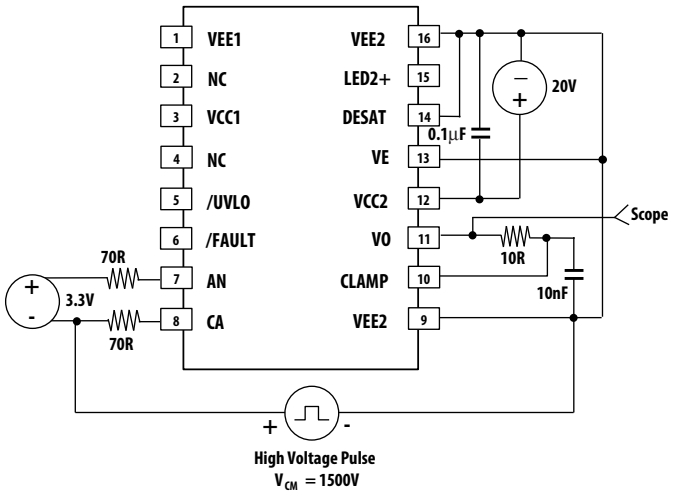
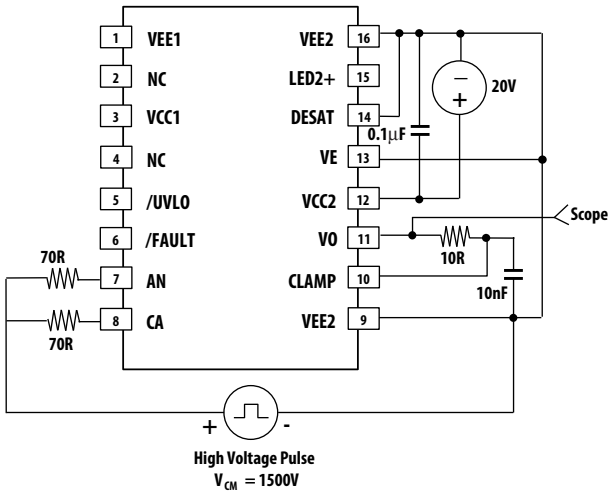


Figure 12 CMR Vo Low Test Circuit



Typical Application/Operation

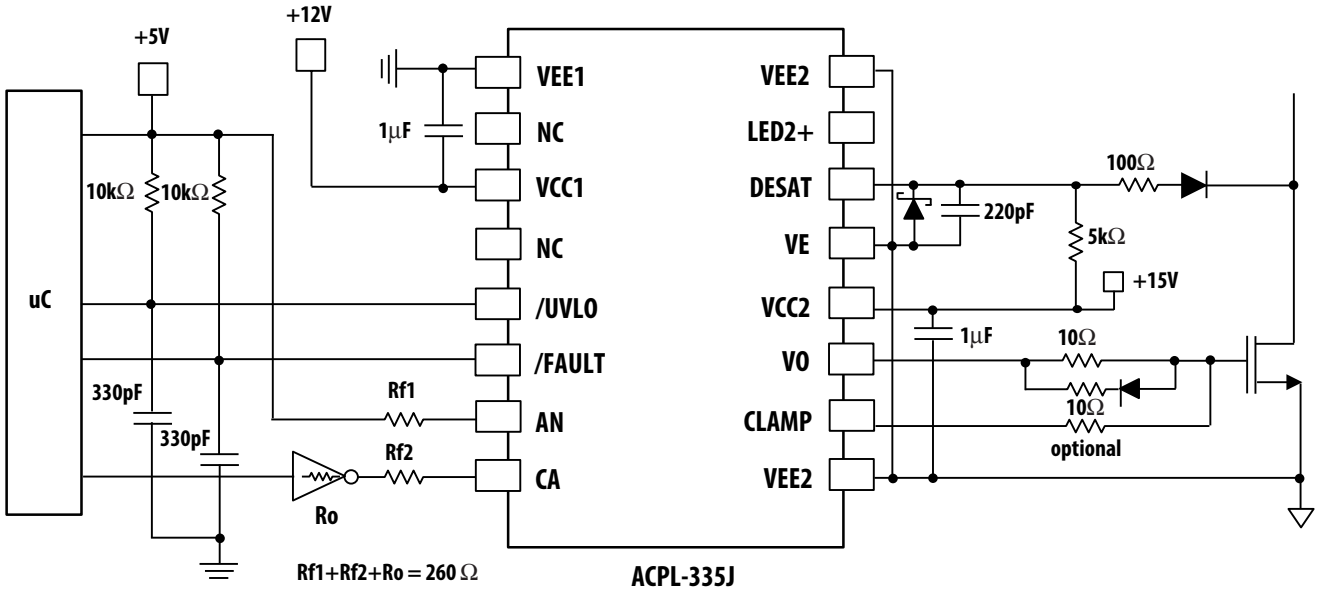
Recommended Application Circuit

The ACPL-335J has non-inverting gate control inputs and an open collector fault and UVLO outputs suitable for wired 'OR' applications.

The recommended application circuit shown in Figure 13 illustrates a typical gate drive implementation using the ACPL-335J.

The two supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. The Desat diode and 220 pF blanking capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10 Ω) serves to limit gate charge current and indirectly control the MOSFET Drain voltage rise and fall times. The open collector fault and UVLO outputs have a passive 10 kΩ pull-up resistor and a 330 pF filtering capacitor.

Figure 13 Recommended gate drive circuit with Desat current sensing using ACPL-335J



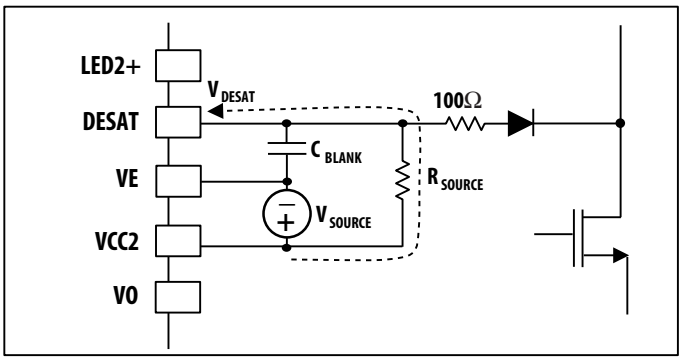
Desat Fault Detection Blanking Time

The Desat fault detection circuitry must be remain disabled for a short time period following the turn-on of the MOSFET to allow the drain voltage to fall below the Desat threshold. This time period, called the Desat blanking time, is controlled by both the internal Desat blanking time and external blanking time. The external blanking time is determined by external RC charging time and the Desat voltage threshold.

The total blanking time is calculated in terms of internal blanking time ($t_{DESAT(BLANKING)}$) and external RC charging time contributed by external resistor (R_{SOURCE}), external capacitor (C_{BLANK}), external charging source (V_{SOURCE}) and Desat sensing threshold (VDESAT). Figure 14 illustrates the external RC charging circuit.

$$t_{BLANK} = t_{DESAT(BLANKING)} - R_{SOURCE}\, C_{BLANK}\, ln\,(1 - \frac{V_{DESAT}}{V_{SOURCE}})$$

Figure 14 External RC charging circuit



Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of ACPL-335J is capable of delivering 2.5A sourcing current to drive the MOSFET's gate. While LED is switched off the gate driver can provide 2.5A sinking current to switch the gate off fast. Additional miller clamping pull-down transistor is activated when output voltage reaches about 2V with respect to V_{EE2} to provide low impedance path to miller current as shown in Figure 15.

Figure 15 Gate drive signal behavior

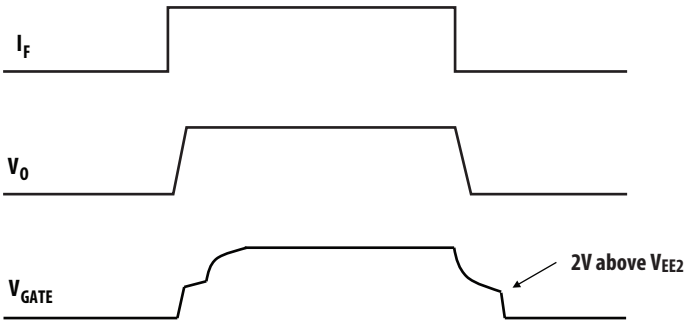
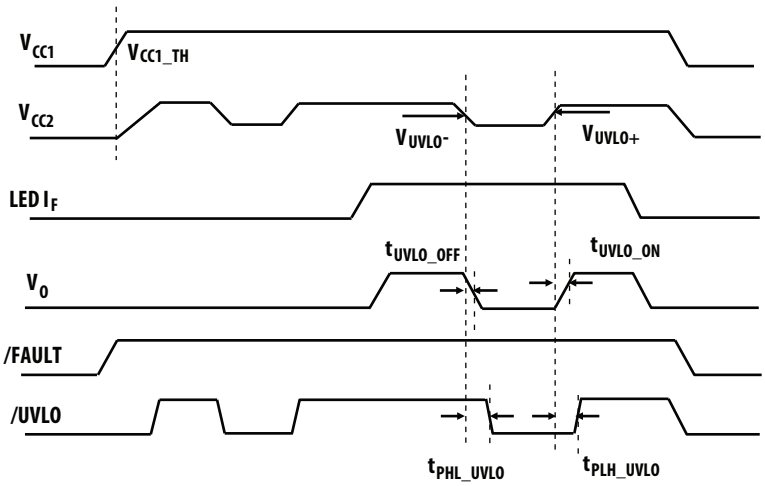


Figure 16 Circuit behaviors at power up and power down



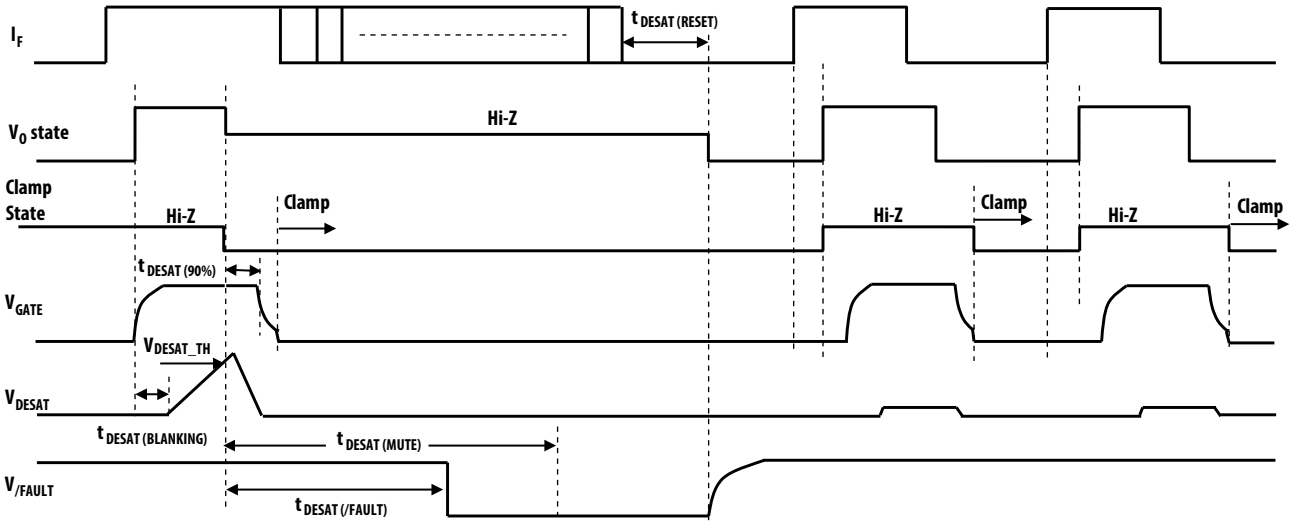
Description of Under Voltage Lock Out

Insufficient gate voltage to MOSFET can increase turn on resistance of MOSFET, resulting in large power loss and MOSFET damage due to high heat dissipation. ACPL-335J monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect MOSFET from low voltage bias. During power up, the UVLO feature forces the gate driver output to low to prevent unwanted turn-on at lower voltage.

Description of Operation during Over Current Condition

1. DESAT terminal monitors MOSFET's Drain-Source voltage, V_{DS}.
2. When the voltage on the DESAT terminal exceeds Desat sensing threshold, the output shuts down immediately.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.
5. When $t_{DESAT(MUTE)}$ expires LED input need to be kept low for $t_{DESAT(RESET)}$ before fault condition is cleared. FAULT status will return to high and CLAMP output will return to Hi-Z state.
6. Output (V_O) starts to respond to LED input after fault condition is cleared.

Figure 17 Circuit behaviors during over current event

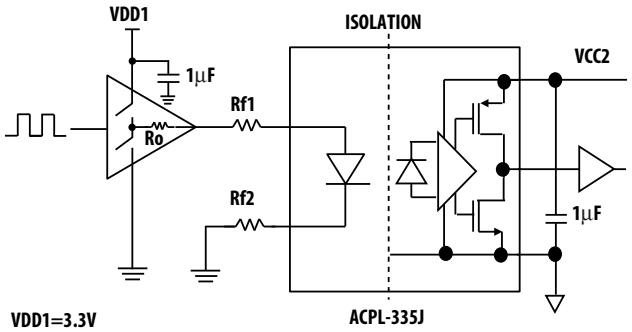


Recommended LED Drive Circuits

There will be common mode noise whenever there is a difference in the ground level of the optocoupler's input control circuitry and that of the output control circuitry. Figure 18 and Figure 19 show the recommended LED drive circuits that use logic gate (CMOS buffer) for high common mode rejection (CMR) performance of the optocoupler gate driver. Split limiting resistors are used to balance the impedance at both anode and cathode of the input LED for high common mode noise rejection. The output impedance of the CMOS buffer (shown as R_O in Figure 18 and Figure 19) has to be included in the calculation for LED drive current.

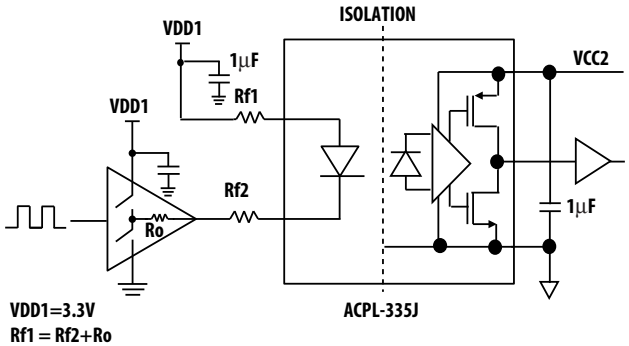
On the other hand, Figure 20 shows the recommended LED drive circuits that use a single transistor. During the LED off state, M1 and Q1 in Figure 20 will shunt current, which results in greater power consumption. It is not recommended to have open drain and open collector drive circuits, as shown in Figure 21. This is because during the off state of the MOSFET/transistor, the cathode of the input LED sees high impedance and becomes sensitive to common mode switching noise.

Figure 18 Recommended non inverting drive circuit



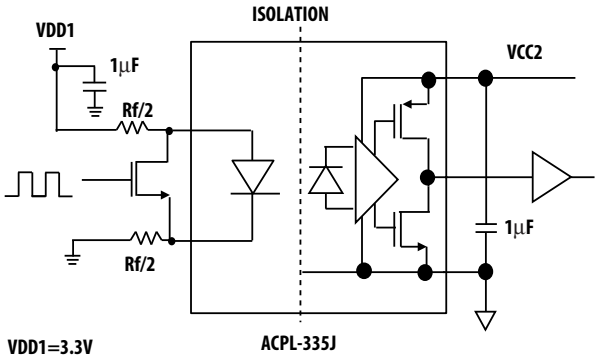
VDD1=3.3V
Rf2 = Rf1+Ro
Recommended Ro+Rf1+Rf2 = 140Ω

Figure 19 Recommended single transistor drive circuit

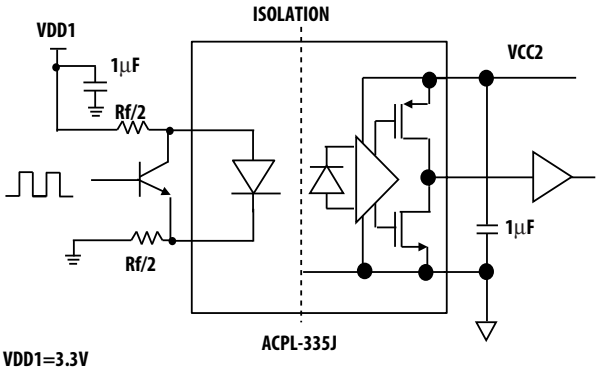


VDD1=3.3V
Rf1 = Rf2+Ro
Recommended Ro+Rf1+Rf2 = 140Ω

Figure 20 Recommended inverting drive circuit

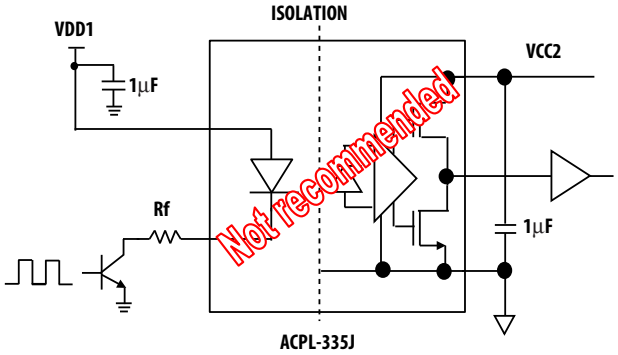


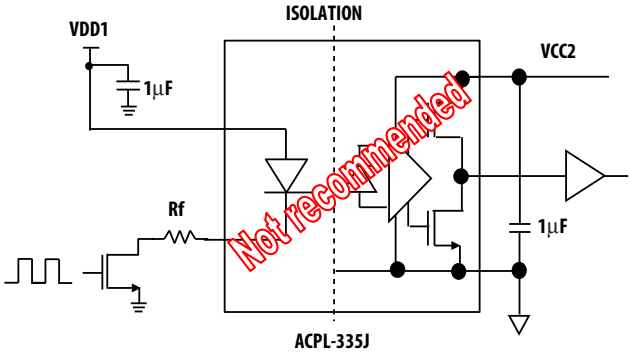
VDD1=3.3V
Recommended Rf = 140Ω



VDD1=3.3V
Recommended Rf = 140Ω

Figure 21 Not recommended – Open drain/ open collector drive circuit





Drive Power

If a CMOS buffer is used to drive the LED, it is recommended that user connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually greater than the driving capability of the PMOS in a CMOS buffer.

Drive Logic

The designer can configure LED drive circuits for non-inverting and inverting logic as recommended in Figure 21 and Figure 22. For the inverting and non-inverting logic to work, the external power supply V_{DD1} must be connected to the CMOS buffer. If the V_{DD1} supply is lost, the LED will be permanently off and output will be low.

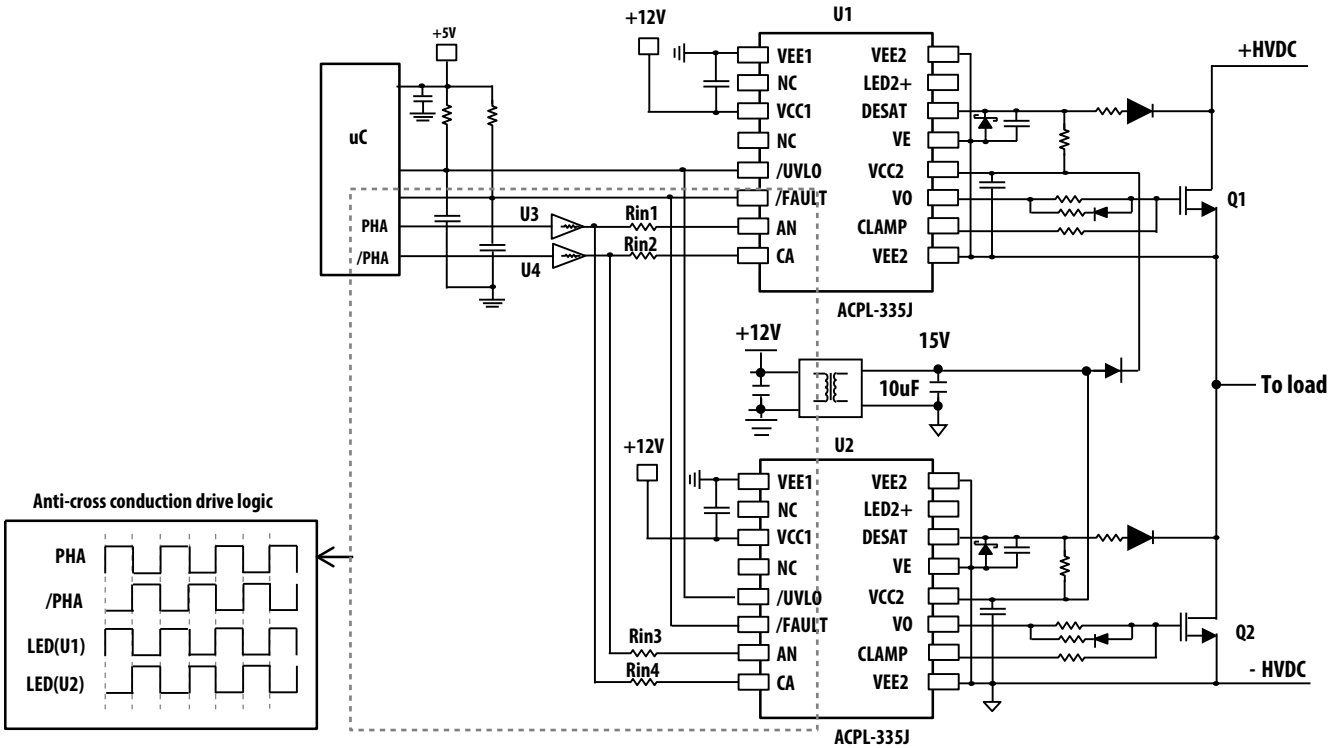
Bypass and Reservoir Capacitors

Supply bypass capacitors are necessary at the input buffer and ACPL-335J output supply pins. A ceramic capacitor with the value of 1 µF is recommended at the input buffer to provide high frequency bypass, which also helps to improve CMR performance. At the output supply pins, it is recommended to use a 1 µF low ESR and low ESL capacitor across $V_{CC2} - V_E$, $V_E - V_{EE2}$ and $V_{CC2} - V_{EE2}$ pins. These capacitors are used to supply instant driving current to MOSFET at V_{OUT} during switching.

Anti-Cross Conduction Drive

One of the many benefits of using ACPL-335J is the ease of implementing anti-cross conduction drive between the high side and the low side gate drivers to prevent a shoot-through event. This safety interlock drive can be realized by interlocking the output of buffer U3 and U4 to both the high and the low side gate drivers, as shown in Figure 22. Due to the difference in propagation delay between optocouplers, however, a certain amount of dead time has to be added to ensure sufficient dead time at the MOSFET gate. For more details, see the “Dead Time and Propagation Delay” section.

Figure 22 Typical high speed MOSFET gate drive circuit



Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high side and low side power transistors (shown as Q1 and Q2 in Figure 22) are off. Originally, the system is required to design in some amount of dead time to compensate for the turnoff delay needed for the MOSFET to discharge the input capacitance after the gate is switched off. In this application note, this amount of dead time is called system original dead time. When an optocoupler is used, the designer has to consider the effect of the optocoupler's dead time distortion (DTD) toward system original dead time. The optocoupler's negative DTD decreases system original dead time; on the other hand, the optocoupler's positive DTD increases system original dead time. Therefore, the designer must add extra dead time to system original dead time to compensate for the optocoupler's negative DTD. Figures 23 and 24 illustrate the effect of the optocoupler's DTD to system original dead time.

Dead Time and Propagation Delay Waveforms

Figure 23 Negative DTD reduces original DT

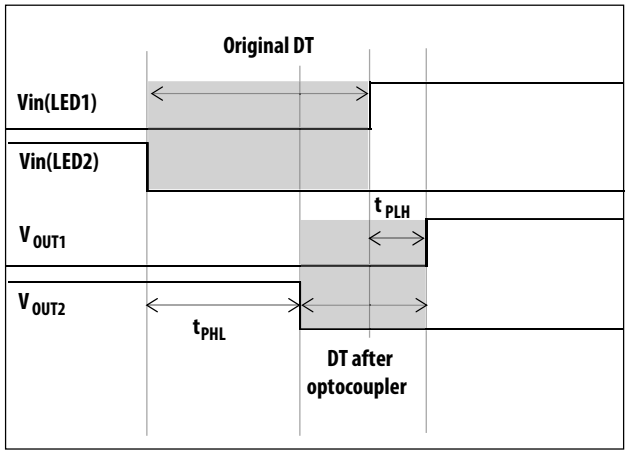
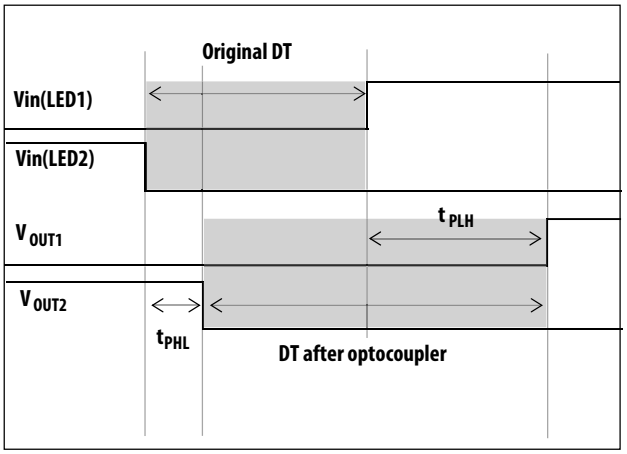


Figure 24 Positive DTD increases original DT



Here is an example of total dead time calculation for a typical optocoupler drive circuit for MOSFET.

Total dead time required

= System original dead time + |optocoupler's negative DTD|

= System original dead time + |100 ns|

where system original dead time = MOSFET turn-off delay

Note:
The propagation delays used to calculate dead time distortion (DTD) are taken at equal temperatures and test conditions as the optocouplers used under consideration are typically mounted in close proximity to each other and are switching same type of MOSFETs.

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