

CERAMIC SMD CRYSTAL CLOCK OSCILLATOR

ABFM SERIES



RoHS
Compliant



7.0 x 5.0 x 1.8mm

FEATURES:

- Based on a proprietary analog multiplier
- Tri-State Output
- Ultra low Phase Noise
- 125MHz, 156.25MHz, 187.5MHz, and 212.5MHz applications
- 2.5V to 3.3V +/- 10% operation
- Ceramic SMD, low profile package

APPLICATIONS:

- Fiber Channel
- 12Gbit SERDES
- 10Gbit SERDES
- PCI Express

STANDARD SPECIFICATIONS:

PARAMETERS

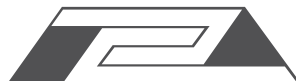
ABRACON P/N	ABFM Series
Frequency Range	30 MHz to 280 MHz (Contact ABRACON for frequencies out of the range)
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	- 55°C to + 125°C
Overall Frequency Stability:	± 50 ppm max. (see options)
Supply Voltage (Vdd)	3.3V or 2.5V ±10% (see options)
Jitter	See Table 2.1
Low Phase Noise	See Table 2.1
Aging (ppm/ the first year) :	± 3.0 ppm max.

PECL

Supply Current (I_{DD}) [$F_{out} = 212.50\text{MHz}$]	100mA max.
Output Clock Duty Cycle @ $V_{DD}=1.3\text{V}$	45% min, 50% typical, 55% max.
Output High Voltage (V_{OH})	$V_{DD} - 1.025\text{V}$ min
Output Low Voltage (V_{OL})	$V_{DD} - 1.620\text{V}$ max
Clock Rise time (t_r) @ 20/80%	0.2ns typ, 0.8ns max
Clock Fall time (t_f) @ 80/20%	0.2ns typ, 0.8ns max

LVDS

Supply Current (I_{DD}) [$F_{out} = 212.50\text{MHz}$]	55mA typical, 60mA max
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V_{OD})	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV_{OD})	-50mV min, 50mV max
Output High Voltage (V_{OH})	1.4V typical, 1.6V max
Output Low Voltage (V_{OL})	1.1V typical, 0.9V min
Offset Voltage [$R_L = 100\Omega$]	$V_{OS} = 1.125\text{V}$ min, 1.2V typical, 1.375V max
Offset Magnitude Voltage [$R_L = 100\Omega$]	$\Delta V_{OS} = 0\text{mV}$ min, 3mV typical, 25mV max
Power-off Leakage (I_{OXD}) [$V_{out}=V_{DD}$ or GND, $V_{DD}=0\text{V}$]	±1mA typical, ±10µA max
Output Short Circuit Current (I_{OSD})	-5.7mA typ, -8mA max
Differential Clock Rise Time (t_r) [$R_L=100\Omega$, $C_L=10\text{pF}$]	0.2ns min, 0.5ns typical, 1.0ns max
Differential Clock Fall Time (t_f) [$R_L=100\Omega$, $C_L=10\text{pF}$]	0.2ns min, 0.5ns typical, 1.0ns max



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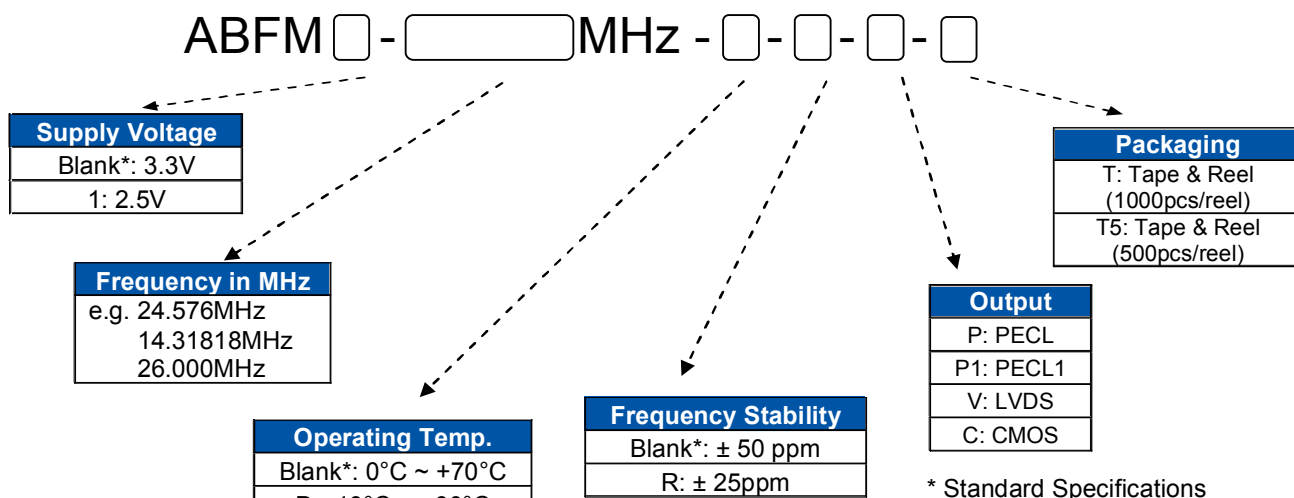
STANDARD SPECIFICATIONS:

CMOS	
Supply Current (I_{DD}) [at 100MHz, load 15pF]	16mA typ, 40mA max
Output Clock Duty Cycle @ 50% V_{DD}	45% min, 50% typical, 55% max
Output High Voltage (V_{OH}) [$I_{OH} = -8.5mA$]	2.4V min
Output Low Voltage (V_{OL}) [$I_{OL} = 8.5mA$]	0.4V max
Output Drive Current (I_{OSD}) [$V_{OL} = 0.4V$, $V_{OH} = 2.4V$]	8.5mA typ
Output Clock Rise/Fall time [10% ~ 90% V_{DD} w/10pF load]	2.0ns typical, 2.5ns max
Output Clock Duty cycle [Measured @ 50% V_{DD}]	45% min, 50% typical, 55% max

Table 2.1 (Example data. Frequency dependent. Reference only)

Frequency (MHz)	Phase Noise (dBc)			Phase jitter RMS (ps)		Period jitter peak to peak (ps)	
	Offset			Typical	Max	Typical	Max
	1kHz	10kHz	100kHz				
155.52	-128	-137	-143	0.5	1	5	10
212.5	-115	-122	-120	3.5	5	10	20
312.5	-113	-120	-115	3.5	5	10	20
622.08	-107	-117	-111	3.5	5	10	20

OPTIONS AND PART IDENTIFICATION [Left blank if standard]



TRI-STATE PIN OUT DESCRIPTION:

OUTPUT TYPE OPTION		PIN 1 logic level* (Tri-State pinout operation)	Output State
P	PECL	1	Tri-state
		0 (Default)	Enabled
P1	PECL1	0	Tri-state
		1	Enabled
V	LVDS	0	Tri-state
		1(Default)	Enabled
C	CMOS	0	Tri-state
		1(Default)	Enabled

*Connect to VDD for logic level "1", connect to ground for logic level "0".



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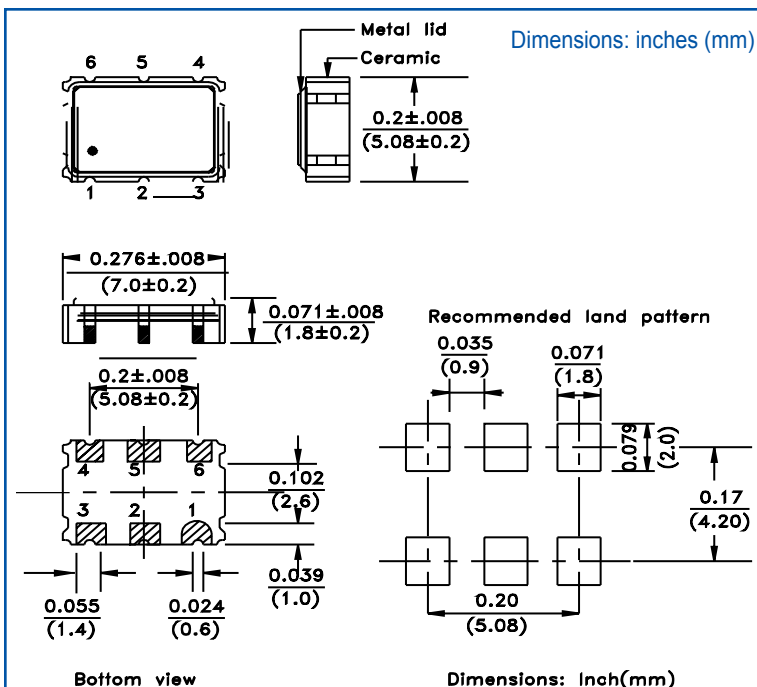


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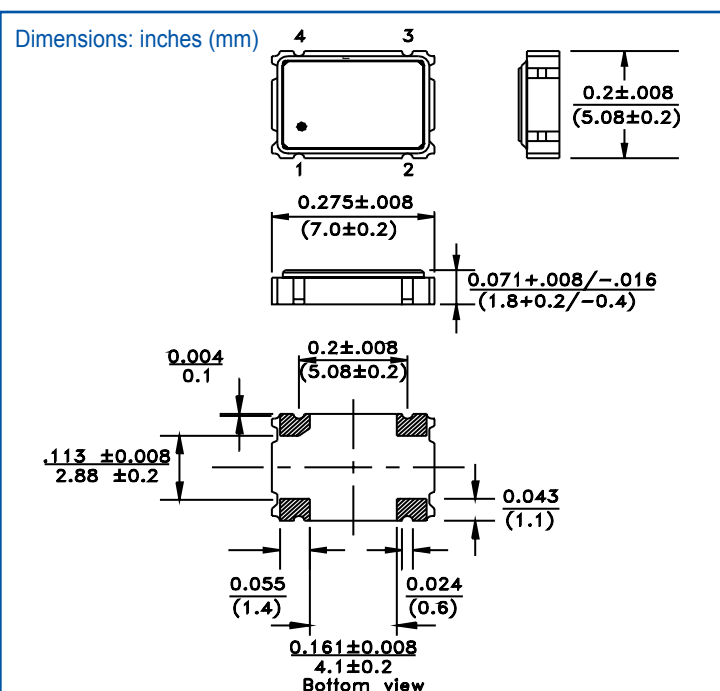
7.0 x 5.0 x 1.8mm

PECL & LVDS OUTLINE DRAWING:



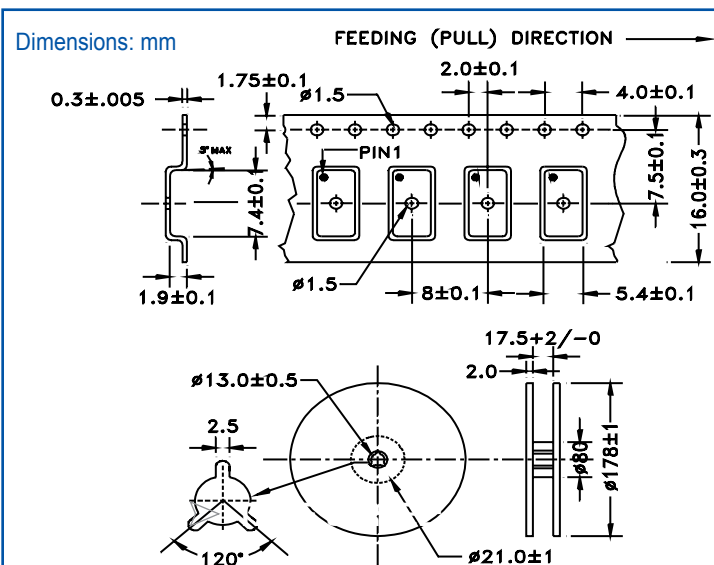
PIN #	Name	Description
1	Tri-state	Tri-state
2	NC	No Connect
3	GND	Ground
4	Q	PECL, LVDS
5	Q'	Complimentary PECL, LVDS
6	V _{DD}	VDD Connection

CMOS OUTLINE DRAWING:

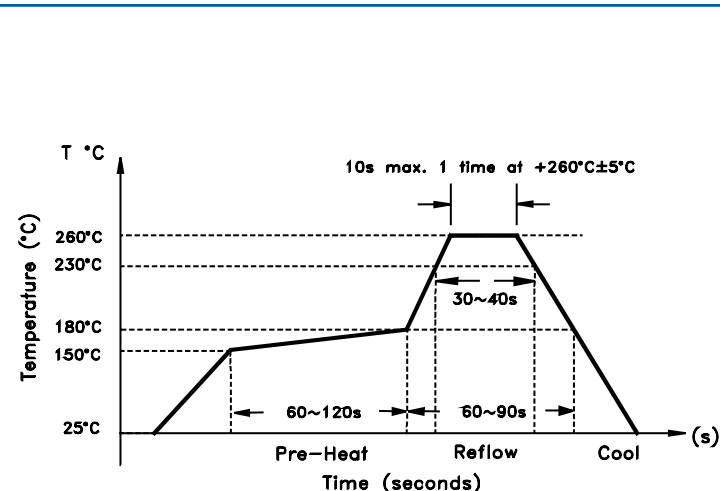


PIN	FUNCTION
1	Tristate
2	GND/Case
3	Output
4	Vdd

TAPE & REEL: T= tape and reel (1,000pcs/reel)



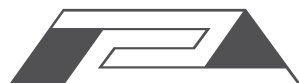
REFLOW PROFILE:



Need a test socket for the ABFM Series?
To view compatible **PRECISION TEST AND BURN-IN SOCKETS** for these parts, [click here.](#)

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