APPLICATION NOTE

ATA663211 LIN TRX VHDL Model - Level 2 Model Documentation

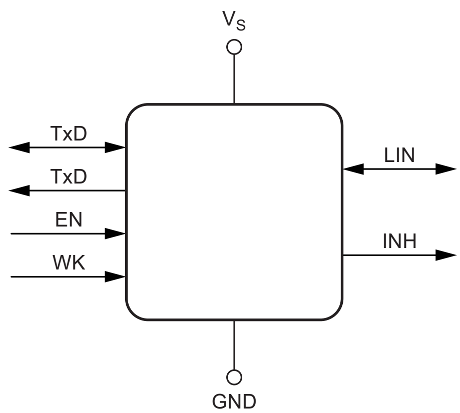
ATAN0100

Level 2 Approach Schema

In a level 2 approach, the model is kept as simple as possible with the main characteristics of the device subdivided into blocks. The output ports are shown in Figure 1:

- **VBAT** Supply positive port (VS refers to the same pin, which is used in figures)
- **GND** Ground or supply negative port
- **LIN** Bus connection, LIN input/output
- **INH** Inhibit output, connects Vs directly when the device is operable
- **EN** Enable port, a high state enables data transmission
- **WK** Wake-up port, high voltage input, a low level wakes up the device
- **TxD** Transmission port, includes a pull-down transistor
- **RxD** Receiver port, includes a pull-down transistor

Figure 1. Model Inputs and Outputs



A main block does the signal filtering and general control inside the model (for more information, see Figure 2 on page 2). This main block (monitor) continuously communicates with the state machine block, sending the filtered wake, EN and supply state signals. The state machine block decides the actual state of the model with respect to the filtered signals that the monitor sends.

The monitor is the main control and also specifies when to actuate any switch on the model (pull-down transistor, output switch, etc.). The monitor additionally reads the actual state from the state machine block as feedback and makes decisions based on it.

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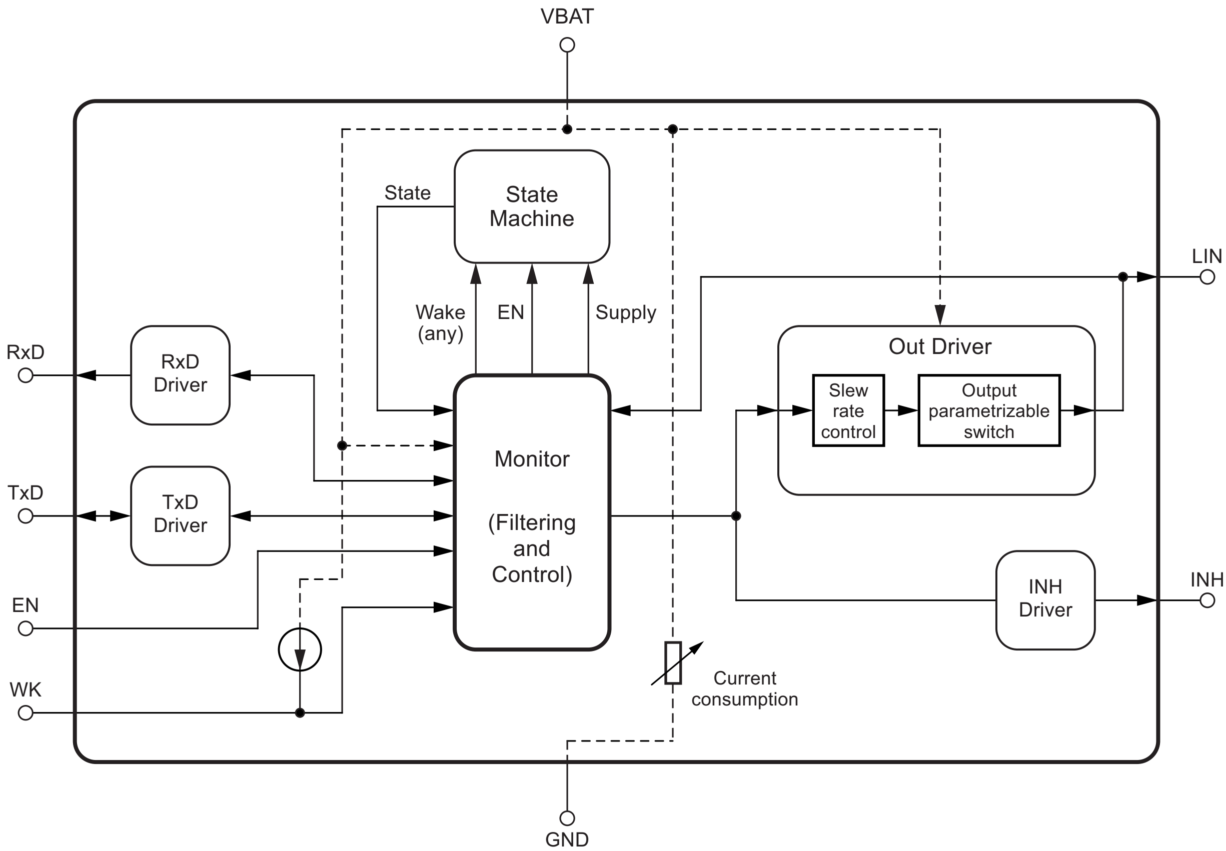
Counters or timing filters are implemented in the monitor and in this way the state machine block is simplified as much as possible, receiving the filtered signals instead of raw acquisition from the periphery.

Pull-down transistors are implemented characterizing their interfaces on RxD and TxD drivers. The output driver includes a characteristic slew rate control and output interface containing the main switch of the model. Pull-up circuitry is implemented inside this block.

The INH driver consists of an internal transistor connecting the INH pin directly to VBAT when this is switched on. In Figure 2 VBAT is used to illustrate that in this case the supply pin should be named as specified in (4).

Figure 2. Level 2 Approach Schema



As the model specifies, a pull-up current supply in WK was modeled in relation to the power supply state. The model maintains the characteristics from the measurement information provided by the manufacturer regarding the temperature scenario as well supply variation.

The current consumption in different modes (normal, sleep, etc.) was modeled in an abstract manner, with an equivalent resistor that changes its value for each scenario. This consumption maintains the changes with respect to temperature scenario and supply level variation.

Reference List

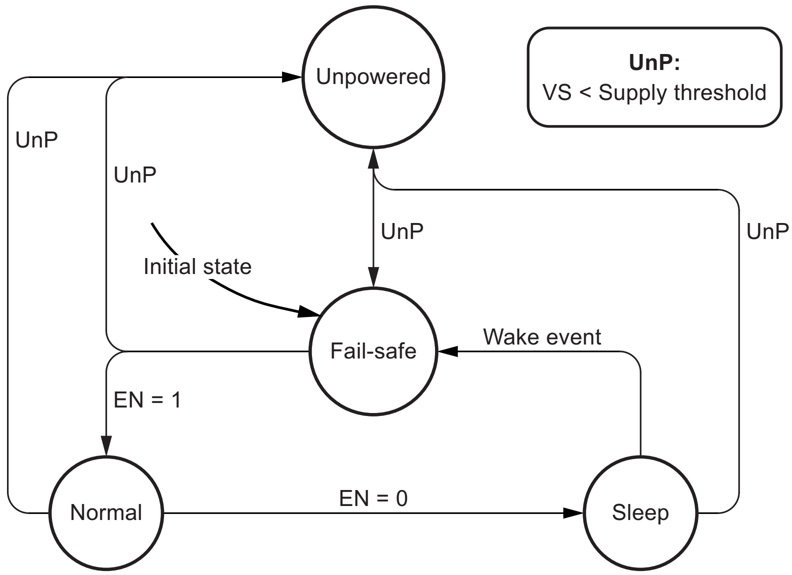
1. ATA6632xx_doc9198.pdf
2. ATA6632-4_36861-ED.xls
3. ATA666x_VHDL_AMS_Modell_v2.pdf
4. LIN OSI Layer1 Physical Layer for LIN Specification V2.2 for devices with RX TX access.pdf
5. LIN OSI Layer1 Physical Layer for LIN Specification V2.2 for devices without RX TX access.pdf

1. States Covered by the Model

The state machine can vary among the four states (see Figure 1-1)

- Sleep (S)
- Fail-safe (FS)
- Normal (N)
- Unpowered (UnP).

Figure 1-1. State Machine



When the device is powered, the state machine begins in fail-safe mode (FS). If the supply voltage (VBAT) is low, the state machine goes to the unpowered mode (UnP). A change from UnP to FS is only possible with VBAT moving to a correct level.

During FS mode a high level on the enable pin (EN) changes the state to normal if the voltage on TxD pin is recessive. If this voltage is dominant, the state does not change from FS until it changes to recessive.

In N mode, if the EN goes down, the state changes to sleep mode (S). With a high level on EN, it changes from S to FS and generates a wake process. After the wake-up time is reached, the mode automatically changes from FS to N.

Any of the options for generating a wake-up process, i.e., wake-up process via the WK pin (local wake-up), EN pin (local wake-up) or LIN bus (remote wake-up) can only change the state from S to FS. A change from FS to N requires the EN to be high.

2. Model Behavior - Test Benches

Different test benches were performed in order to show the behavior of the model and its interaction with external signals. A description of each one is shown in Table 2-1.

Table 2-1. Sections on the Test Bench Draw

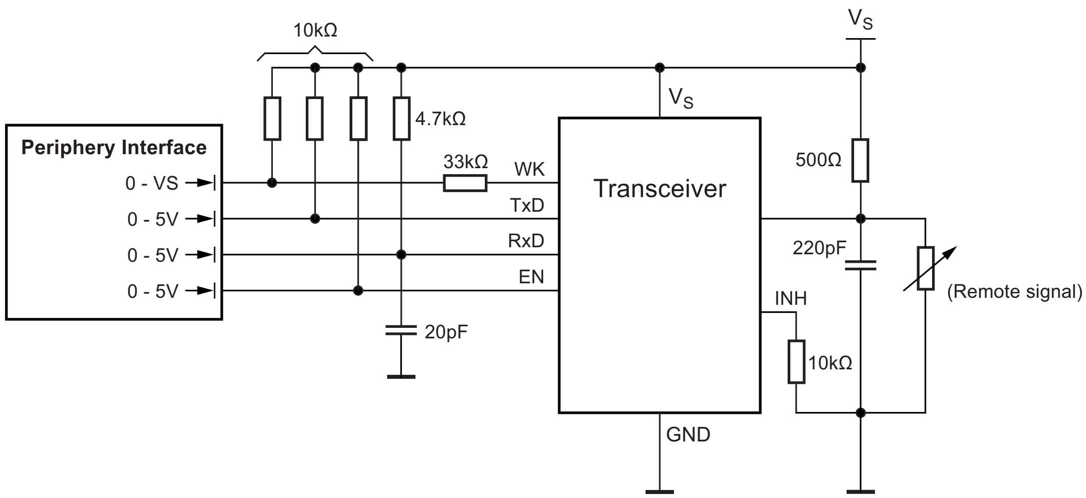
Test Bench	Description
TB_a	Startup, sleep mode, wake via the EN, normal behavior
TB_b	Normal to sleep, sleep to normal, wake-up via the WK pin
TB_c	Wake-up via the BUS
TB_d	Three devices with min, typ and max use cases
TB_e	TxD/LIN time-out functionality

2.1 Test Circuit

To compare the required behavior of the model (Figure 2 on page 2) with the simulation outputs, the circuit shown in Figure 2-1 was used. This circuit can be analyzed using the top-level “test bench” or “demo” file. Please also note that the signals generated from the periphery of the model are WK, TxD, EN and LIN. They are stimulus signals.

The WK stimulus control signal is generated as a high-voltage signal. TxD and EN signals are low-voltage signals, in this case modeled with a high level of 5 [V]. The LIN control signal comes from an imaginary node (remote signal) and is modeled as a load for the LIN pin that switches to a high-resistance or low-resistance value.

Figure 2-1. Test Bench Circuit



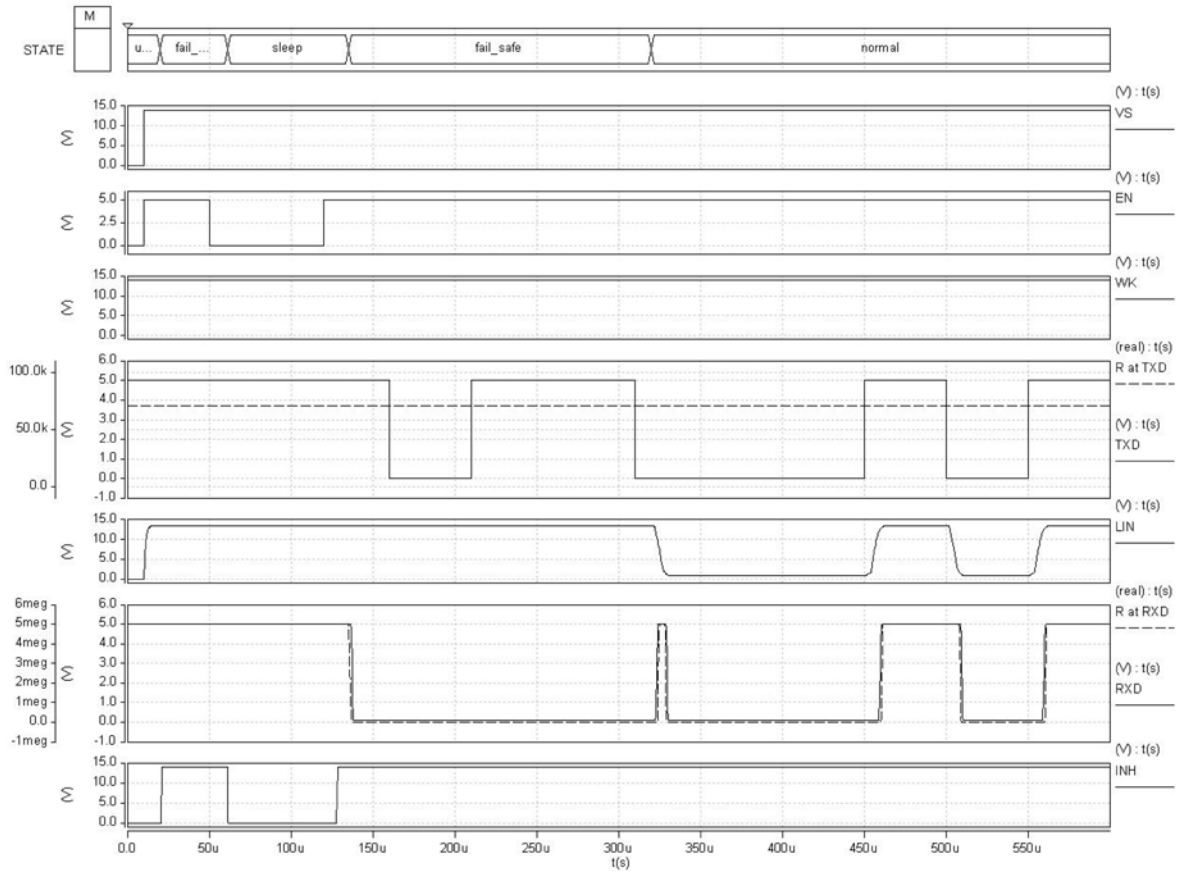
2.2 State Transitions and Logic Behavior

2.2.1 Initialization of the Model and Typical Transmission

Figure 2-2 shows the behavior of the test bench "TB_a" of Table 2-1 on page 4, while in Figure 2-3 on page 6 and Figure 2-4 on page 6 a detailed view of the power-on and power-off situations is shown.

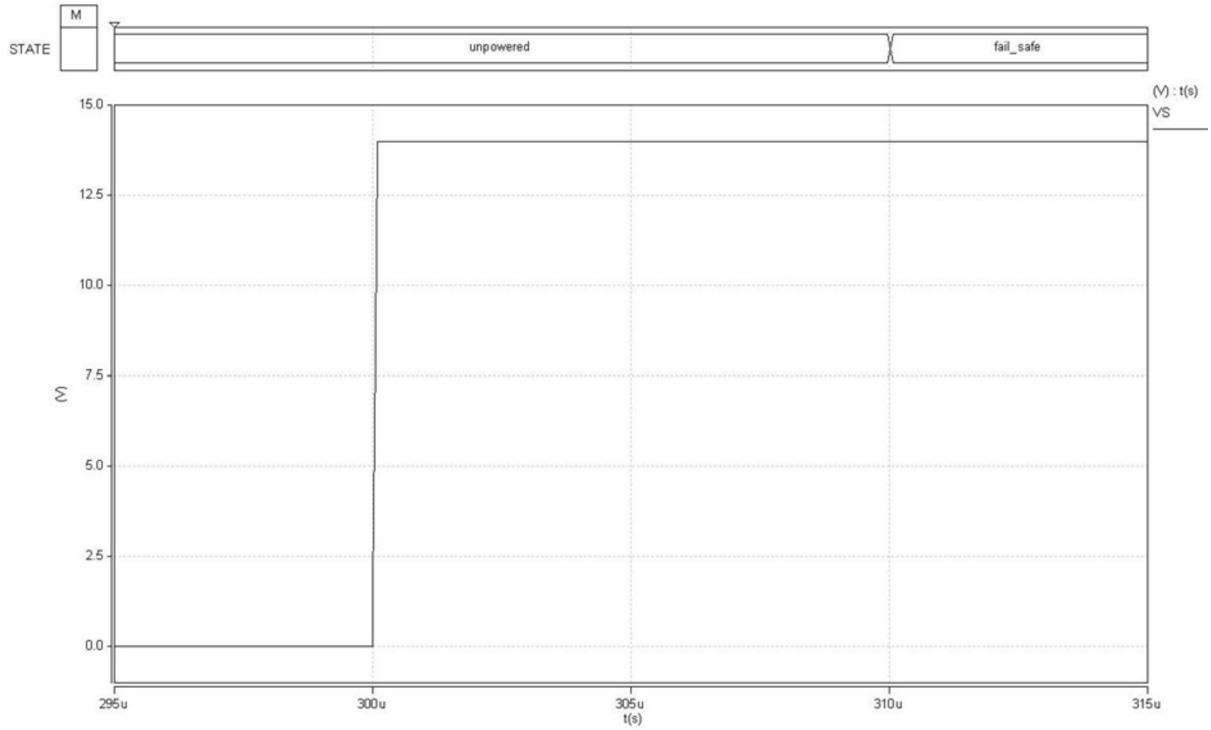
- The model starts at unpowered mode (UnP) and when the supply voltage (VBAT) goes to high the model changes from UnP mode to fail-safe mode (FS). During FS mode an enable signal (EN=low) activates sleep mode (S) behavior after the appropriate delay.
- During sleep mode the inhibit pin (INH) is internally disconnected from the supply (VBAT).
- From S mode, with EN=high, a wake process is active and switches the state to fail-safe mode (FS). After the appropriate time it automatically changes to normal mode (N).
- Once in N mode, LIN follows TxD and RxD follows LIN.

Figure 2-2. EN and TXD Signals are Stimulus



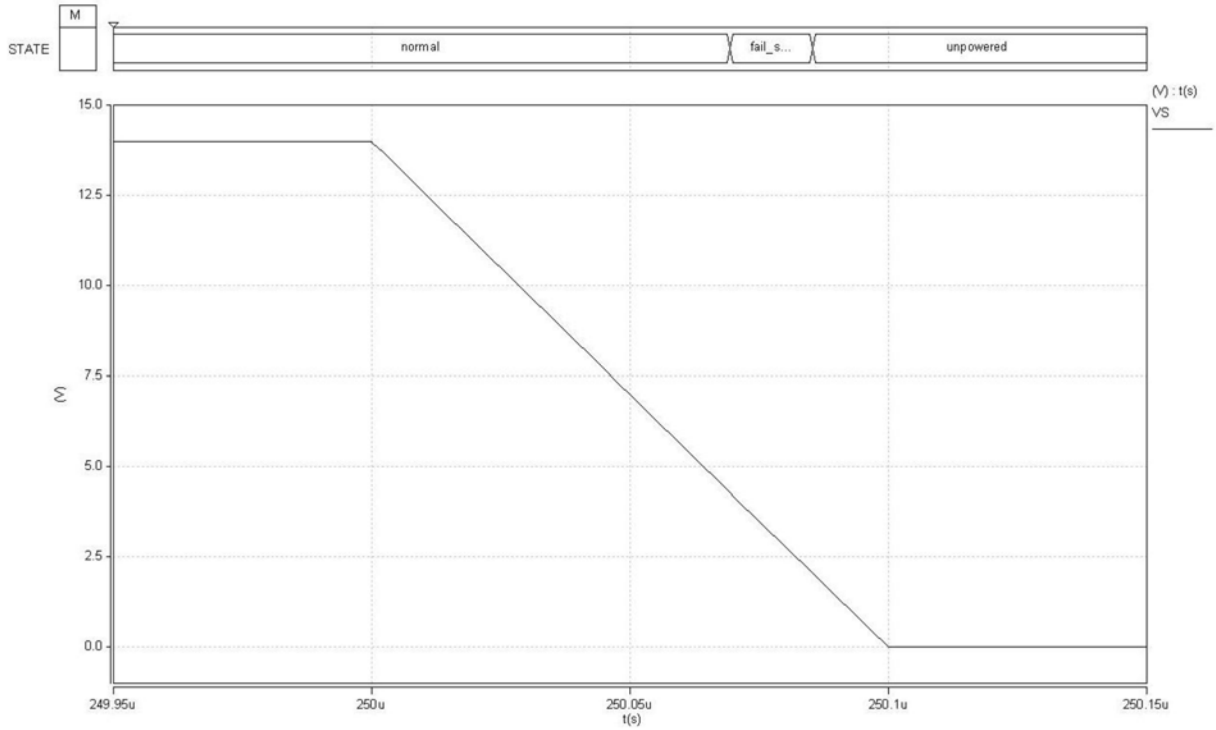
A detailed view during a power-on is shown in Figure 2-3. The device starts at FS mode.

Figure 2-3. Power-on



A detailed view during a power off is shown in Figure 2-4. When the supply level is lower than a threshold, the device changes its state to FS mode. When the supply level decreases even more, the device changes its state to UnP mode.

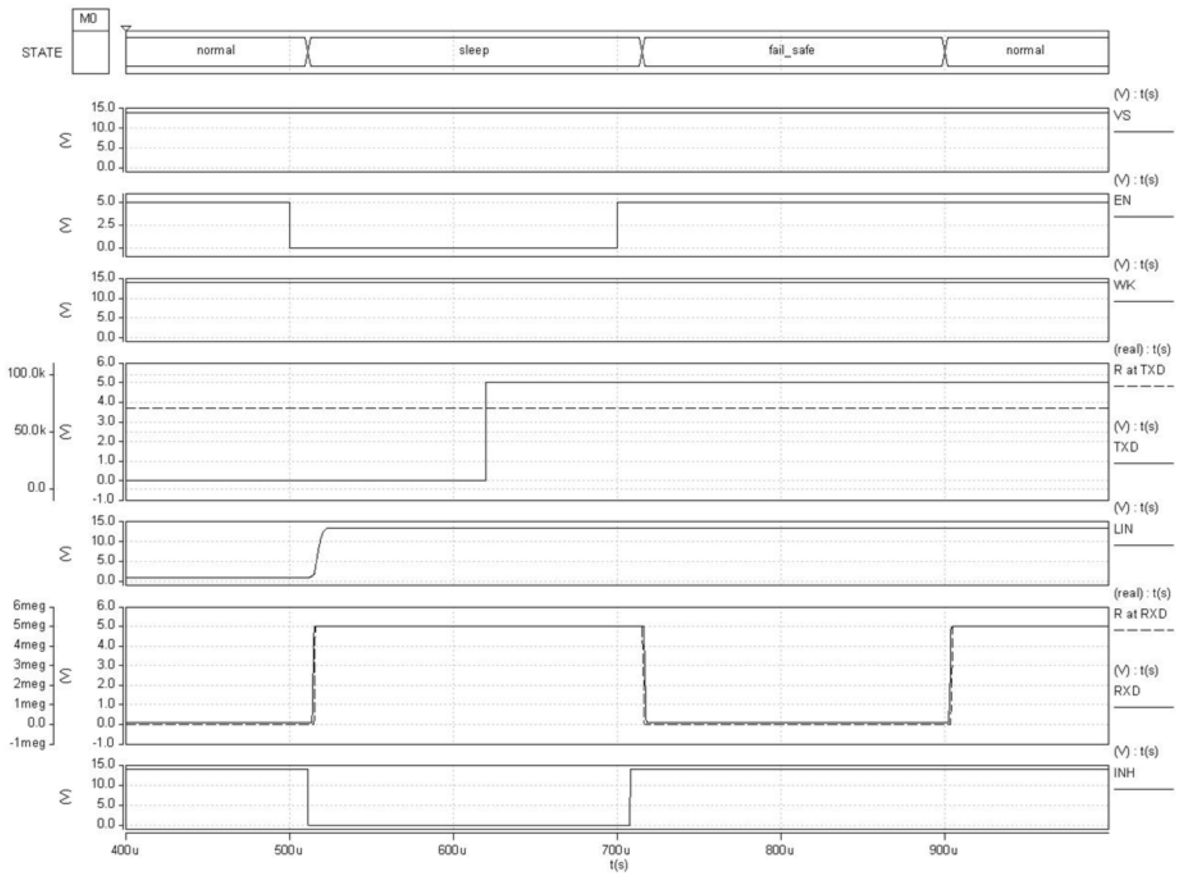
Figure 2-4. Power Off



2.2.2 Normal to Sleep, Sleep to Normal

Figure 2-5 shows a state change from normal mode (N) to sleep mode (S). The figurer shows the corresponding delays and how the transmission are switched off during sleep mode. During S mode, EN goes high and a wake-up process starts changing the state to fail safe (FS) mode and, after an appropriate time, to N mode. During FS mode, a wake caused by EN is signaled on the RXD pin with the pull-down transistor.

Figure 2-5. Normal Mode to Sleep Mode and Vice Versa



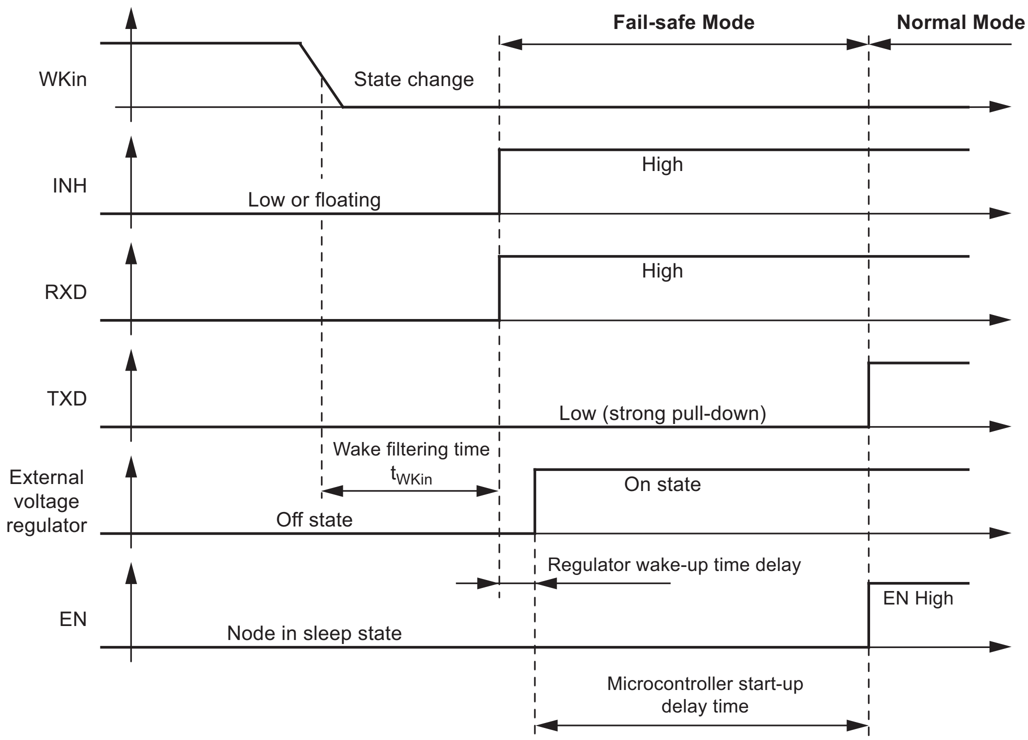
2.2.3 Wake-up Modes

2.2.3.1 Local Wake-up via WK Pin

The process of a local wake-up via the WK pin is as follows:

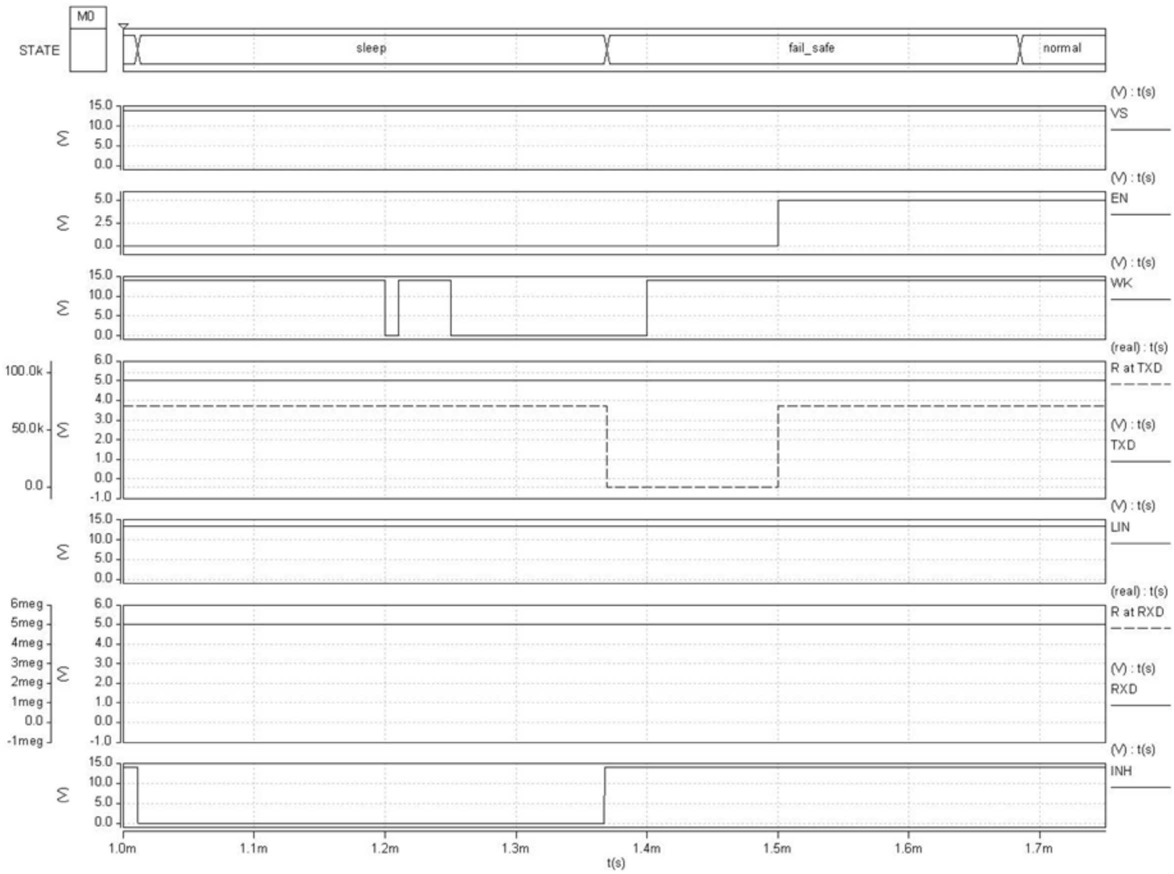
- A falling edge at the WK pin followed by a low level maintained for a certain period of time (> t_{WKin}) result in a local wake-up request, causing the device to switch to fail-safe mode.
- The INH pin is activated (switches to VS).
- The local wake-up request is indicated by a low level at the TXD pin and high level at the RXD pin, generating an interrupt for the microcontroller.
- When the WK pin is low, it is possible to switch to sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10µs before the negative edge at WK starts a new local wake-up request.

Figure 2-6. Local Wake-up via WK Pin



The signals resulting from the test bench are shown in Figure 2-7. A local wake-up process takes place only for signals that fall to dominant and stay for a time greater than t_{WKin}. In this test bench a small pulse in WK is shown in order to demonstrate that the model does not wake up.

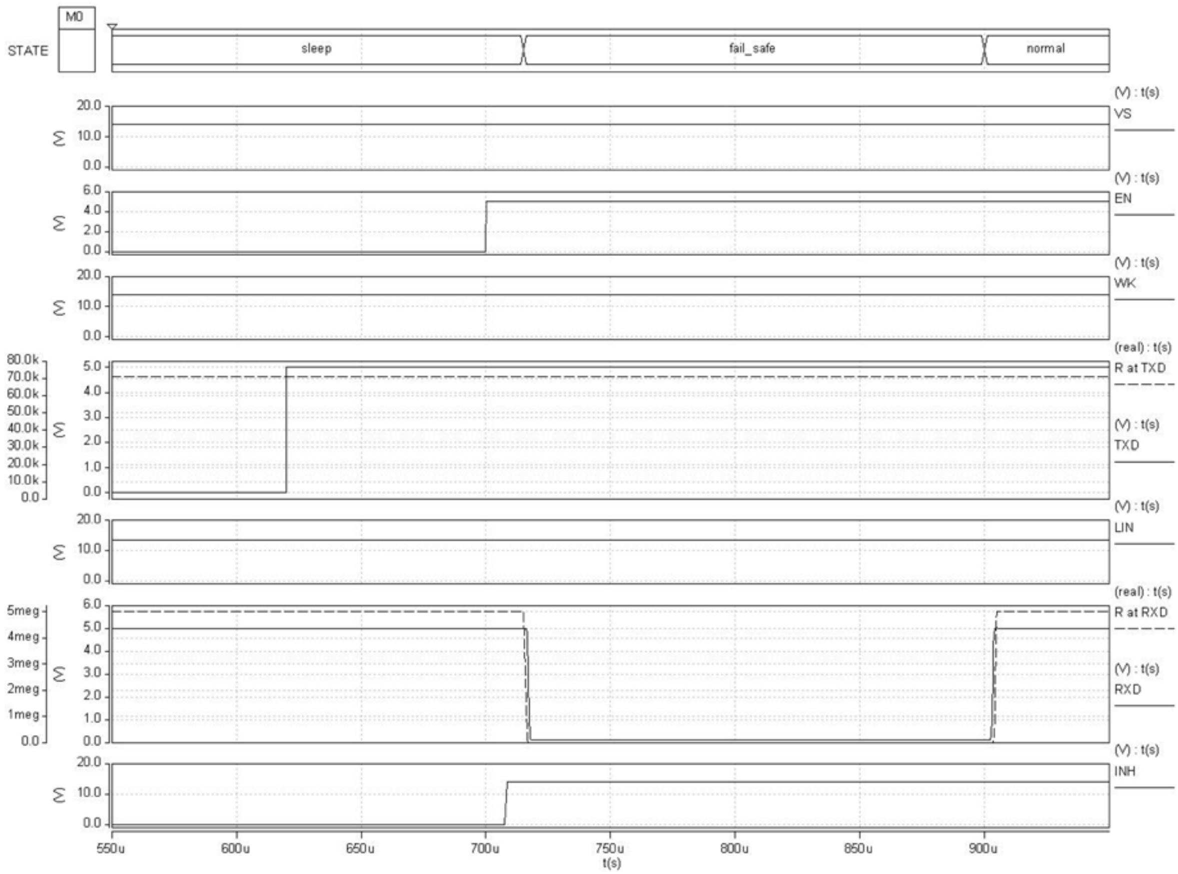
Figure 2-7. Local Wake by WK



2.2.3.2 Local Wake-up via the EN Pin

When the device sleeps, a wake-up with the EN pin is possible. This process is shown in Figure 2-8. The wake-up source is signaled by the RxD pull-down transistor.

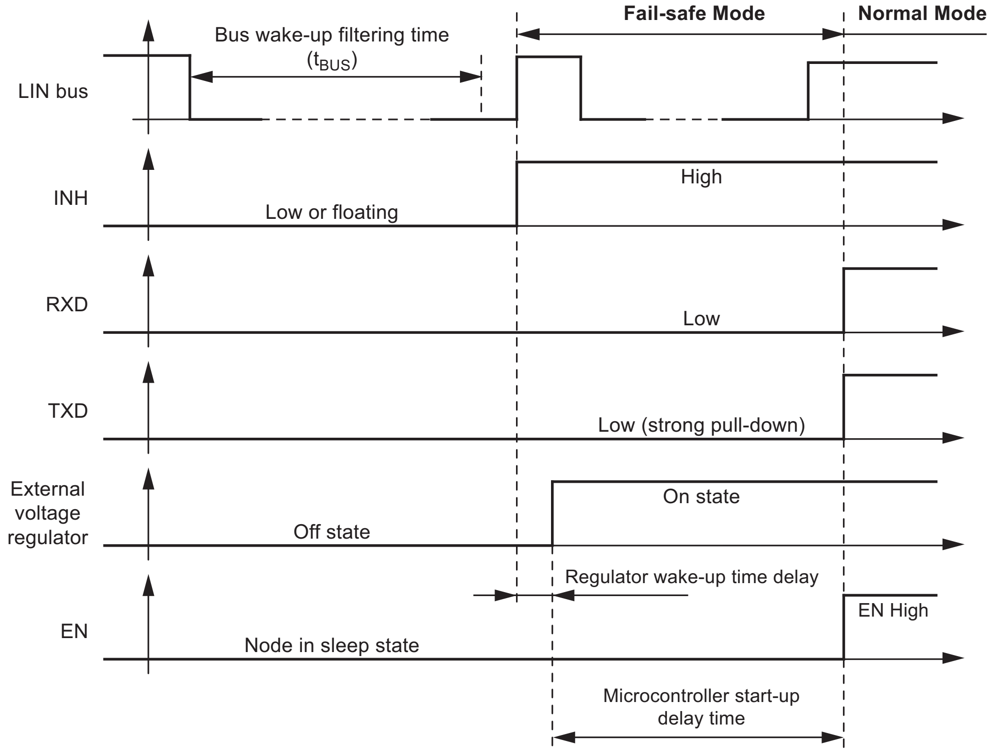
Figure 2-8. Local Wake-up by the EN Pin



2.2.3.3 Remote Wake-up from Sleep Mode

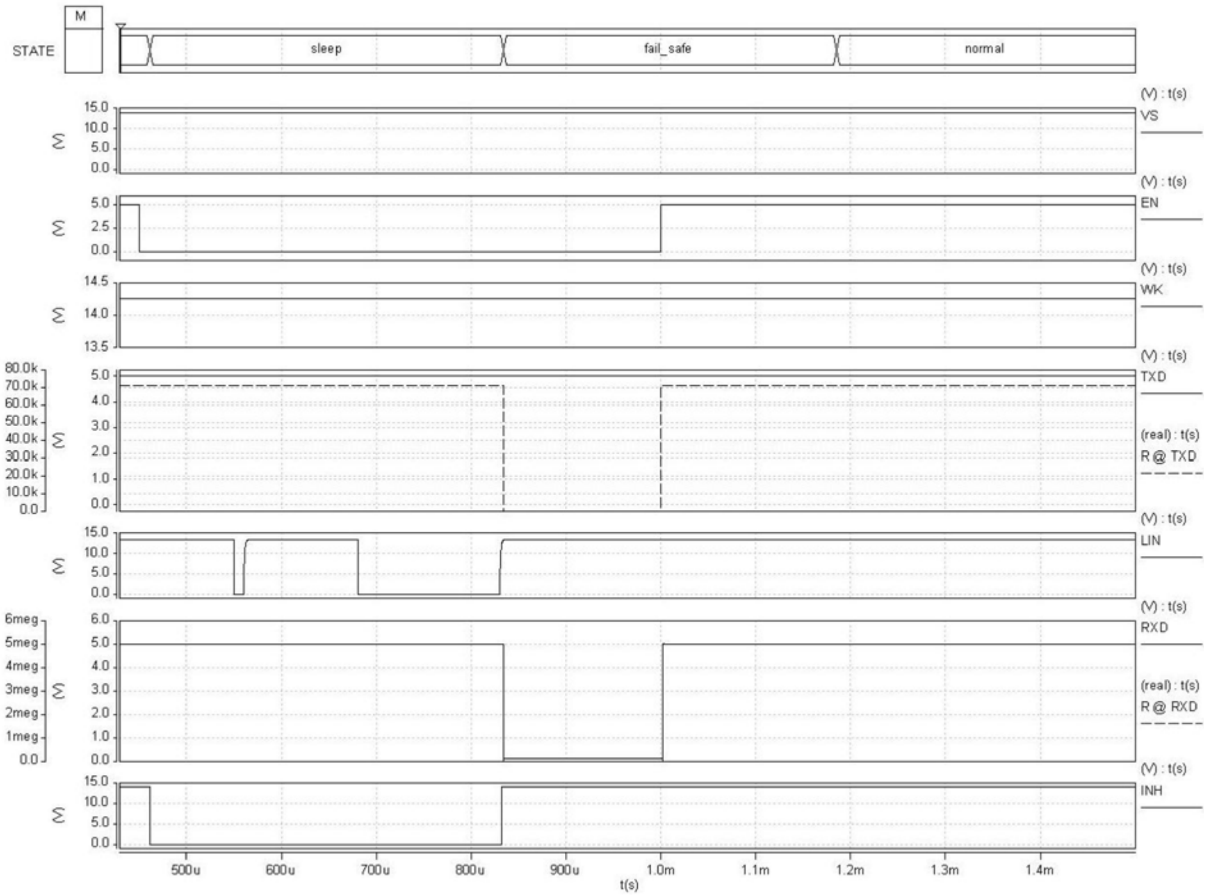
- A voltage lower than the LIN pre-wake detection (VLINL) at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.
- A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{BUS}) and following a rising edge at the LIN pin result in a remote wake-up request, causing the device to switch to fail safe mode.
- The INH pin is activated (switches to VBAT) and the internal termination resistor is switched on.
- The remote wake-up request is indicated by a low level at pin RXD and interrupts the microcontroller.

Figure 2-9. Remote Wake-up from Sleep Mode



The signals resulting from the test bench are shown in Figure 2-10. A remote wake-up process takes place only for signals that fall to dominant and stay for a time greater than t_{BUS} followed by a rising edge. In the figure it can be seen that a short time duration pulse in LIN does not wake up the model. If a sufficiently long pulse is applied, a counter reaches its time-out value. After a rising edge in LIN, the model enters in FS mode and signals the wake source with TXD and RXD going low. With EN = high during FS mode, the model finishes the wake-up process.

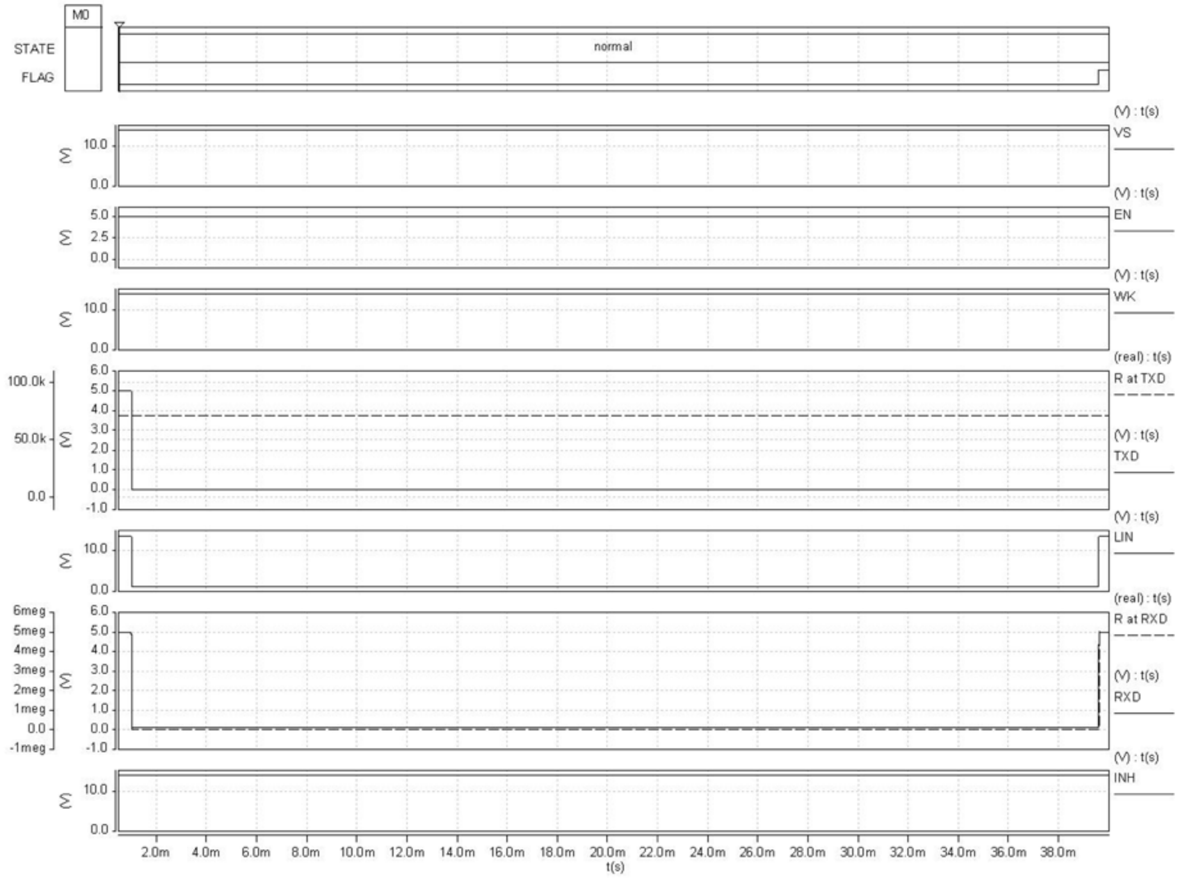
Figure 2-10. Remote Wake-up



2.2.4 LIN Time Out (for Signals with Long TxD = Dominant)

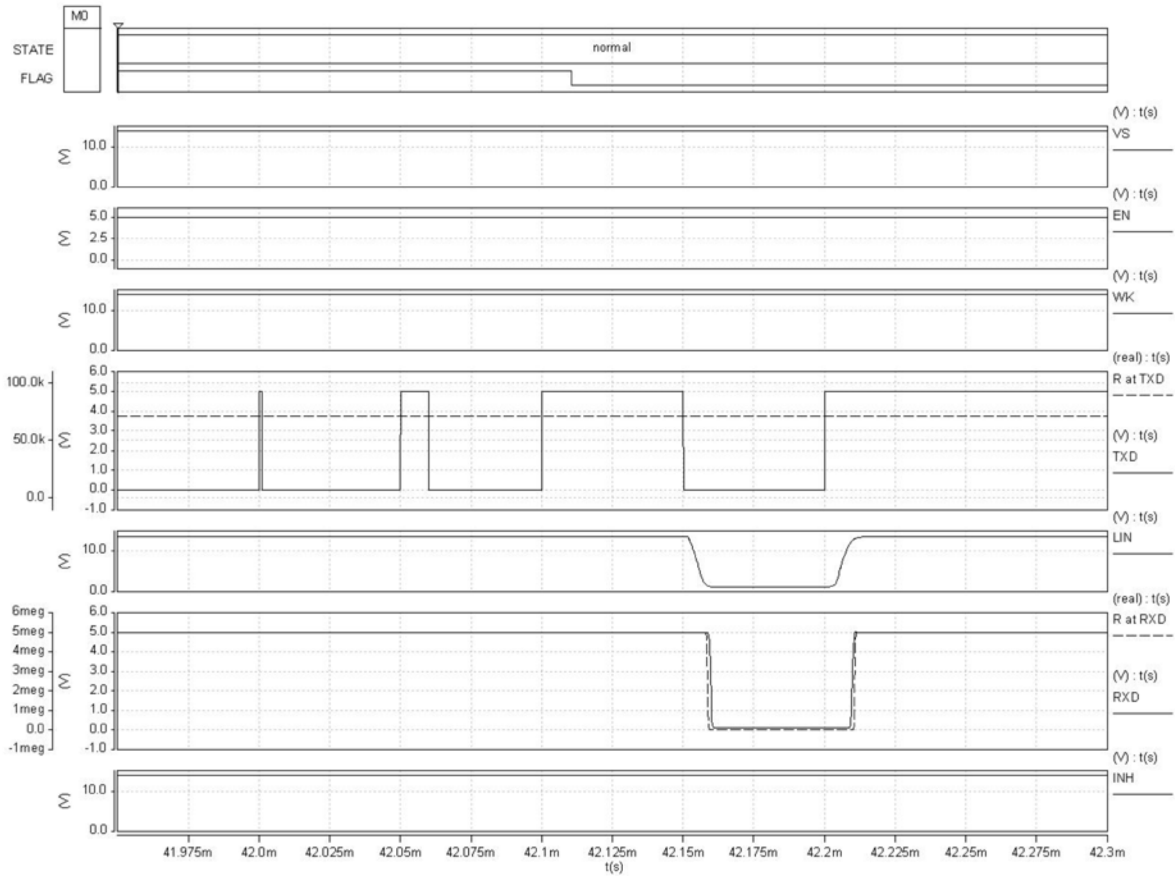
If TxD stays dominant for more than a certain value of time, the output LIN is disabled, going to recessive state to avoid interference in the bus. In Figure 2-11 the resulting behavior of the model is shown, with a flag indicating when the device is disabled.

Figure 2-11. A Detailed View is Shown in Figure 2-12



The TxD signal is monitored during the disabled state for the LIN output. In order to enable the LIN output again, TxD should go recessive and stay for a minimum required time. If TxD goes dominant again before of the required time, the model stays in disabled state. A detailed view of this requirement following the timed-out condition is shown in Figure 2-12 where the flag signal goes down when the device is enabled again.

Figure 2-12. Detailed View of the Enabling Requirement



2.2.4.1 Disabling the LIN Time-out Functionality

With the parameter "use_txd_timeout" it is possible to enable or disable the time-out functionality.

2.3 Diagnosis in Fail-safe Mode

At system power-up, the device automatically starts in fail-safe (FS) mode. LIN communication stays off during this mode. The model stays in FS mode until EN is high. If this happens, the model changes to normal mode (N). In N mode, if EN goes low, the mode is changed to sleep mode (S). While in S mode, a wake-up event switches the IC to fail-safe mode.

When the device change to fail-safe mode, it is possible to know from the periphery why it was change to this mode. This can be done by reading the TxD and RxD pins. Both of them contain pull-down transistors as outputs. During FS mode, the TXD pin is an output and, together with the RXD output pin, signals the FS mode source. The possible sources are shown in Table 2-2 where a wake-up event from sleep mode or an under-voltage condition is signaled to the microcontroller using RXD and TXD pins.

For a wake-up process, the device behaves as described in Section 2.2.3 “Wake-up Modes” on page 8 to Section 2.2.3.3 “Remote Wake-up from Sleep Mode” on page 11.

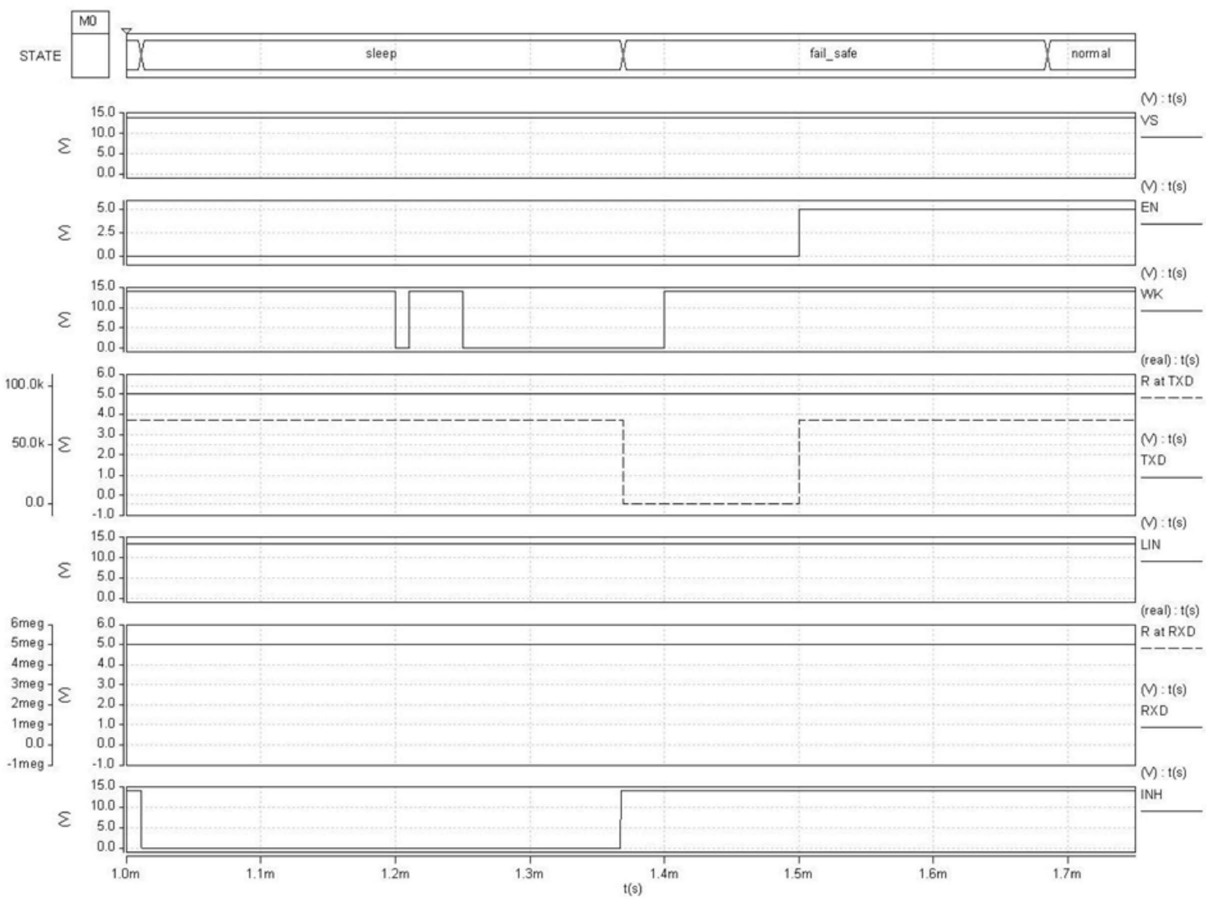
Table 2-2. Fail-safe (Pre-normal) Mode Source Signaling

Fail-safe Sources	TxD	RxD
Remote wake-up (LIN pin)	Low	Low
Local wake-up (EN pin)	High	Low
Local wake-up (WK pin)	Low	High
VS_{th} undervoltage detection (VS < 3.9V)	High	Low

2.3.1 Local Wake-up Signaling (by the WK Pin)

As described in detail in Section 2.2.3.1 “Local Wake-up via WK Pin” on page 8, the following figure shows how the model behaves. For a local wake-up by the WK pin, only TXD goes low during fail-safe mode.

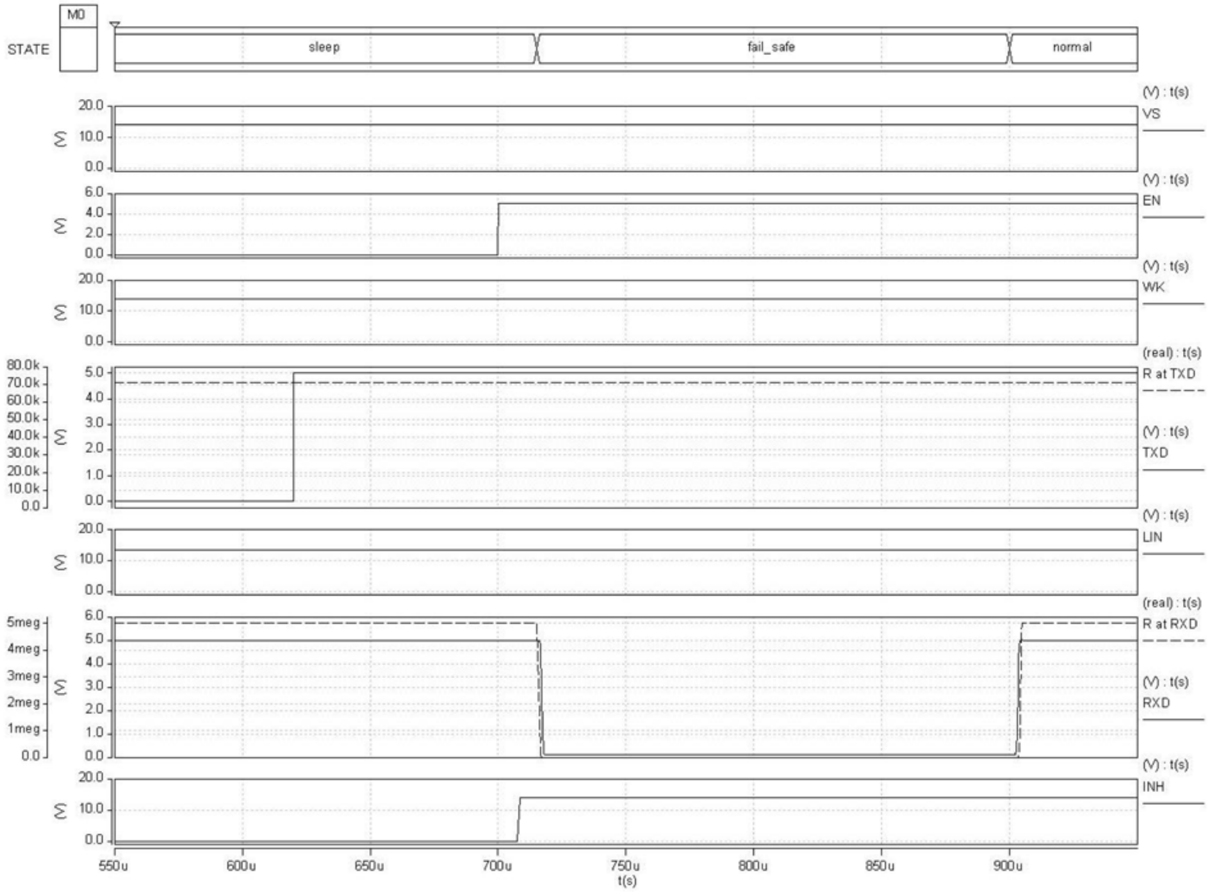
Figure 2-13. Local Wake-up by the WK Pin



2.3.2 Local Wake-up Signaling (by the EN Pin)

If wake-up is generated by the EN pin, RxD goes low and TxD goes high. This is illustrated in Figure 2-14. In addition, no signal is transmitted during sleep or fail-safe mode.

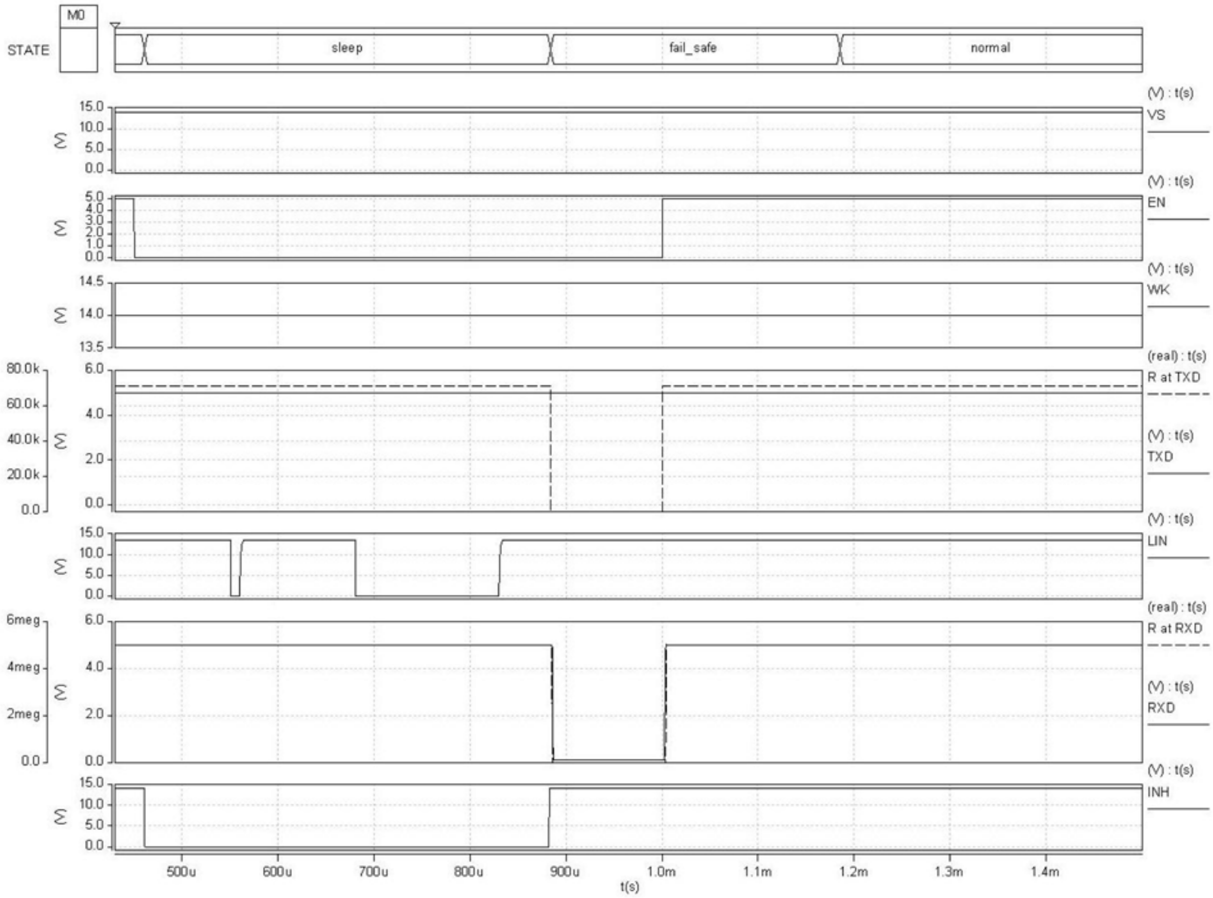
Figure 2-14. Local Wake-up by the EN Pin



2.3.3 Remote Wake-up Signaling

As described in detail in Section 2.2.3.3 "Remote Wake-up from Sleep Mode" on page 11, the following figure show how the model behaves. In Table 2-2 on page 15 both the RxD and the TxD transistors switch down during fail-safe mode. Remote wake-up is achieved when the LIN bus switches and stays low for a certain period before switching up again. This can be seen with the time that changes from "pre-reset" to "reset" when the LIN bus switches down. While the LIN stays down, after a certain time the timer change to "started" and awaits a rise signal. When the LIN bus goes high again, the counter changes to "t_reached" and the wake-up process starts and goes to FS mode.

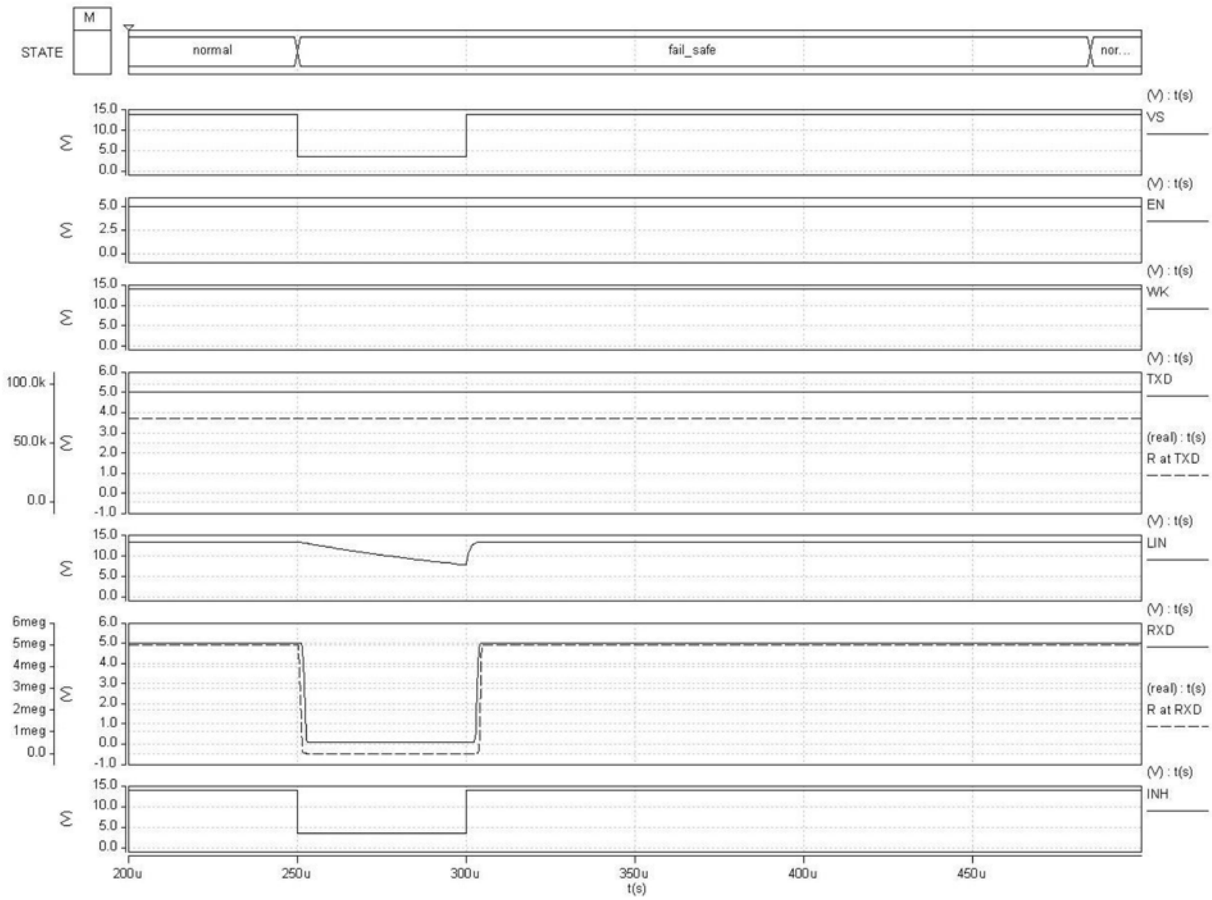
Figure 2-15. Remote Wake-up Process and Signaling



2.3.4 Undervoltage Supply Condition Signaling

Table 2-2 on page 15 shows how the model signals a low supply condition, which automatically triggers fail-safe mode. RXD switches to low only during fail-safe mode. Please note that the LIN switches to low due to the implementation test circuit (Figure 2-1 on page 4) while the INH pin switches off because it has an internal connection to the supply by means of an internal transistor.

Figure 2-16. Low-supply Signaling



2.4 Analogous Behavior

This section shows measured LIN vs. model output LIN signals in order to show the results of the slew rate control and analog output behavior. The test bench circuit is shown in Figure 2-1 on page 4.

The analog behavior mainly depends on two factors: supply level and temperature. This model is designed with a wide range of parameters, some of which are mainly temperature-dependent, while others depend on supply level and some on both factors. In order to achieve a more accurate model while maintaining the most simplicity, the main structure of the parameterization depends on the temperature influence. On the other hand, to reflect dependency on the supply level an internal monitor to the supply level is performed, creating a correction factor to be added to the parameters.

2.4.1 Supply Variation

Many analog behavior parameters depend on the supply level. A test of the model was performed in order to compare the output signals with the measured signals. The model uses a monitor that is able to detect the supply level. With this level a proportional factor is calculated which is linear regarding the supply variation and used to apply a correction factor to the parameters that are affected by the supply level.

In the special case of the slew rate control, it is not possible to implement a linear factor correction as described above. The correlation between the signal shapes and the supply level is not linear. The solution to this special case is to use one value of the parameters involved in the slew rate control portion of the model for each of five different levels of supply. When the supply changes over time, the model is able to compute a linear interpolation between the two nearest points of the actual supply level.

The measuring process was completed with the same load condition as the test bench circuitry shown in Figure 2-1 on page 4. The supply source was changed in five increments: 5, 7, 14, 18 and 28 [V]. In the following section the characteristic of the model for different supplies and the measured signals are shown, however while varying the temperature parameter, i.e., the three possible scenarios low, type and high are described.

2.4.2 Temperature Variation

This model is parameterized into three different modes (high, room and low temperature). Many of the parameters depend on the temperature level. With the high level parameter “Temp,” it is possible to change among the three modes. he parameter is an integer value which can be set to 0 (room temperature and typical values), 1 (high temperature) and –1 (low temperature). In the setup used, 120°C was the high, –40°C the low, and 24°C the room temperature.

A comparison of the measurements and the parameterized model is shown in the following section. See Figure 2-17 on page 20 to Figure 2-26 on page 24 for a broad comparison overview. Figure 2-17 on page 20 to Figure 2-26 on page 24 show the measured LIN signal versus the model output LIN signal. Each figure corresponds to a fixed supply level and only one edge of the signal (falling or rising). In this way it is possible to see the figures for five different levels of supply (5V to 28V), the falling and rising edge for each supply level and the three temperatures (or parameter sets) for each edge. The test bench circuit is shown in Figure 2-1 on page 4 and described in Section 2.1 “Test Circuit” on page 4.

2.4.2.1 Supply = 5V

The three temperature scenarios are shown with a supply level of 5V in the following figures. The model output (SIM LIN) overwrites the measured signals (MSR LIN) with a dashed line.

Figure 2-17. Fall for VS = 5V

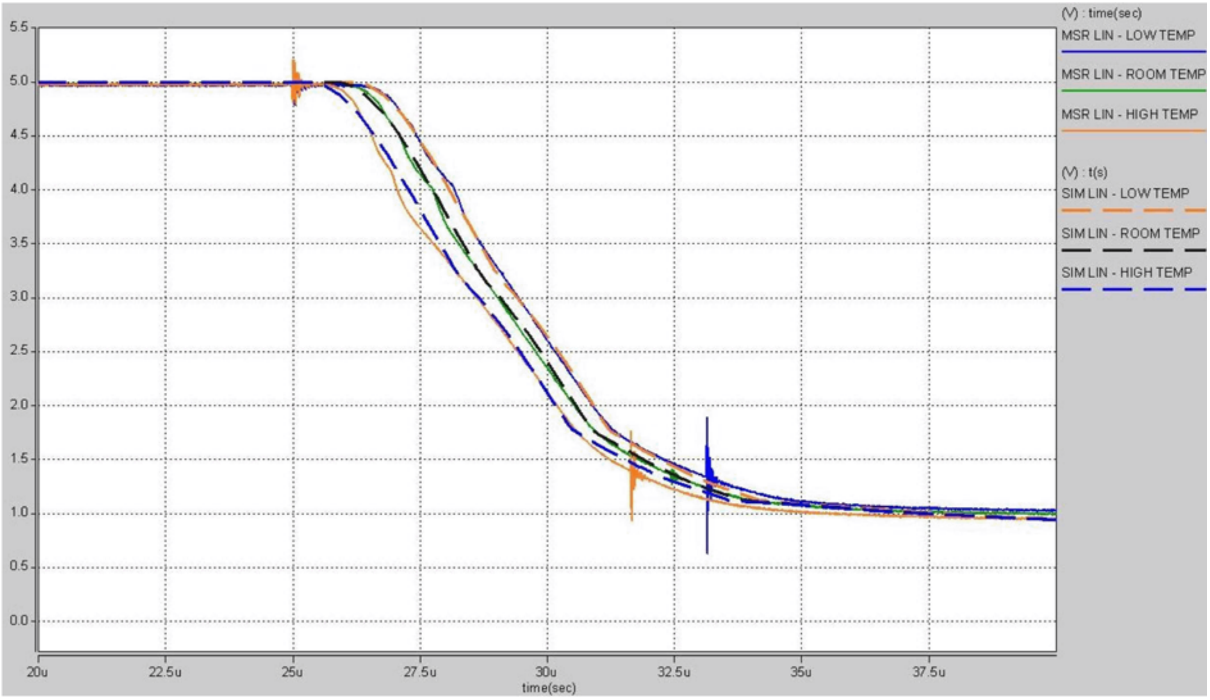
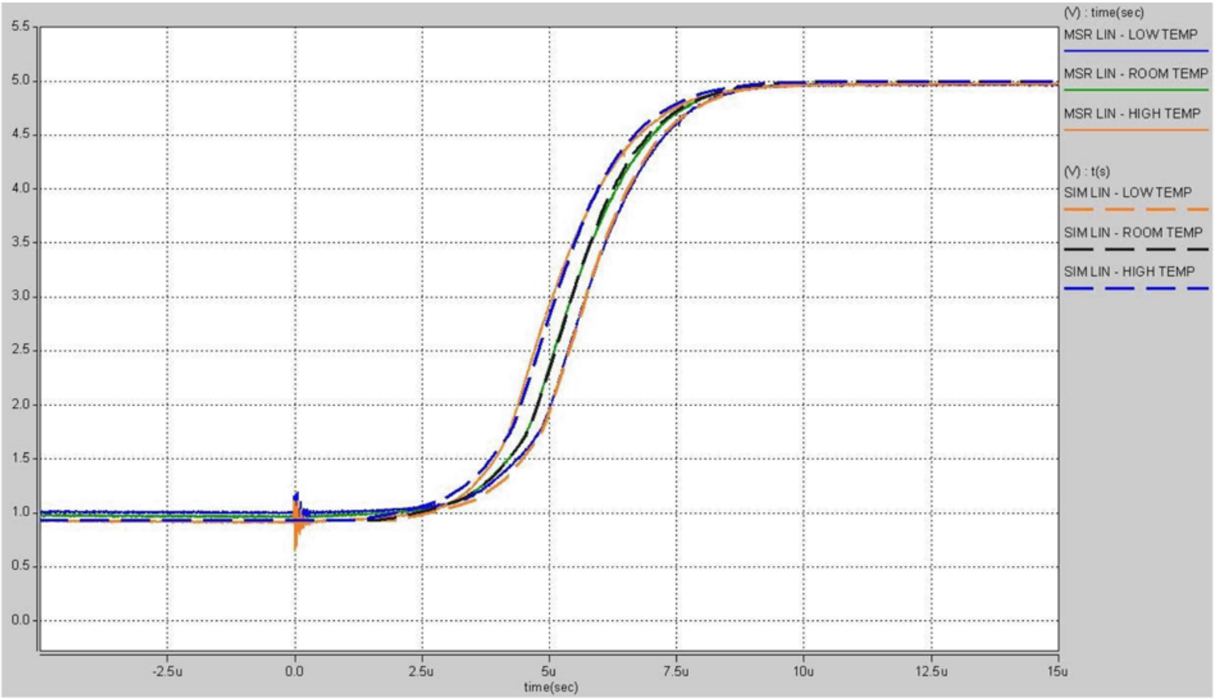


Figure 2-18. Rise for VS = 5V



2.4.2.2 Supply = 7V

The three temperature scenarios are shown with a supply level of 7V in the following figures. The model output (SIM LIN) overwrites the measured signals (MSR LIN) with a dashed line.

Figure 2-19. Fall for VS = 7V

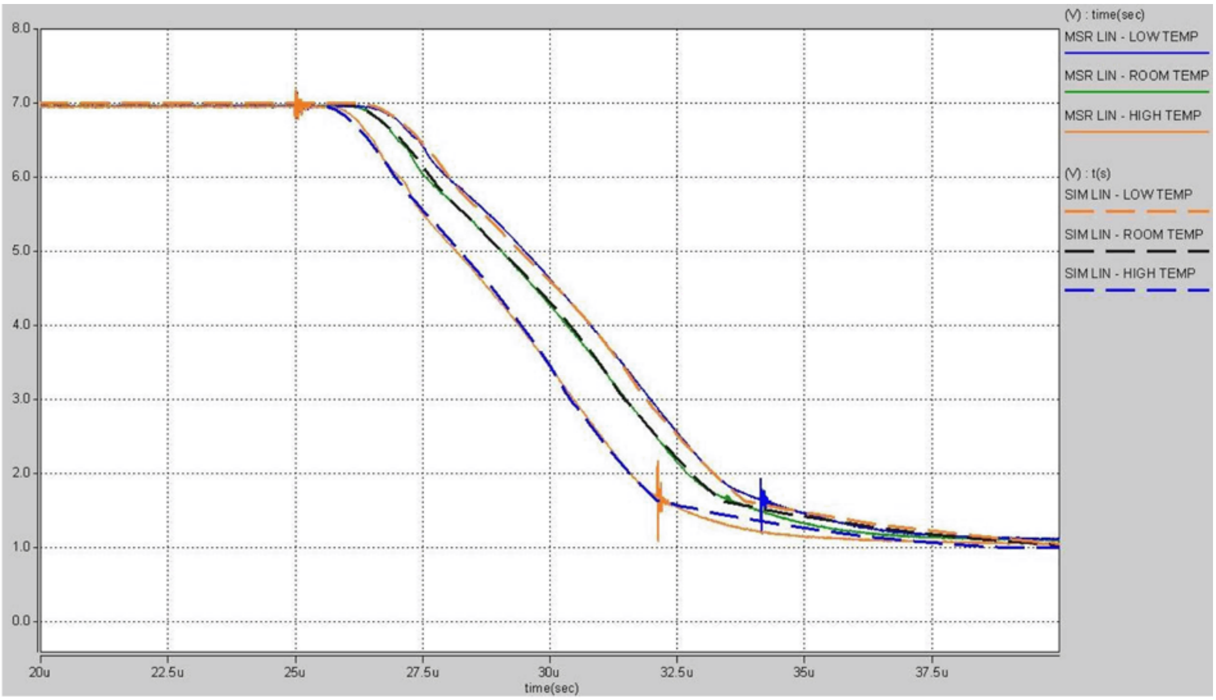
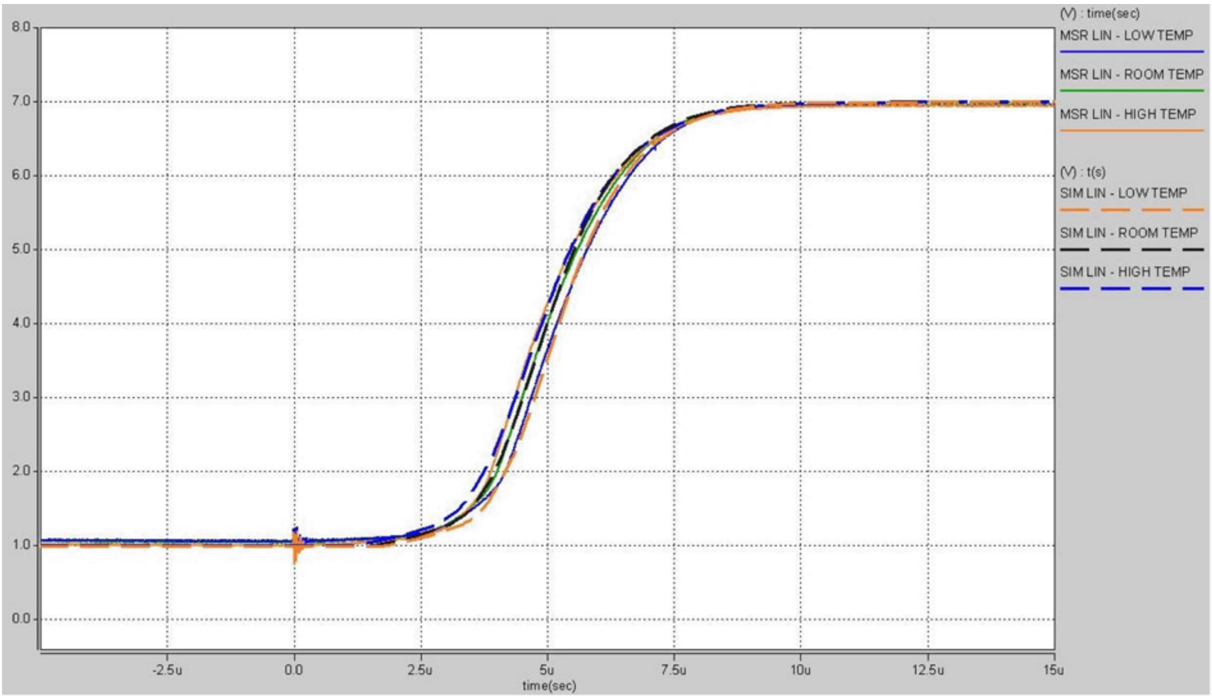


Figure 2-20. Rise for VS = 7V



2.4.2.3 Supply = 14V

The three temperature scenarios are shown with a supply level of 14V in the following figures. The model output (SIM LIN) overwrites the measured signals (MSR LIN) with a dashed line.

Figure 2-21. Fall for VS = 14V

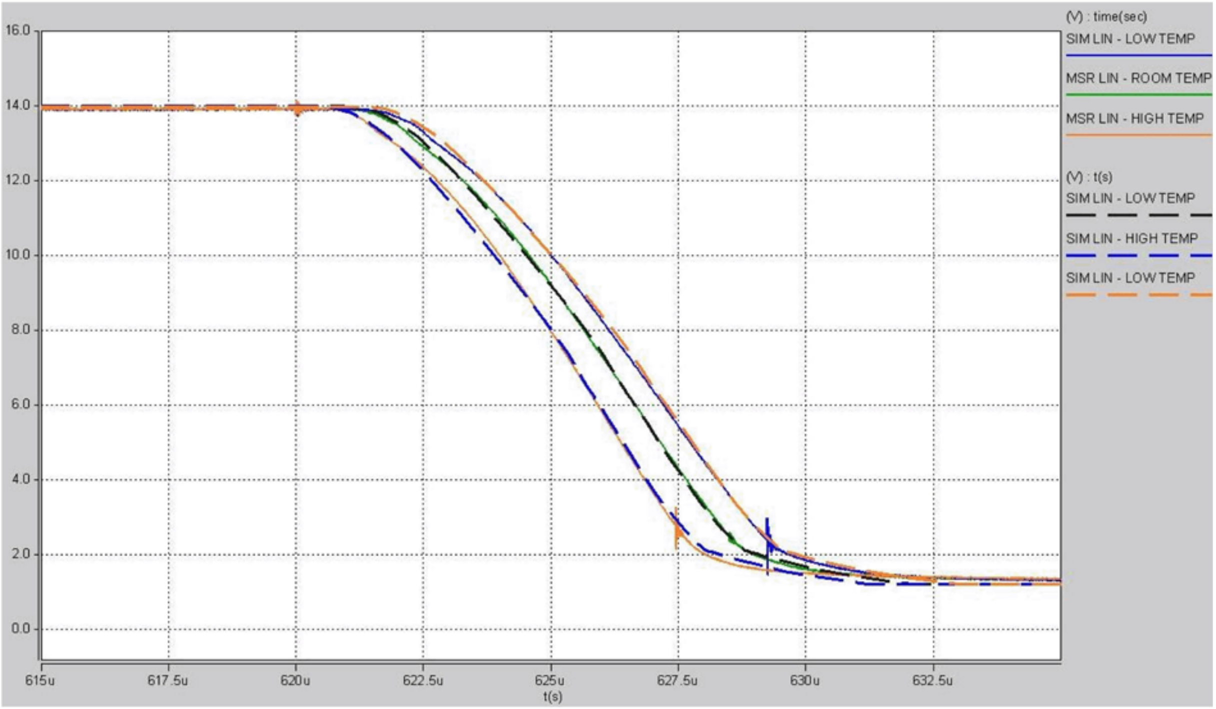
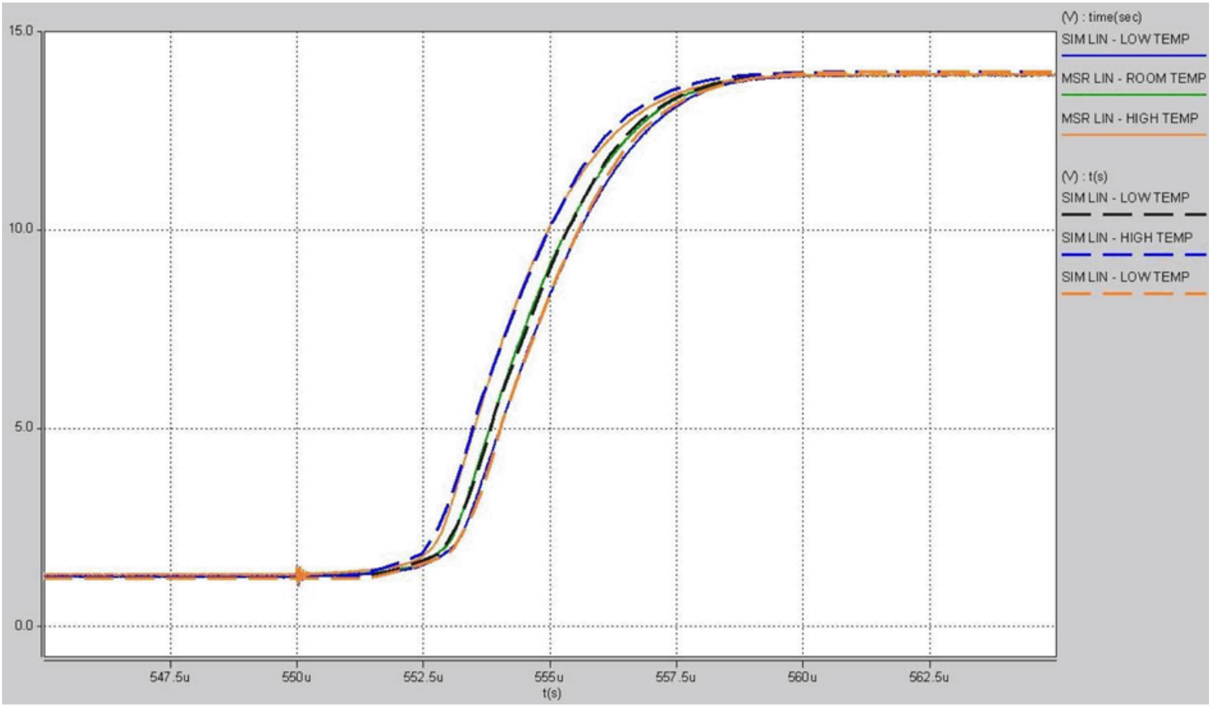


Figure 2-22. Rise for VS = 14V



2.4.2.4 Supply = 18V

The three temperature scenarios are shown with a supply level of 18V in the following figures. The model output (SIM LIN) overwrites the measured signals (MSR LIN) with a dashed line.

Figure 2-23. Fall for VS = 18V

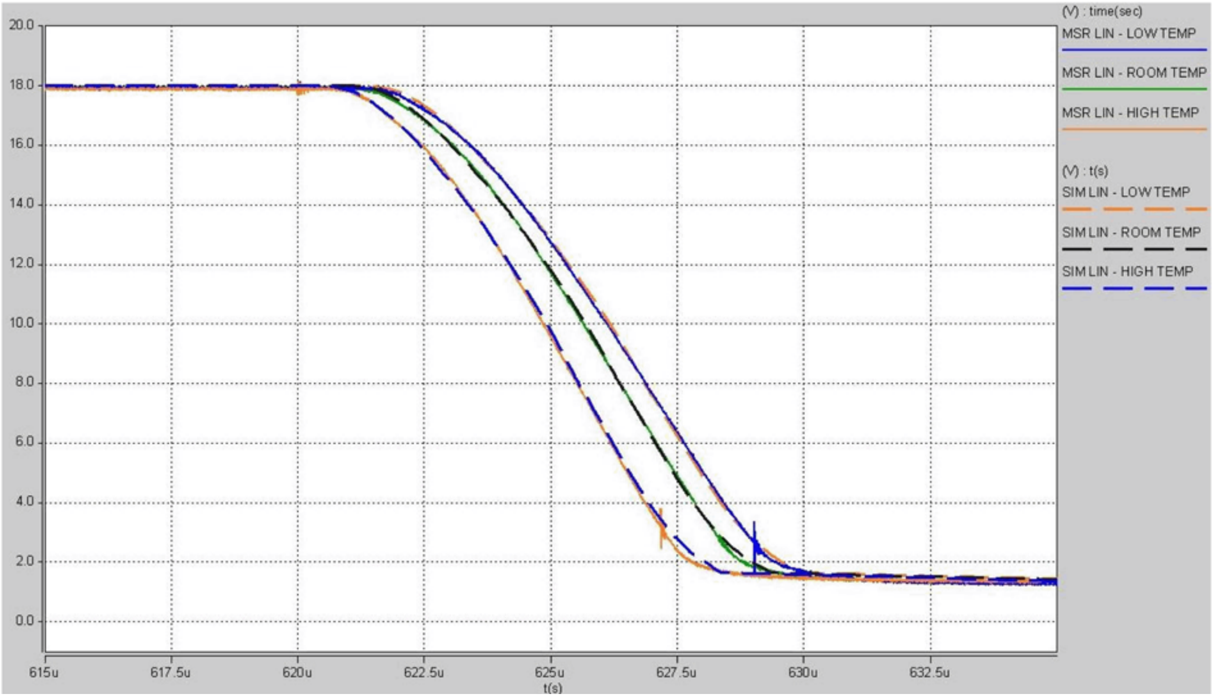
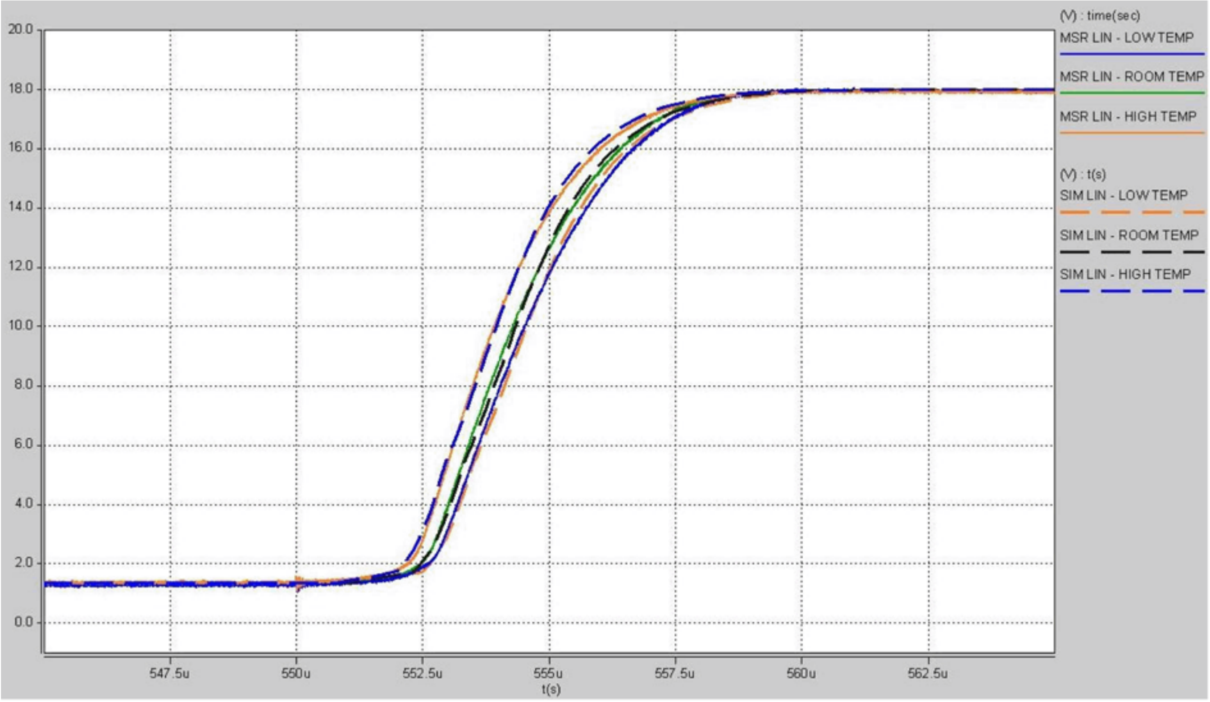


Figure 2-24. Rise for VS = 18V



2.4.2.5 Supply = 28V

The three temperature scenarios are shown with a supply level of 28V in the following figures. The model output (SIM LIN) overwrites the measured signals (MSR LIN) with a dashed line.

Figure 2-25. Fall for VS = 28V

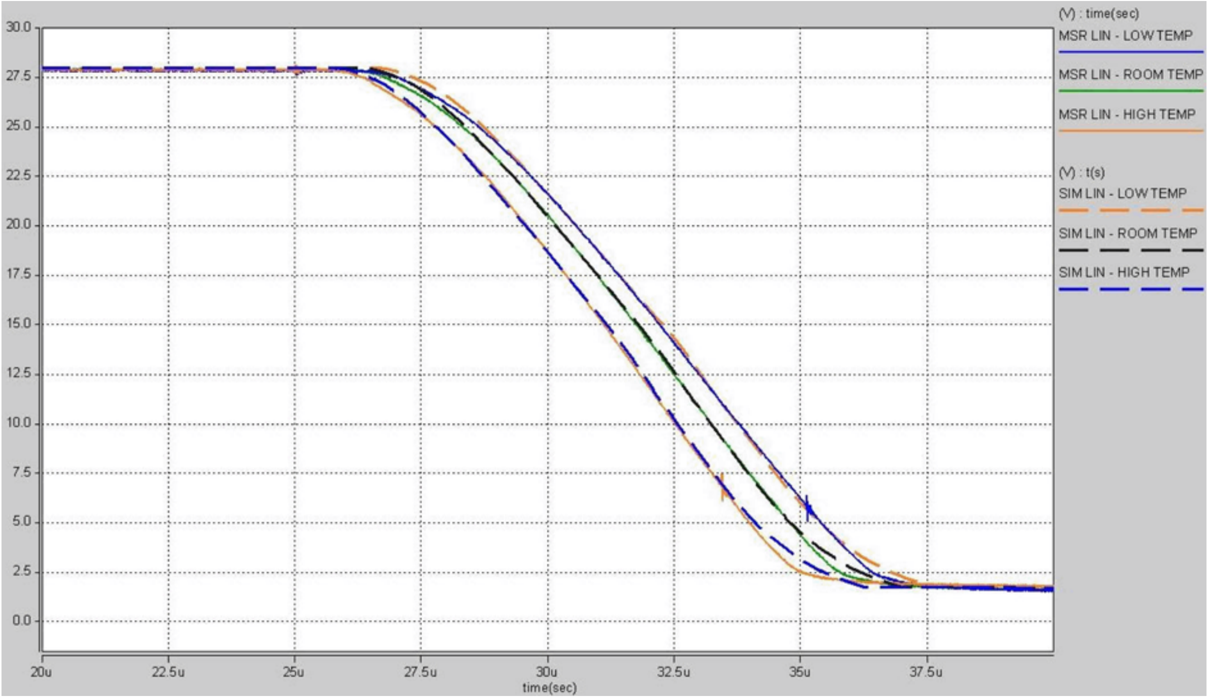
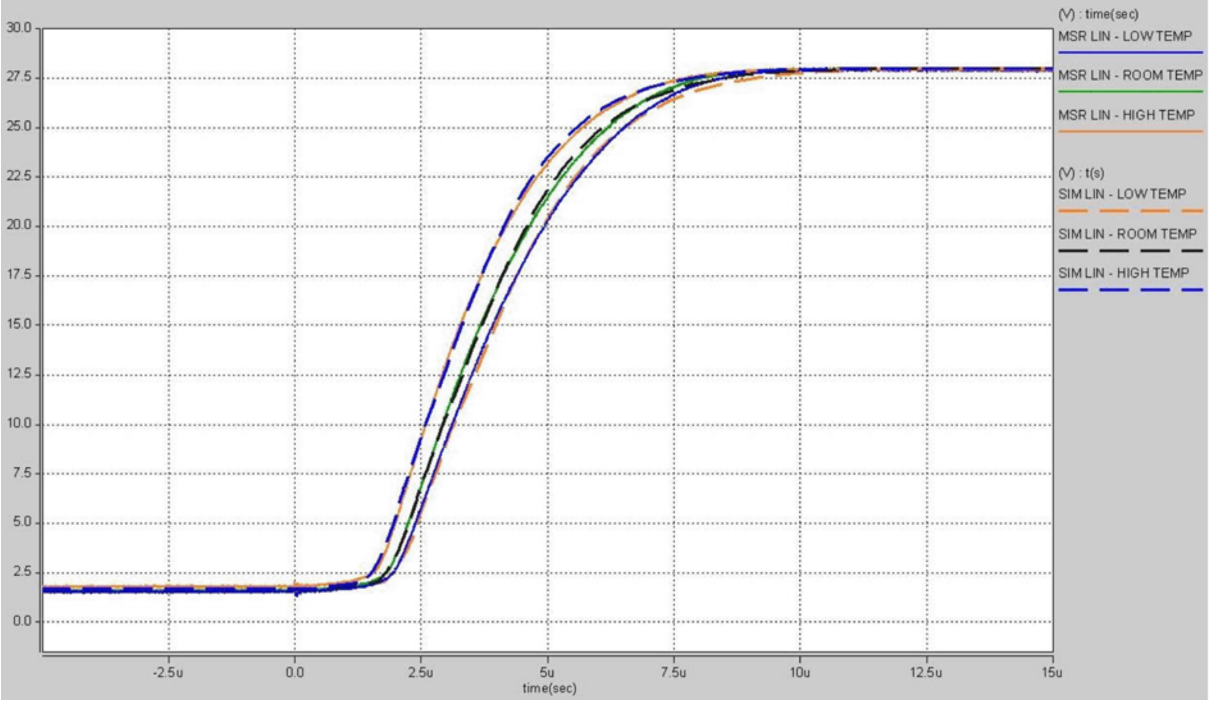


Figure 2-26. Rise for VS = 28V



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