AS8221D

FlexRay Standard Transceiver

Objective DataSheet

1 General Description

This objective data sheet describes the intended functionality of the AS8221 bus transceiver. As long the device is not fully qualified, the parameters are not characterized in the means that parameters may change or can be updated during final product qualification and characterization. This document shows the objective of the AS8221 and this document is subjected to change without notice.

The AS8221 is a high speed automotive bus driver designed according to the FlexRay Electrical Physical Layer Specification V2.1 Rev B. The AS8221 operates as a bi-directional interface between the FlexRay Communication Controller and the twisted-pair copper wiring.

The AS8221 provides an optimized host controller interface consisting of three low-active pins. The Enable and Standby input pins for mode handling by the microcontroller and the Error out pin where system, chip failures or status information are signalled to the microcontroller. Signalling logic high on the Enable and Standby pin the device will enter Normal mode in case no fault condition is given and in this mode the device is fully operational meaning FlexRay communication is possible. Additionally a Receive Only mode is implemented, which can be accessed by the microcontroller where only FlexRay streams can be received in order to avoid unwanted disturbances on the FlexRay bus while listening on the bus traffic. In the low power modes (Standby and Sleep mode) very low power consumption is achieved.

In case of undervoltage on one of the supply voltages (V_{BAT}, $V_{CC}$and V_{IO}) the device will change its mode to a low power mode (either Standby or Sleep mode) and the device will signal an error accordingly. In case of low voltage is detected on both V_{BAT} and V_{CC} the device will enter the Power Off mode, where no operation is possible. A safe mechanism from the low power modes to Power Off mode and vice versa is implemented ensuring that no deadlock can happen during the startup phase.

Ensuring application in safety critical environments a two wire bus-guardian interface is implemented where additional monitoring circuitries on the electronic-control-unit can activate and deactivate the transmitter and additionally on the receive enable output in low power modes the wake conditions and in normal power modes the received FlexRay streams can be monitored.

A thermal sensor circuit with an integral shutdown mechanism prevents damage to the device in extreme temperature conditions. The symmetrical transient control for the high- and low-side driver for both the bus-minus and bus-plus line allows an ideal balance of communications over different network topologies, with excellent EMC performance.

2 Key Features

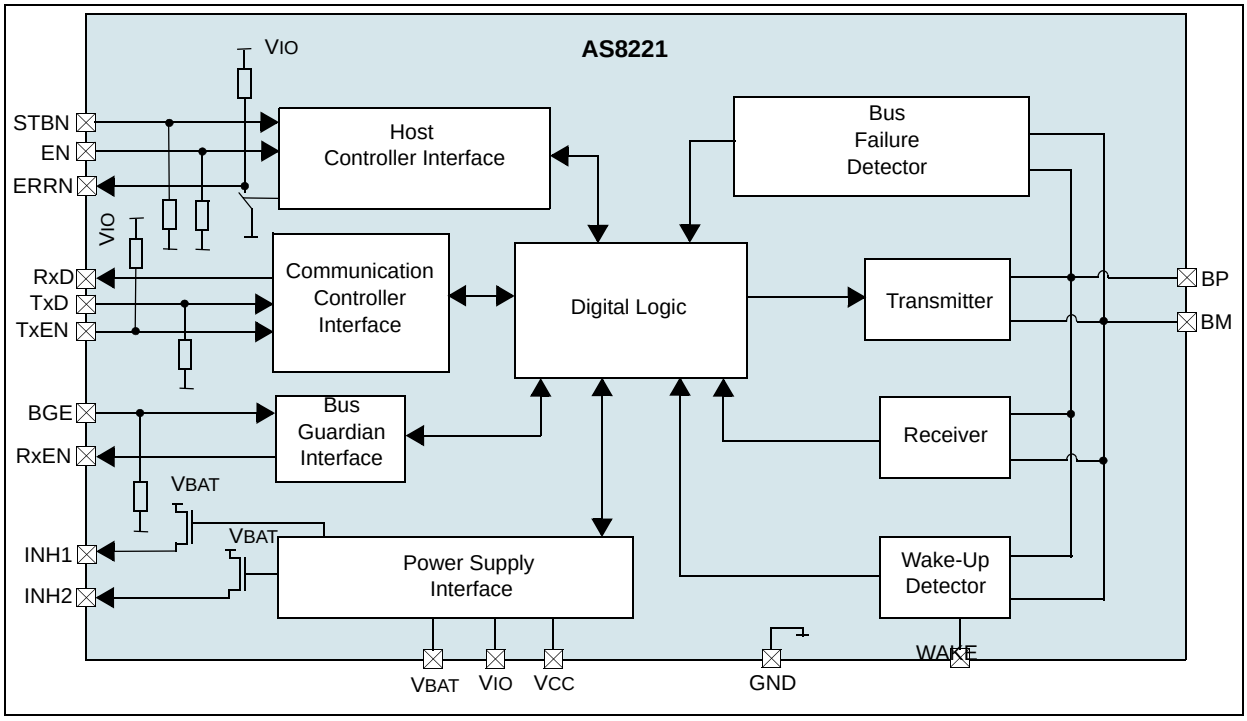
- Compliant with FlexRay Electrical Physical Layer Specification V2.1 Rev. B
- Data transfer up to 10 Mbps
- Excellent EMC performances. High common mode range insure excellent EMI
- Interface for Bus Guardian or supervision circuits
- Automatic thermal shutdown protection
- Supports 12V and 24V systems with very low sleep current
- Integrated power management system
  - Two inhibit pins for external voltage supply control
  - Local wake-up input
  - Remote wake-up capability via FlexRay bus in low power modes
- Supports 2.5, 3, 3.3, 5 V microcontrollers and automatically adapts to interface levels
- Protection against damage due to short circuit conditions on the bus (positive and negative battery voltage)
- Operating temperature range -40ºC to +125ºC
- Lead-free SSOP20 package

3 Applications

The AS8221 FlexRay Standard Transceiver is best fitting for all automotive applications where the full functionality of the FlexRay bus driver is needed in the electronic-control-unit like bus wake-up and control for voltage supplies.

The device addresses all ECUs connected to the permanent battery supply (clamp 30). The AS8221 is connected to the battery voltage and therefore can be used as the only ECU wake-up component with very low power consumption in Sleep mode.

Figure 1. Block Diagram



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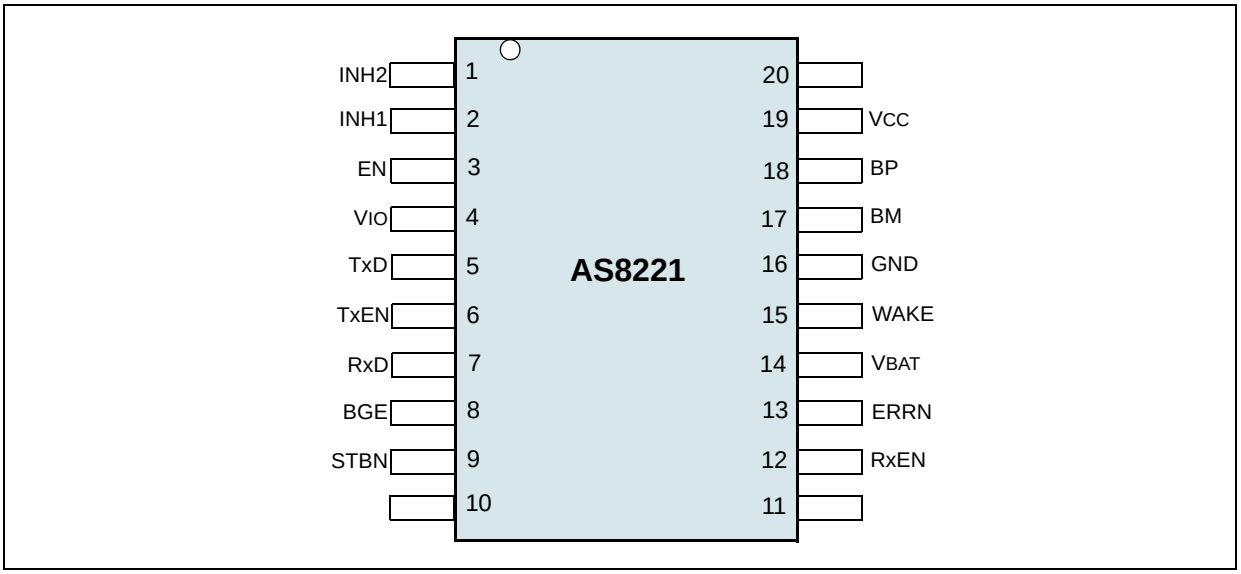
4 Pin Assignments

Figure 2. Pin Assignments SSOP20 Package



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
INH2	1	**Analog Output.** Inhibit 2 output for switching external voltage regulator
INH1	2	**Analog Output.** Inhibit 1 output for switching external voltage regulator
EN	3	**Digital Input.** Enable input
VIO	4	**Supply Voltage.** I/O supply voltage
TxD	5	**Digital Input.** Transmit data input
TxEN	6	**Digital Input.** Transmitter enable input
RxD	7	**Digital Output.** Receive data output
BGE	8	**Digital Input.** Bus guardian enable input
STBN	9	**Digital Input.** Standby input
Not used	10	
Not used	11	
RxEN	12	**Digital Output.** Receive data enable output
ERRN	13	**Digital Output.** Error diagnosis output and wake status output
VBAT	14	**Supply Voltage.** Battery supply voltage
WAKE	15	**Analog Input.** Local wake-up input
GND	16	**Ground**
BM	17	**Analog Input/Output.** Bus line Minus
BP	18	**Analog Input/Output.** Bus line Plus
VCC	19	**Supply voltage.**
Not used	20	

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Battery Supply Voltage (V_{BAT})	-0.3	+50	V	
Supply Voltage (V_{CC})	-0.3	+7.0	V	
Supply Voltage (V_{IO})	-0.3	+7.0	V	
DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-0.3	V_{IO} + 0.3	V	$V_{IO} < V_{CC}$
DC Voltage on pin WAKE, INH1, INH2	-0.3	V_{BAT} + 0.3		
DC Voltage at BP and BM	-40	+50	V	
Input current (latchup immunity)	-100	100	mA	According to JEDEC 78
Electrostatic discharge at bus lines BP, BM, V_{BAT}, WAKE	-4	+4	kV	According to AEC-Q100-002
Electrostatic discharge	-2	+2	kV	According to AEC-Q100-002
Transient voltage on BP, BM	-200	+200	V	According to ISO7637 part3 test pulses a and b; class C; RL=45 W, CL= 100 pF; (see Figure 20 on page 34).
Transient voltage on V_{BAT}	-200	+200	V	According to ISO7637 part2 test pulses 1, 2, 3a and 3b; class C; RL=45 W, CL= 100 pF; (see Figure 20 on page 34).
	+6.5	+50	V	According to ISO7637 part2 test pulse 4; class C; RL=45 W, CL= 100 pF; (see Figure 20 on page 34).
		+50		According to ISO7637 part2 test pulse 5b; class C; RL=45 W, CL= 100 pF; (see Figure 20 on page 34).
Total power dissipation (all supplies and outputs)		150	mW	
Storage temperature	-55	+150	ºC	
Junction temperature	-40	+150	ºC	
Package body temperature[1]		250	ºC	
Humidity non-condensing	5	85	%	

1. The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

T_{vj} = -40 to +150 ºC, V_{CC} = +4.75V to +5.25V, V_{BAT}= 6.5 to +50 V, V_{IO} = +2.2 to V_{CC}, R_L= 45Ω, C_L= 100 pF unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage						
T_{amb}	Ambient temperature		-40		+125	ºC
V_{CC}-V_{IO}	Difference of supplies		-0.1		3.05	V
I_{BAT}	V_{BAT} current consumption	V_{BAT}=12V; Low Power Mode[1] T_{vj} < 125ºC	0		30	µA
		V_{BAT}=12V; Low Power Mode[1] T_{vj} < 150ºC	0		50	µA
		Non Low Power Mode	0		1	mA
I_{CC}	V_{CC} current consumption	Low Power Mode[1] V_{CC} = 0V to +5.25V	-5		20	µA
		Non Low Power Mode: NORMAL, driver enabled;	0		45	mA
		Non Low Power Mode: NORMAL, driver enabled; R_{BUS} = ∞Ω	0		15	mA
		Non Low Power Mode: RECEIVE ONLY	0		10	mA
I_{IO}	V_{IO} current consumption	Low Power Mode[1] V_{IO} = 0V to +5.25V	-5		5	µA
		Non Low Power Mode	0		1	mA
State Transitions						
t_{STBN_RxD}	Delay STBN high to RxD high with wake flag set		1		50	µs
t_{STBN_RxEN}	Delay STBN high to RxEN high with wake flag set		1		50	µs
t_{SLEEP_INH1}	Delay STBN high to INH1 high	INH1 high = 80% V_{BAT}	1		50	µs
$t_{STANDBY\_INH2}$	Delay STBN high to INH2 high	INH2 high = 80% V_{BAT}	1		50	µs
t_{SLEEP}	go-to-sleep hold time	INH1 low = 20% V_{BAT}	10		70	µs
Transmitter						
$V_{BUS\_DIFF\_D0}$	Differential bus voltage low in NORMAL mode (Data0)	$V_{BPdata0}$ - $V_{BMdata0}$; 40Ω < R_L < 55Ω	-2		-0.6	V
$V_{BUS\_DIFF\_D1}$	Differential bus voltage high in NORMAL mode (Data1)	$V_{BPdata1}$ - $V_{BMdata1}$; 40Ω < R_L < 55Ω	0.6		2	V
ΔV_{BUS_DIFF}	Matching between Data0 and Data1 differential bus voltage in NORMAL mode	$V_{BUS\_DIFF\_D0}$ - $V_{BUS\_DIFF\_D1}$ 40Ω < R_L < 55Ω	-200		200	mV
$V_{BUS\_COM\_D0}$	Common mode bus voltage in case of Data0 in non low power modes	$V_{BPdata0}$/2 + $V_{BMdata0}$/2 40Ω < R_L < 55Ω	0.4 * V_{CC}		0.6 * V_{CC}	V

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{BUS\_COM\_D1}$	Common mode bus voltage in case of Data1 in non low power modes	$V_{BPdata1}/2 + V_{BMdata1}/2$ $40\Omega < R_L < 55\Omega$	0.4 * Vcc		0.6 * Vcc	V
ΔV_{BUS_COM}	Matching between Data0 and Data1 common mode voltage	$V_{BUS\_COM\_D0} - V_{BUS\_COM\_D1}$ $40\Omega < R_L < 55\Omega$	-200		200	mV
$V_{BUS\_DIFF\_Idle}$	Absolute differential bus voltage in idle mode				30	mV
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute max current when BP is shorted to BM	$V_{BP}=V_{BM}$			+100	mA
$IBP_{GNDShortMax}$	Absolute max current when BP is shorted to GND	V_{BP}= 0V			+100	mA
$IBM_{GNDShortMax}$	Absolute max current when BM is shorted to GND	V_{BM}= 0V			+100	mA
$IBP_{-5VShortMax}$	Absolute max current when BP is shorted to -5 V	V_{BP}= -5V			+100	mA
$IBM_{-5VShortMax}$	Absolute max current when BM is shorted to -5 V	V_{BM}= -5V			+100	mA
$IBP_{27VShortMax}$	Absolute max current when BP is shorted to 27 V	V_{BP}= 27V			+100	mA
$IBM_{27VShortMax}$	Absolute max current when BM is shorted to 27 V	V_{BM}= 27V			+100	mA
$IBP_{48VShortMax}$	Absolute max current when BP is shorted to 48 V	V_{BP}= 48V			+100	mA
$IBM_{48VShortMax}$	Absolute max current when BM is shorted to 48 V	V_{BM}= 48V			+100	mA
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	t_{TxD_RISE} = 5ns			50	ns
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	t_{TxD_FALL} = 5ns			50	ns
$t_{TxD\_MISMATCH}$	Delay time from TxD to BUS mismatch	$t_{TxD\_BUS10} - t_{TxD\_BUS01}$	-4		4	ns
t_{BUS10}	Fall time differential bus voltage	80% - 20% of V_{BUS}	3.75		18.75	ns
t_{BUS01}	Rise time differential bus voltage	20% - 80% of V_{BUS}	3.75		18.75	ns
$t_{TxEN\_BUS\_Idle\_Active}$	Delay time from TxEN to bus active				50	ns
$t_{TxEN\_BUS\_Active\_Idle}$	Delay time from TxEN to bus idle				50	ns
$t_{TxEN\_MISMATCH}$	Delay time from TxEN to bus mismatch	$\lvert t_{TxEN\_BUS\_Idle\_Active} - t_{TxEN\_BUS\_Active\_Idle} \rvert$			50	ns
$t_{BGE\_BUS\_Idle\_Active}$	Delay time from BGE to bus active				50	ns
$t_{BGE\_BUS\_Active\_Idle}$	Delay time from BGE to bus idle				50	ns
$t_{BUS\_Idle\_Active}$	Differential bus voltage transition time: idle to active				30	ns

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{BUS\_Active\_Idle}$	Differential bus voltage transition time: active to idle				30	ns
$t_{TxEN\_timeout}$	TxEN timeout		0.64		3.07	ms
Receiver						
R_{BP}, R_{BM}	BP, BM input resistance	Idle mode; R_{BUS}=∞	10		40	KΩ
R_{DIFF}	BP, BM differential input resistance	Idle mode; R_{BUS}=∞	20		80	KΩ
V_{BPidle}, V_{BMidle}	Idle voltage in non low power modes on pin BP, BM	Non low power modes; V_{TxEN} = V_{IO}	0.4* V_{CC}	0.5* V_{CC}	0.6* V_{CC}	V
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in low power modes on pin BP, BM	Low power modes	-0.2	0	+0.2	V
I_{BPidle}	Absolute idle output current on pin BP	-40V < V_{BP} < 50V	0		7.5	mA
I_{BMidle}	Absolute idle output current on pin BM	-40V < V_{BM} < 50V	0		7.5	mA
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	V_{BP} = V_{BM} = 5V, V_{CC} = 0V, V_{BAT} = 0V; V_{IO} = 0V	0		+10	uA
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	Normal power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM}) < 15V	150	225	400	mV
$V_{BUSActiveLow}$	Activity detection differential input voltage low	Normal power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM})< 15V	-400	-225	-150	mV
V_{Data1}	Data1 detection differential input voltage	Pre-condition: activity already detected. Normal power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM})< 15V	150	225	300	mV
V_{Data0}	Data0 detection differential input voltage	Pre-condition: activity already detected. Normal power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM})< 15V	-300	-225	-150	mV
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	$2 \times (\lvert \lvert V_{Data0} \rvert - \lvert V_{Data1} \rvert \rvert) / (\lvert V_{Data0} \rvert + \lvert V_{Data1} \rvert)^2$			10	%
$V_{RECEIVE\_COM}$	Max. common mode voltage range when receiving	Normal power modes	-10		+15	V
t_{BUS_RxD10}	Delay from BUS to RxD negative edge	C_{RxD} = 15 pF [3]			80	ns
t_{BUS_RxD01}	Delay from BUS to RxD positive edge	C_{RxD} = 15 pF [3]			80	ns
t_{BIT}	Bit time	C_{RxD} = 15 pF [3]	54			ns
t_{RxD_ASYM}	Delay time from BUS to RxD mismatch	C_{RXD}=15 pF; $\lvert t_{BUS\_RxD10} - t_{BUS\_RxD01} \rvert$ [3]			5	ns

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RxD_FALL}	Fall time RxD voltage	80% - 20% of V_{RxD}; C_{RxD}=15 pF [3]			5	ns
t_{RxD_RISE}	Rise time RxD voltage	20% - 80% of V_{RxD}; C_{RxD}=15 pF [3]			5	ns
$t_{BUSIdleDetection}$	Idle detection time	V_{BUS}: 400mV → 0V	50		200	ns
$t_{BUSActivitiyDetection}$	Activity detection time	V_{BUS}: 0V → 400mV	100		250	ns
$t_{BUSIdleReaction}$	Idle reaction time	V_{BUS}: 400mV → 0V	50		300	ns
$t_{BUSActivityReaction}$	Activity reaction time	V_{BUS}: 0V → 400mV	100		350	ns
Wake-Up Detector						
t_{BWU_D0}	Data0 detection time in remote wake-up pattern	-10V < (V_{BP}, V_{BM}) < 15V	1		4	µs
t_{BWU_Idle}	Idle or Data1 detection time in remote wake-up pattern	-10V < (V_{BP}, V_{BM}) < 15V	1		4	µs
t_{BWU_Detect}	Total remote wake-up detection time	-10V < (V_{BP}, V_{BM}) < 15V	48		140	µs
V_{BWUTH}	Bus wake-up detection threshold	-10V < (V_{BP}, V_{BM}) < 15V	-300		-150	mV
V_{LWUTH}	Local wake-up detection threshold		-2		4	V
I_{LWUL}	Low level input current on local WAKE pin	V_{BAT} = 12V; V_{LWAKE} = 2V for t < $t_{LWUFilter}$	-20		-5	µA
I_{LWUH}	High level input current on local WAKE pin	V_{BAT} = 12V; V_{LWAKE} = 4V for t < $t_{LWUFilter}$	5		20	µA
$t_{LWUFilter}$	Local wake filter time		1		40	µs
Supply Voltage Monitor						
V_{BATTHH}	V_{BAT} undervoltage recovery threshold		3.5		4.5	V
V_{BATTHL}	V_{BAT} undervoltage detection threshold		2.5		3.5	V
V_{CCTHH}	V_{CC} under-voltage recovery threshold		3.5		4.5	V
V_{CCTHL}	V_{CC} undervoltage detection threshold		2.5		3.5	V
V_{IOTHH}	V_{IO} undervoltage recovery threshold		1.25		2.0	V
V_{IOTHL}	V_{IO} undervoltage detection threshold		0.75		1.5	V
t_{UV_DETECT}	Detection time for undervoltage at V_{BAT}, V_{CC}, V_{IO}		100		700	ms
t_{UV_REC}	Detection time for undervoltage recovery at V_{BAT}, V_{CC}, V_{IO}		0.7		5	ms
Bus Error Detection						
I_{THL}	Absolute bus current for low current detection	NORMAL mode, Transmitter enabled		5		mA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{THH}	Absolute bus current for high current detection	NORMAL mode, Transmitter enabled		40		mA
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	NORMAL mode, Transmitter enabled		225		mV
t_{BUS_ERROR}	Bus error detection time	NORMAL mode, Transmitter enabled		20		µs
Over Temperature						
OT_{TH}	Over temperature threshold		150		180	ºC
OT_{TL}	Over temperature hysteresis		10		20	ºC
Power Supply Interface						
ΔV_{OINH}	High level voltage drop on INH1, INH2	I_{INH} = 0.2mA, V_{BAT} = 5.5V	0		0.8	V
$\lvert I_{IL} \rvert$	Leakage current	SLEEP mode, V_{INH} = 0V			5	µA
Communication Controller Interface						
V_{TxDIH}	Threshold for detecting TxD as on logical high				0.7* V_{IO}	V
V_{TxDIL}	Threshold for detecting TxD as on logical low		0.3* V_{IO}			V
I_{TxDIH}	TxD high level input current		30		100	µA
I_{TxDIL}	TxD low level input current		-5		5	µA
V_{TxENIH}	Threshold for detecting TxEN as on logical high				0.7* V_{IO}	V
V_{TXENIL}	Threshold for detecting TxEN as on logical low		0.3* V_{IO}			V
I_{TxENIH}	TxEN high level input current		-5		5	µA
I_{TxENIL}	TxEN low level input current		-100		-30	µA
V_{RxDOH}	RxD high level output voltage	I_{RxD} = -4mA, V_{IO} = 5V	0.8* V_{IO}		1.0* V_{IO}	V
V_{RxDOL}	RxD low level output voltage	I_{RxD} = 4mA, V_{IO} = 5V	0		0.2* V_{IO}	V
Host Interface						
V_{STBNIH}	Threshold for detecting STBN as on logical high				0.7* V_{IO}	V
V_{STBNIL}	Threshold for detecting STBN as on logical low		0.3* V_{IO}			V
I_{STBNIH}	STBN high level input current		30		100	µA
I_{STBNIL}	STBN low level input current		-5		5	µA
$t_{STBN\_DEB\_LP}$	STBN de-bouncing time low power modes		0.1		40	µs
$t_{STBN\_DEB\_NLP}$	STBN de-bouncing time non low power modes		0.1		2	µs

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ENIH}	Threshold for detecting EN as on logical high				0.7* V_{IO}	V
V_{ENIL}	Threshold for detecting EN as on logical low		0.3* V_{IO}			V
I_{ENIH}	EN high level input current		30		100	µA
I_{ENIL}	EN low level input current		-5		5	µA
$t_{EN\_DEB\_LP}$	EN de-bouncing time low power modes		0.1		40	µs
$t_{EN\_DEB\_NLP}$	EN de-bouncing time non low power modes		0.1		2	µs
V_{ERRNOH}	ERRN high level output voltage	I_{ERRN} = -4mA, V_{IO} = 5V	0.8* V_{IO}		1.0* V_{IO}	V
V_{ERRNOL}	ERRN low level output voltage	I_{ERRN} = 4mA, V_{IO} = 5V	0		0.2* V_{IO}	V
Bus Guardian Interface						
V_{BGEIH}	Threshold for detecting BGE as on logical high				0.7* V_{IO}	V
V_{BGEIL}	Threshold for detecting BGE as on logical low		0.3* V_{IO}			V
I_{BGEIH}	BGE high level input current		30		100	µA
I_{BGEIL}	BGE low level input current		-5		5	µA
V_{RxENOH}	RxEN high level output voltage	I_{RxEN} = -4mA, V_{IO} = 5V	0.8* V_{IO}		1.0* V_{IO}	V
V_{RxENOL}	RxEN low level output voltage	I_{RxEN} = 4mA, V_{IO} = 5V	0		0.2* V_{IO}	V
Read Out Interface						
$t_{RO\_EN\_ERRN}$	Propagation delay falling edge EN to ERRN				4.5	µs
$t_{RO\_EN\_TIMEOUT}$	Error read out time out		25		100	µs

1. EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN, LWAKE, INH1, INH2: open
2. Test condition: (V_{BP} + V_{BM}) / 2 = 2,5V ± 5%
3. For test signal (see Figure 18)

7 Typical Operating Characteristics

Figure 3.

Figure 4.

Figure 5.

Figure 6.

Figure 7.

Figure 8.

8 Detailed Description

The AS8221 is a high-speed fault tolerant device operating as an interface between a generic controller and the copper wire physical bus. The AS8221 is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The drivers are short circuit protected against the positive and negative supply voltage to increase the robustness and reliability of automotive systems. The AS8221 operates at baudrates up to 10 Mbps to increase the bandwidth for automotive applications.

Block Description

The electrical AS8221 high-speed bus-system transceiver is the interface between a FlexRay™ network node module and the channel. The transceiver provides differential transmit and receive capability to the bus, allowing the node module bidirectional time multiplexed binary data stream transfer. Besides the transmit and receive function, the transceiver provides low power management, supply voltage monitoring (under voltage detection) as well as bus failure detection and represents a ESD-protection barrier between the bus and the ECU.

The AS8221 consists of 9 different functional blocks(see Figure 1):

Table 4. Functional Blocks

Functional Block	Short Description
Host Controller Interface (HCI)	Digital interface between the transceiver and the host controller (HC) The host interface comprises the read out handler, which delivers failure and status information via the ERRN pin to the host controller.
Communication Controller Interface (CCI)	Digital interface between the transceiver and the FlexRay communication controller (CC)
Bus Guarding Interface (BGI)	Digital interface between the transceiver and the FlexRay bus guardian (BG)
Power Supply Interface (PSI)	The power supply interface consists of an sub functional block, the voltage monitor (VM) and includes two analogue inhibit outputs for signalling the internal state of the transceiver
Internal Logic (IL)	The digital signals from the functional blocks of the device are fed into the internal logic where the forwarding of FlexRay messages from analogue side to digital interfaces and vice versa is done. The state machine is performed in this block and is dealing the error, wake and power-on flags.
Bus Failure Detector (BFD) Temperature Protection (TP)	The bus failure detector is directly connected to the bus pins, in order to detect several external failure conditions which may occur on the bus. The temperature protection turns off the output driver when reaching the specified internal temperature in order to protect the device.
Transmitter	The transmitter provides the bus signals as specified on the bus lines.
Receiver	The receiver captures FlexRay valid signals on the bus lines and provides received data streams to the internal logic
Wake-Up Detector (WUD)	The wake-up detector recognizes valid wake-up frames on the bus, recognizes a wake signal on the local WAKE pin and signals valid wake-up events to the internal logic.

Events

Transitions in order to change between the operation modes are possible only when events are detected. The device supports three type of events, events on the host controller interface (STBN, EN), detection of undervoltage or supply voltage recovery, and detected wake events. Whenever an event is recognized, a transition can be performed.

Operating Modes

The AS8221 provides the following operating modes:

- NORMAL: non low power mode
- RECEIVE ONLY: non low power mode

- STANDBY: low power mode
- GO TO SLEEP: low power mode
- SLEEP: low power mode

NORMAL mode

In this mode the transceiver is able to send and receive data signals on the bus. TxEN and BGE control the state of the transmitter. INH1 and INH2 outputs are set high. RxD reflects the bus data and reflect the bus state. The error read out mechanism is enabled. In this mode, the transmitter state can be selected as shown in the Table 5. In case the over-temperature flag is set the transmitter is disabled. The bus wires are terminated to Vcc/2 via receiver input resistances.

Table 5. Transmitter State

BGE	TxEN	TxD	Transmitter state	Bus State
H	L	H	Enabled	Data1 (BP is driven high, BM is driven low)
H	L	L	Enabled	Data0 (BP is driven low, BM is driven High)
X	H	X	Disabled	Idle (BP and BM are not driven)
L	X	X	Disabled	Idle (BP and BM are not driven)

- If the differential bus voltage is higher than $V_{BUSActivehigh}$ or lower than $V_{BUSActivelow}$ for a time longer than $t_{BUSActivityDetection}$, then activity is detected on the bus (Bus = active), RxEN is switched to logical “low” and RxD is released.
- If, after the activity detection, the differential bus voltage is higher than V_{Data1}, RxD is high.
- If, after the activity detection, the differential bus voltage is lover than V_{Data0}, RxD is low.
- If the absolute differential bus voltage is lower than $V_{BUSActivehigh}$ and higher than $V_{BUSActivelow}$ for a time longer than $t_{BUSIdleDetection}$, then idle is detected on the bus (Bus = idle), RxEN and RxD are switched to logical “high”

RECEIVE ONLY mode

In this mode the transceiver has the same behaviour as in NORMAL mode but the transmitter is disabled.

STANDBY mode

In this mode the transceiver is not able to send and receive data signals from the bus, but the wake-up detector is active. The power consumption is significantly reduced respect the non low power operation modes. RxD and RxEN, reflects the negation of the wake-up flag. INH1 is set to high. If wake-up flag is set then INH2 is high, otherwise it is floating. The error read out mechanism is not enabled. The bus wires are terminated to GND (bus state: Idle_LP).

GO TO SLEEP mode

In this mode the transceiver has the same behavior as in STANDBY mode but if this mode is selected for a time longer than t_{SLEEP} and the wake flag is cleared the device enters into the SLEEP mode.

SLEEP mode

In this mode the transceiver has the same behaviour as in STANDBY mode but INH1 and INH2 are floating.

Non Operating Mode

The AS8221 provides the following non operating mode:

POWER OFF

In this mode the transceiver is not able to operate. RxD, RxEN are set to high and ERRN is set to low. INH1 and INH2 are floating. The bus wires are not connected to GND (bus state: Idle_HZ).

Undervoltage Events

Undervoltage V_{BAT}

When V_{BAT} voltage falls below V_{BATTHL} for a time longer than t_{UV_DETECT} then the undervoltage V_{BAT} flag is set and it is reset when V_{BAT} exceeds the voltage threshold V_{BATTHH} for a time longer than t_{UV_REC} or in case a wake-up event has been detected. The flag can be set or reset in all the modes.

Undervoltage V_{IO}

When V_{IO} voltage falls below V_{IOTHL} for a time longer than t_{UV_DETECT} then the undervoltage V_{IO} flag is set and it is reset when V_{IO} exceeds the voltage threshold V_{IOTHH} for a time longer than t_{UV_REC} or in case a wake-up event has been detected. The flag can be set or reset in all the operation modes. The flag is reset at POWER OFF.

Undervoltage V_{CC}

When V_{CC} voltage falls below V_{CCTHL} for a time longer than t_{UV_DETECT} then the undervoltage V_{CC} flag is set and it is reset when V_{CC} exceeds the voltage threshold V_{CCTHH} for a time longer than t_{UV_REC} or in case a wake-up event has been detected. The flag can be set or reset in all the operation modes. The flag is reset at POWER OFF.

Power On/Off Events

- Starting from POWER OFF mode a power on event occurs in case V_{BAT} undervoltage flag is reset.
- Starting from every operation mode a power off event occurs in case V_{BAT} and V_{CC} undervoltage flags are set.

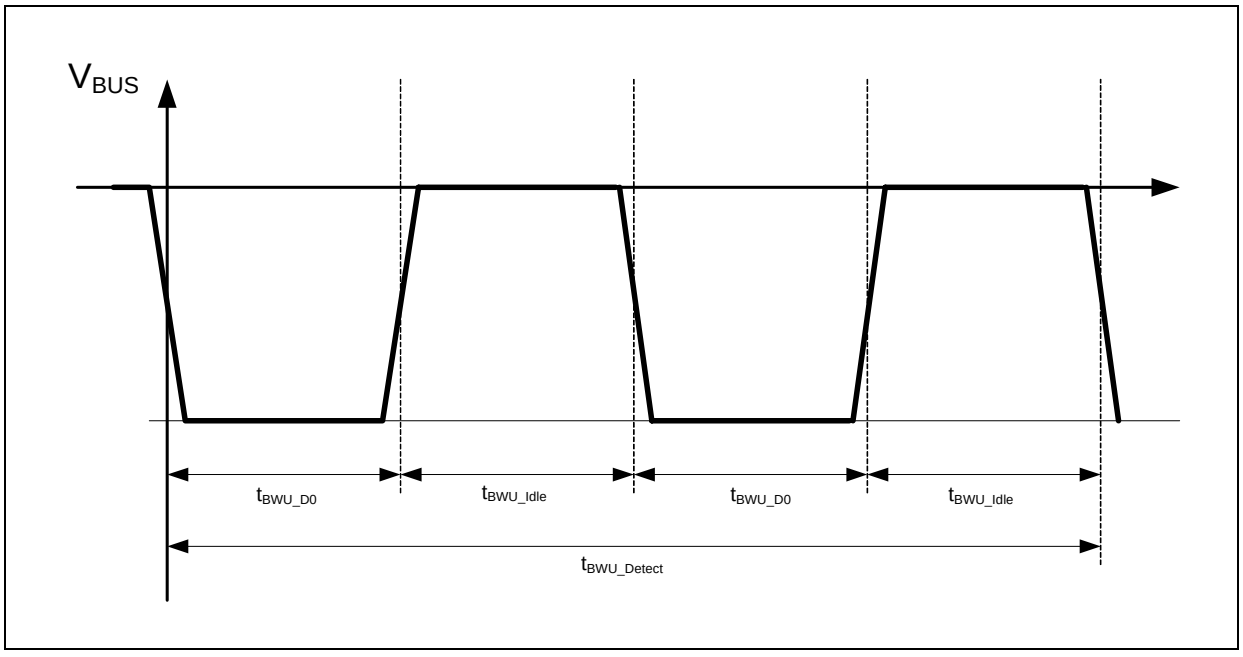
Wake-Up Events

A wake-up event can be detected only in low power modes. The wake-up flag is set when the remote or local wake flag is set. The wake-up flag is reset when the remote and local wake-up flags are reset. The remote wake-up flag is set if a remote wake-up event occurs. The local wake-up flag is set if a local wake-up event occurs. The remote and local wake-up flags are reset entering a low power mode from a non low power mode, entering NORMAL mode, whenever an undervoltage event occurs and at POWER OFF.

Remote Wake-Up event

A remote wake-up event, only possible in low power mode, consists in the reception of at least two consecutive wake-up symbols via the bus within t_{BWU}. The wake-up symbol is defined as Data0 longer than tBWU0 followed by idle or Data1 longer than $t_{BWUidle}$ as in Figure 9 unless an undervoltage or wake-up event is present.

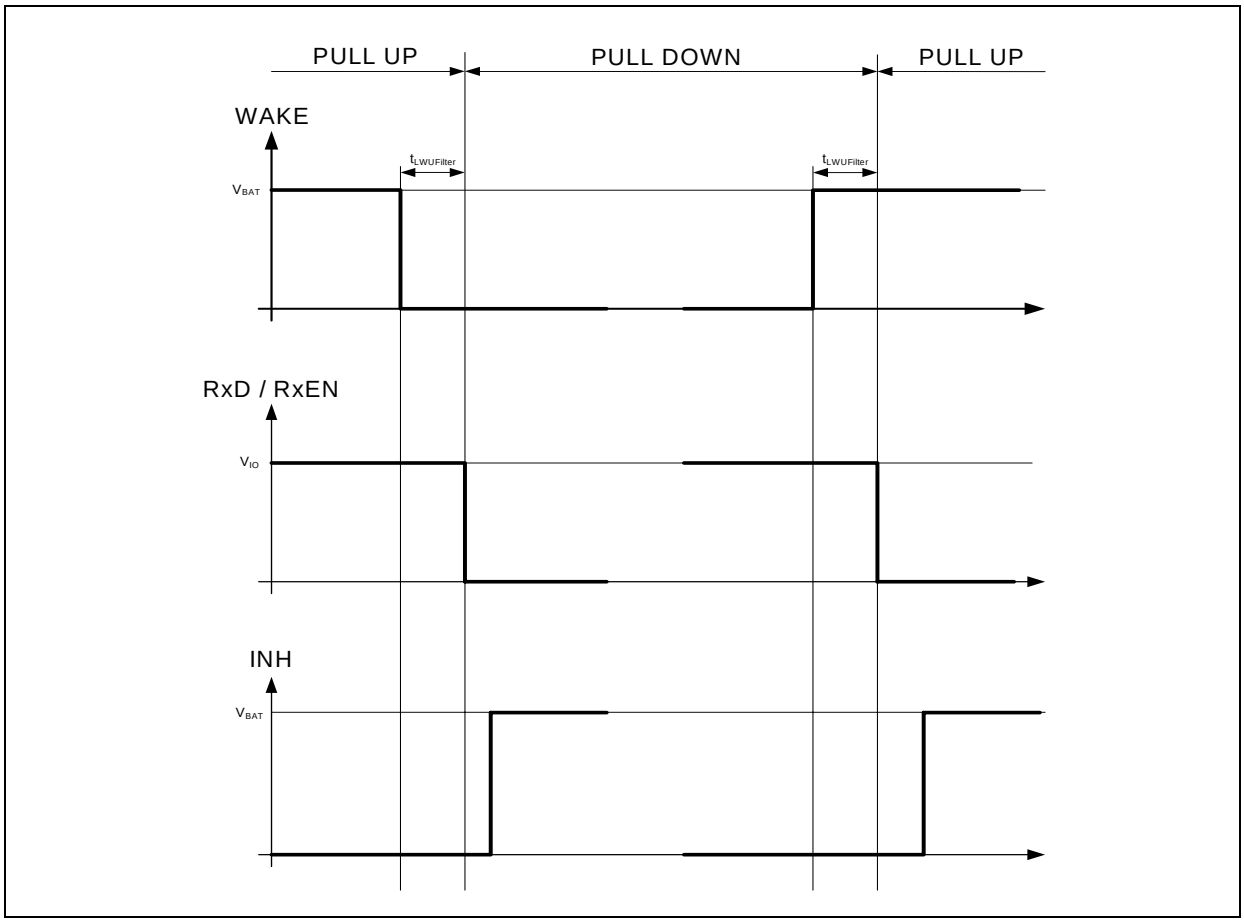
Figure 9. Signal for wake-up pattern recognition



Local Wake-Up Event

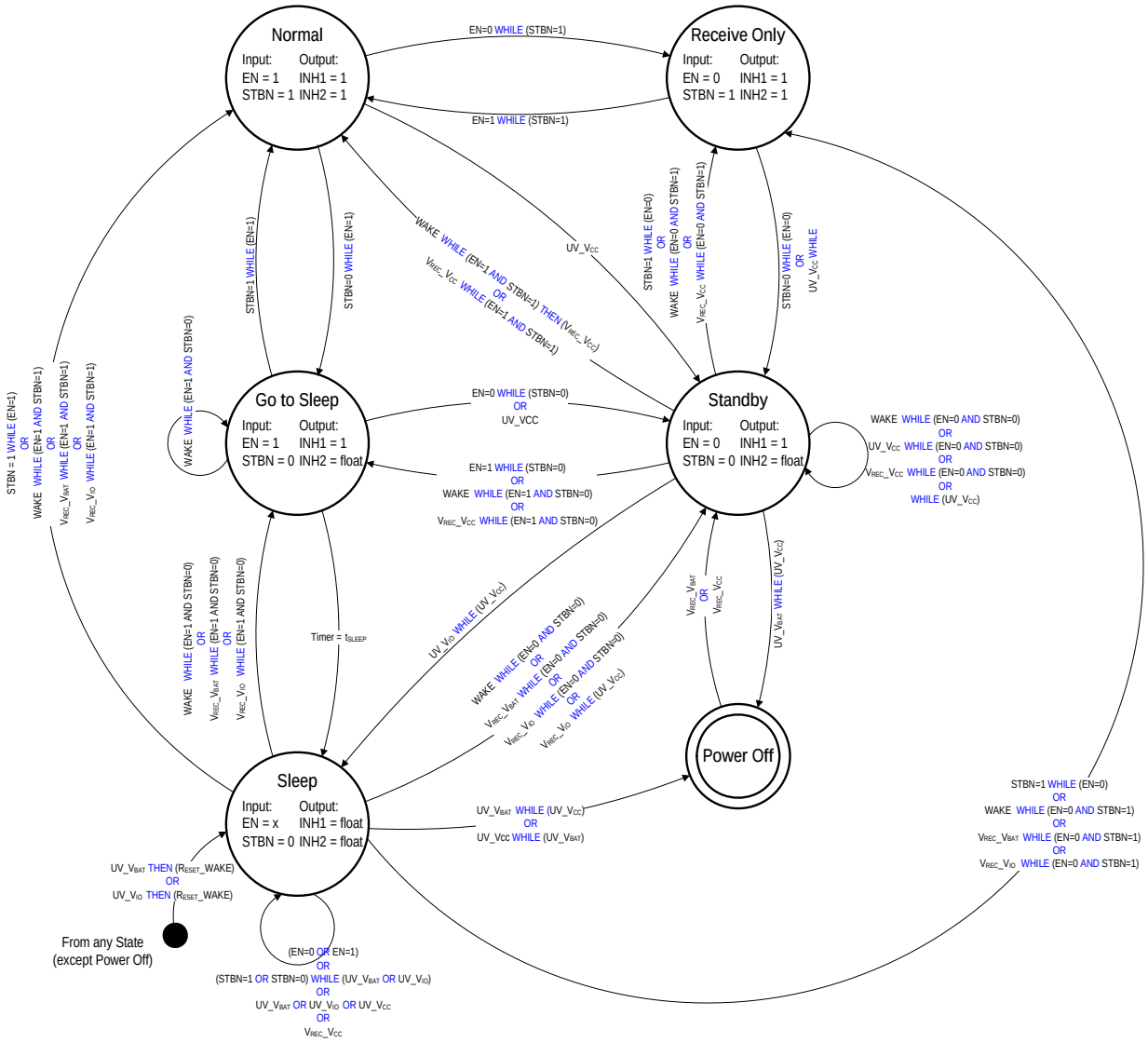
In all low power modes, if the voltage on the WAKE pin falls below V_{LWUTH} for longer than $t_{LWFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-down. If the voltage on the WAKE pin rises above V_{LWUTH} for longer than $t_{LWFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-up. The pull up and down mechanism is also active in non low power modes.

Figure 10. WAKE input pin behavior



System Description

Figure 11. State Diagram



Note: This state diagram does not include all transitions, which are shown in Table 7

Prefix of "WHILE" is always the event and suffix in brackets checks the flags or in case of EN and STBN the input condition. For example: V_{REC}_VBAT WHILE (EN=0 AND STBN=0)

After the event VBAT supply voltage recovery is detected, the transition is performed if EN and STBN are "low".

Legend:

UV_VBAT: Undervoltage event and/or flag for VBAT supply voltage

UV_V_{IO}: Undervoltage event and/or flag for VIO supply voltage

UV_V_{CC}: Undervoltage event and/or flag for VCC supply voltage

V_{REC}_VBAT: Voltage recovery event and/or flag for VBAT supply voltage

V_{REC}_V_{IO}: Voltage recovery event and/or flag for VIO supply voltage

V_{REC}_V_{CC}: Voltage recovery event and/or flag for VCC supply voltage

Wake: Wake event and/or flag

Fail Silent Behavior

In order to be fail silent, undervoltage detection on the three power supplies V_{BAT}, V_{IO} and V_{CC} is implemented

- V_{BAT}**:** Battery supply voltage
- V_{IO}**:** Supply voltage for I/O digital level adaptation
- V_{CC}**:** Supply voltage (+5V)

State transitions due to under voltage detection

- In case of V_{BAT} or V_{IO} undervoltage is detected, SLEEP mode will be entered regardless of the voltage present on pins EN and STBN.
- In case V_{CC} undervoltage is detected, STANDBY mode will be entered regardless of the voltage present on pins EN and STBN.
- V_{BAT} and V_{IO} undervoltage detection have higher priority than V_{CC} undervoltage detection.
- In case V_{BAT} and V_{CC} undervoltage are detected, POWER OFF mode is entered (bus state: Idle_HZ).

State transitions due to voltage recovery detection

- If the undervoltage recovers the device will enter the mode determined by the voltages at pins EN and STBN.
- Starting from the Power Off, the device enters the state indicated by the host input pins (EN, STBN) only when V_{BAT} or V_{CC} recovers ($V_{BAT} \geq V_{BATTHH}$ or $V_{CC} \geq V_{CCTHH}$) while V_{IO} is available (undervoltage flag of V_{IO} flag not set). If the V_{IO} undervoltage flag is set, the STANDBY mode will be entered. In both cases the Power On flag is set.
- When $V_{BAT} \leq V_{BATTHL}$ and $V_{CC} \leq V_{CCTHL}$ the device is in power off state and the bus wires are not terminated (bus state: Idle_HZ).

Wake-Up Mechanism

The wake-up detector is active in all low power modes. In case a remote o local wake-up occurs the V_{BAT}, V_{IO}, V_{CC} undervoltage flags are reset, the wake-up flag is set, INH outputs are switched on and the device enters the state indicated by the host pins.

Remote Wake-Up

A remote wake-up event or bus wake-up event is the reception of at least two consecutive wake-up symbols via the bus within t_{BWU}. The wake-up symbol is defined as Data0 longer than tBWU0 followed by idle or Data1 longer than $t_{BWUIdle}$.

Mode Transitions

Starting from every operation mode the device enters POWER OFF in case a power off event occurs regardless the V_{IO} undervoltage flag, the wake-up flag and the host input pins (EN, STBN) state.

Starting from the POWER OFF the device enters STANDBY only in case a power on event occurs.

Starting from every operation mode the device enters SLEEP in case V_{BAT} or V_{IO} undervoltage flag is set regardless the V_{CC} undervoltage flag, the wake-up flag and the host input pins state.

Starting from every operation mode except SLEEP the device enters STANDBY in case V_{CC} undervoltage flag is set and V_{BAT} and V_{IO} undervoltage flags are not set, regardless the wake-up flag indication and the host input pins state.

Starting from a low power mode the device enters the operation mode indicated by the host input pins if a wake-up event occurs.

In case all the undervoltage flags are reset the operation mode is selected by the wake-up flag and the host pins according to Table 6.

Table 6. Pin Signalling and Operating modes

Inputs		Operation Mode	OutPut				
STBN	**EN**		**RxD**	**ERRN**	**RxEN**	**INH1**	**INH2**
H	H	NORMAL	L Bus = Data_0	not (Error flag)	L Bus = Active	H	H
			H Bus = Idle or Data_1		H Bus = Idle		
H	L	RECEIVE ONLY	L Bus = Data_0	not (Error flag)	L Bus = Active	H	H
			H Bus = Idle or Data_1		H Bus = Idle		
L	H	GO TO SLEEP	not (Wake-up flag)	not (Wake-upake-up flag)	not (Wake-up flag)	H	Float
L	L	STANDBY	not (Wake-up flag)	not (Wake-up flag)	not (Wake-up flag)	H	Float
L	X	SLEEP	not (Wake-up flag)	not (Wake-up flag)	not (Wake-up flag)	Float	Float
X	X	POWER OFF	H	L	H	Float	Float

Where: H = Digital level high

L = Digital level low

x = Do not care

Float = The analog output is not driven

Note: If GO TO SLEEP is selected for more than t_{SLEEP} then the device will enter SLEEP only if the wake-up flag is not set otherwise it will remain in GO TO SLEEP.

If wake-up flag is set INH2=H otherwise INH2=floating.

Starting from SLEEP, if the wake-up flag is set, the device enters STANDBY regardless the host pins state and UV flags. Starting from SLEEP, if the wake-up flag is not set, the only operating mode that can be entered through host pins are the non low power modes.

Operating Mode Transitions

Table 7. Transition Table

Transition		Event	Under Voltage Flag			Wake Flag	Host Input		Remarks
Start Point	**Destination**		V_{IO}	V_{BAT}	V_{CC}		**STBN**	**EN**	
NORMAL	RECEIVE ONLY	S	L	L	L	X	H	(1) H→L	
	STANDBY	U	L	L	(1) L→H	(2) X→L	H	H	
	GO TO SLEEP	S	L	L	L	(2) X→L	(1) H→L	H	timer enabled
	SLEEP	U	(1) L→H	L	L	(2) X→L	H	H	
		U	L	(1) L→H		(2) X→L	H	H	
RECEIVE ONLY	NORMAL	S	L	L	L	X	H	(1) L→H	
	STANDBY	S	L	L	L	(2) X→L	(1) H→L	L	
		U	L	L	(1) L→H	(2) X→L	H	L	
	SLEEP	U	(1) L→H	L	L	(2) X→L	H	L	
		U	L	(1) L→H	L	(2) X→L	H	L	

Table 7. Transition Table

Transition		Event	Under Voltage Flag			Wake Flag	Host Input		Remarks
Start Point	Destination		V_{IO}	V_{BAT}	V_{CC}		STBN	EN	
STANDBY	NORMAL	U	L	L	(1) H→L	L	H	H	
		W	L	L	(2) H→L	(1) L→H	H	H	
	RECEIVE ONLY	S	L	L	L	X	(1) L→H	L	
		U	L	L	(1) H→L	L	H	L	
		W	L	L	(2) H→L	(1) L→H	H	L	
	GO TO SLEEP	S	L	L	L	L	L	(1) L→H	timer enabled
		S	L	L	L	H	L	(1) L→H	timer disabled
		U	L	L	(1) H→L	L	L	H	timer enabled
		W	L	L	(2) H→L	(1) L→H	L	H	timer disabled
	SLEEP	U	(1) L→H	L	L	(2) X→L	L	L	
		U	(1) L→H	L	H	L	X	X	
		U	L	(1) L→H	L	(2) X→L	L	L	
	STANDBY	W	L	L	(2) X→L	(1) L→H	L	L	
		U	L	L	(1) L→H	(2) X→L	L	L	
		U	L	L	(1) H→L	L	L	L	
		S	L	L	H	L	(1) L↔H	X	
		S	L	L	H	L	X	(1) L↔H	
GO TO SLEEP	NORMAL	S	L	L	L	X	(1) L→H	H	
	STANDBY	S	L	L	L	X	L	(1) H→L	
		U	L	L	(1) L→H	(2) X→L	L	H	
	SLEEP	S	L	L	L	L	L	H	$t \geq t_{SLEEP}$
		U	(1) L→H	L	L	(2) X→L	L	H	
		U	L	(1) L→H	L	(2) X→L	L	H	
	GO TO SLEEP	W	L	L	L	(1) L→H	L	H	timer disabled

Table 7. Transition Table

Transition		Event	Under Voltage Flag			Wake Flag	Host Input		Remarks
Start Point	Destination		V_{IO}	V_{BAT}	V_{CC}		STBN	EN	
SLEEP	NORMAL	S	L	L	L	L	(1) L→H	H	
		W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	H	H	
		U	L	(1) H→L	L	L	H	H	
		U	(1) H→L	L	L	L	H	H	
	RECEIVE ONLY	S	L	L	L	L	(1) L→H	L	
		W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	H	H	
		U	L	(1) H→L	L	L	H	L	
		U	(1) H→L	L	L	L	H	L	
	STANDBY	W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	L	L	
		U	L	(1) H→L	L	L	L	L	
		U	(1) H→L	L	L	L	L	L	
		U	(1) H→L	L	H	L	X	X	
	GO TO SLEEP	W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	L	H	timer disabled
		U	L	(1) H→L	L	L	L	H	timer disabled
		U	(1) H→L	L	L	L	L	H	timer disabled
	SLEEP	S	X	X	X	L	X	(1) L↔H	
		S	H	L	X	L	(1) L↔H	X	
		S	L	H	L	L	(1) L↔H	X	
		S	H	H	L	L	(1) L↔H	X	
		U	X	(1) L→H	L	L	X	X	
		U	(1) L→H	X	X	L	X	X	
		U	L	L	(1) L↔H	L	X	X	

Note: S = transition forced via EN, STBN; U = transition forced via undervoltage or voltage recovery; W = transition forced via WAKE

(1) Indicates the action, that initiates the transition

(2) Indicates the consequence after performed transition

(3) Incase of Wake flag is set, it is not possible to enter SLEEP mode through a Sleep command, requested by the host.

(4) In case an undervoltage on V_{BAT} and V_{CC} is detected, the device enters the Power Off state.

ERRN Signalling

The internal flag EN_RISE is set if a rising edge on the EN pin occurs. The EN_RISE is reset when the wake-upake-up flag is set. EN_RISE flag is reset at power off. The ERRN signalling is shown in Table 8.

Table 8. ERRN signalling

SUPPLY VOLTAGE FLAG EVENT V_{IO}	RWAKE FLAG	LWAKE FLAG	HOST COMMAND		ERRN
			STBN	EN	
L	X	X	H	H	Not failure
L	H	X	H	L	If EN_RISE then not an error flag else L
L	L	X	H	L	If EN_RISE then not an error flag else H
L	L	L	L	X	H
L	L	L→H	L	X	H→L
L	L→H	L	L	X	H→L
L	H	L→H	L	X	L
L	L→H	H	L	X	L
H	X	X	X	X	L

Loss of ground

Whenever a loss of ground is detected, the bus lines are switched Idle_HZ with the precondition that the host pins are open. Either error or no error can be indicated on the ERRN pin.

Error Flags Description

Undervoltage V_{BAT} detected

This flag is set when the V_{BAT} UV flag is set and it is reset when the 3rd bit of the read out sequence has been shifted out.

Undervoltage V_{IO} detected

This flag is set when the V_{IO} UV flag is set and it is reset when the 3rd bit of the read out sequence has been shifted out.

Undervoltage V_{CC} detected

This flag is set when the V_{CC} UV flag is set and it is reset when the 3rd bit of the read out sequence has been shifted out.

Bus error

The bus error flag is set when 2 consecutive rising edges on the TxD pin without any rising edge on the RxD pin are detected or when 2 consecutive falling edges on the TxD pin without any falling edge on the RxD pin are detected. This flag is reset when a rising edge on the TxD pin is followed by a rising edge on RxD pin before of the next TxD rising edge or when a falling edge on the TxD pin is followed by a falling edge on RxD pin before of the next TxD falling edge. This flag can be set or reset only in NORMAL mode when the transmitter is enabled. The flag is reset at power off.

Low current on BP high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

Low current on BP low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

Low current on BM high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

Low current on BM low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BP high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BP low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BM high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BM low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

BP open line

This flag is the logical “AND” between: low current on BP high side and low current on BP low side.

BM open line

This flag is the logical “AND” between: low current on BM high side and low current on BM low side.

BP short circuit to V_{CC}

This flag is the logical “AND” between: low current on BP high side and high current on BP low side.

BP short circuit to GND

This flag is the logical “AND” between: high current on BP high side and low current on BP low side.

BM short circuit to V_{CC}

This flag is the logical “AND” between: low current on BM high side and high current on BM low side.

BM short circuit to GND

This flag is the logical “AND” between: high current on BM high side and low current on BM low side.

Short circuit between BP and BM

This flag can only be set or reset in NORMAL mode when the driver is enabled. After a time t_{BUS_ERROR} since TxD edge if the absolute value of the differential bus voltage is lower than V_{SHORT} then the flag is set otherwise it is reset. he flag is reset at power off.

Over temperature

This flag can only be set or reset in the non low power modes. The flag is set when the junction temperature exceeds OT_{TH} and it is reset when the junction temperature falls below OT_{TL}.

TxEN_BGE timeout

This flag can only be set in NORMAL mode when the driver is enabled (TxEN is low and BGE is high) for a time longer than t_{TxEN_max}. It is reset every transition on TxEN or BGE or if the device exits NORMAL mode. If the flag is set the driver is disabled.

Error flag

This flag is set if at least one error flag, except undervoltage V_{BAT}, V_{IO} and V_{CC}, is set and it is reset if none of the previous bits are set.

Status Flags Description

Power on flag

The power on flag is set leaving the power off state and it is reset entering a low power mode after a non low power mode.

For Local Wake Flag and Remote wake Flag description (see Wake-Up Events on page 16)

Error Flags and Status Flags Read Out

The readout mechanism consists of two information groups:

1. Error Read Out
2. Status Information Read Out

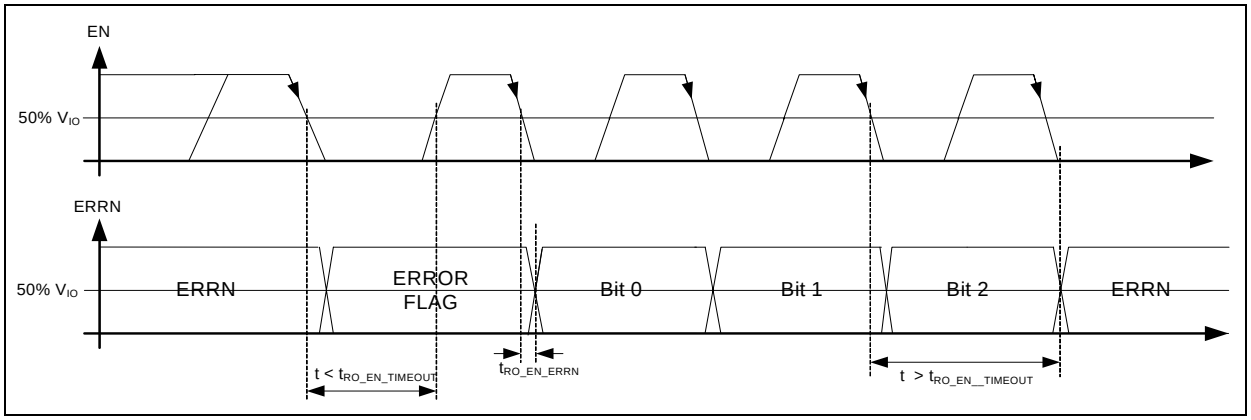
The readout mechanism as serial transmission on Pin EN and ERRN:

Table 9. Read Out Mechanism and Transceiver States

State	Enabled/Disabled
NORMAL mode	Enabled
RECEIVE ONLY mode	Enabled
STANDBY mode	Disabled
GO TO SLEEP mode	Disabled
SLEEP mode	Disabled

The error flags and the status flags can be read out by applying a clock signal to pin EN in a non low power mode. A falling edge on pin EN starts the read out loading the content of the error/status flag into the shift register and signaling the error flag on the ERRN pin. On the second falling edge the first flag (Bit 0) will be shifted out. The ERRN data is valid after $t_{RO\_EN\_ERRN}$. If EN pin keeps on toggling after last flag (Bit 15) the next flag shifted out is Bit 0. The complete list of bits is shown in Table 10. If no transition is detected on pin EN for longer than $t_{RO\_EN\_TIMEOUT}$ the device enters the operation mode indicated by the host pins.

Figure 12. Timing of the read out mechanism



Error and Status flag bit order

Table 10. Bit order for the read out sequence

Bit	Description	Symbol
Bit 0	Undervoltage V_{BAT} detected	UVV_{BAT}_DET
Bit 1	Undervoltage V_{IO} detected	UVV_{IO}_DET
Bit 2	Undervoltage V_{CC} detected	UVV_{CC}_DET
Bit 3	Bus error	BUSERR
Bit 4	BP open line	BP_OL
Bit 5	BP short circuit to V_{CC}	BP_V_{CC}
Bit 6	BP short circuit to GND	BP_GND
Bit 7	BM open line	BM_OL
Bit 8	BM short sourced to V_{CC}	BM_V_{CC}
Bit 9	BM short sourced to GND	BM_GND
Bit 10	Short circuit between BP and BM	BP_BM
Bit 11	Over temperature	OT
Bit 12	TxEN_BGE timeout	TxEN_TO
Bit 13	Local wake flag	LWAKE
Bit 14	Remote wake flag	RWAKE
Bit 15	Power on flag	PWON

When the read out mechanism is started, the first data information is the Bit 0 until Bit 23 is transmitted. Any re-initiation or repetitions is started with the first data Bit 0.

Failure detector

The failure detector detects the transceiver failures and updates the internal failure register as specified below. This register is cleared at power-up, after the dedicated failure cannot be detected and for some failures after a certain time (e.g. over temperature). In the chapters below the fault conditions resulting from the functional features are shown.

Power Off

Fault condition power off is always recognized, if the device is in power off state. In this case the ERRN output pin is switched to “low” for signalling an error and the bus lines are switched to Idle_HZ (bus idle, with high impedance, that means bus lines are floating).

Undervoltage V_{BAT}

Whenever the undervoltage V_{BAT} flag is set, the bus lines are in Idle_LP (idle low power) and the ERRN is switched to “low” for signalling an error. Vice versa, the error is not signalled on the ERRN pin, when the flag is not set.

Undervoltage V_{CC}

Whenever the undervoltage V_{CC} flag is set, the bus lines are in Idle_LP (idle low power) and the ERRN is switched to “low” for signalling an error. Vice versa, the error is not signalled on the ERRN pin, when the flag is not set.

Undervoltage V_{IO}

Whenever the undervoltage V_{IO} flag is set, the bus lines are in Idle_LP (idle low power) and the ERRN is switched to “low” for signalling an error. Vice versa, the error is not signalled on the ERRN pin, when the flag is not set.

Bus Error (Short circuit/open load on bus lines and short circuit between BP and BM)

Short circuit on bus lines comprises the 10 flags for high current flags on BP and BM and the flag for detecting short circuit between the bus lines. Whenever on of these flags is set, an error is signalled on the ERRN pin. For high current detection, the current is limited for the bus lines.

TxD interrupted

If the TxD line is interrupted, Data0 is signalled on the bus lines.

TxEN timeout

Whenever the TxEN timeout flag is set, the bus lines are switched into Idle or Idle_LP

Over temperature

Whenever the over temperature flag is set, the bus lines are switched into Idle or Idle_LP.

No mode change

Whenever the no mode change flag is set, an error is indicated on the ERRN pin.

Transmitter

The transmitter generates out of a digital input signal on TxD the FlexRay differential bus voltage. The transmitter is only active in NORMAL mode when BGE is on logical high and TxEN is on logical low.

Figure 13. Transmitter characteristics (TxD → BUS)

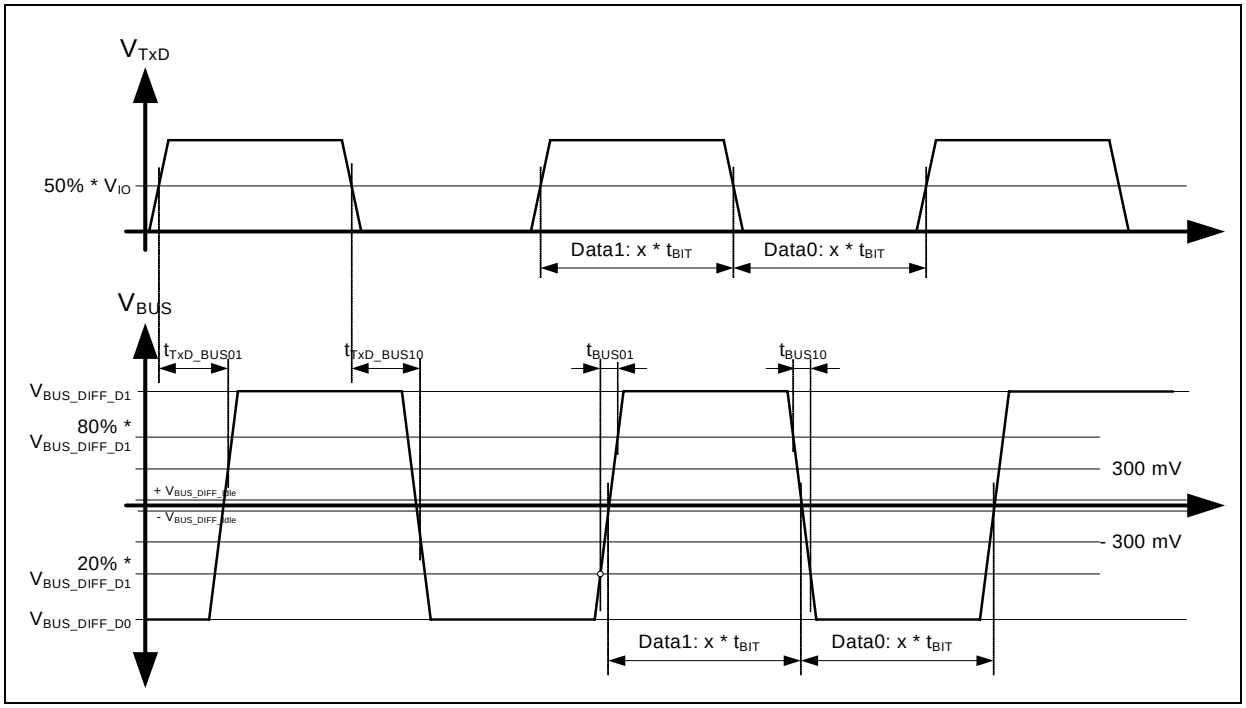


Figure 14. Transmitter characteristics (TxEN → BUS)

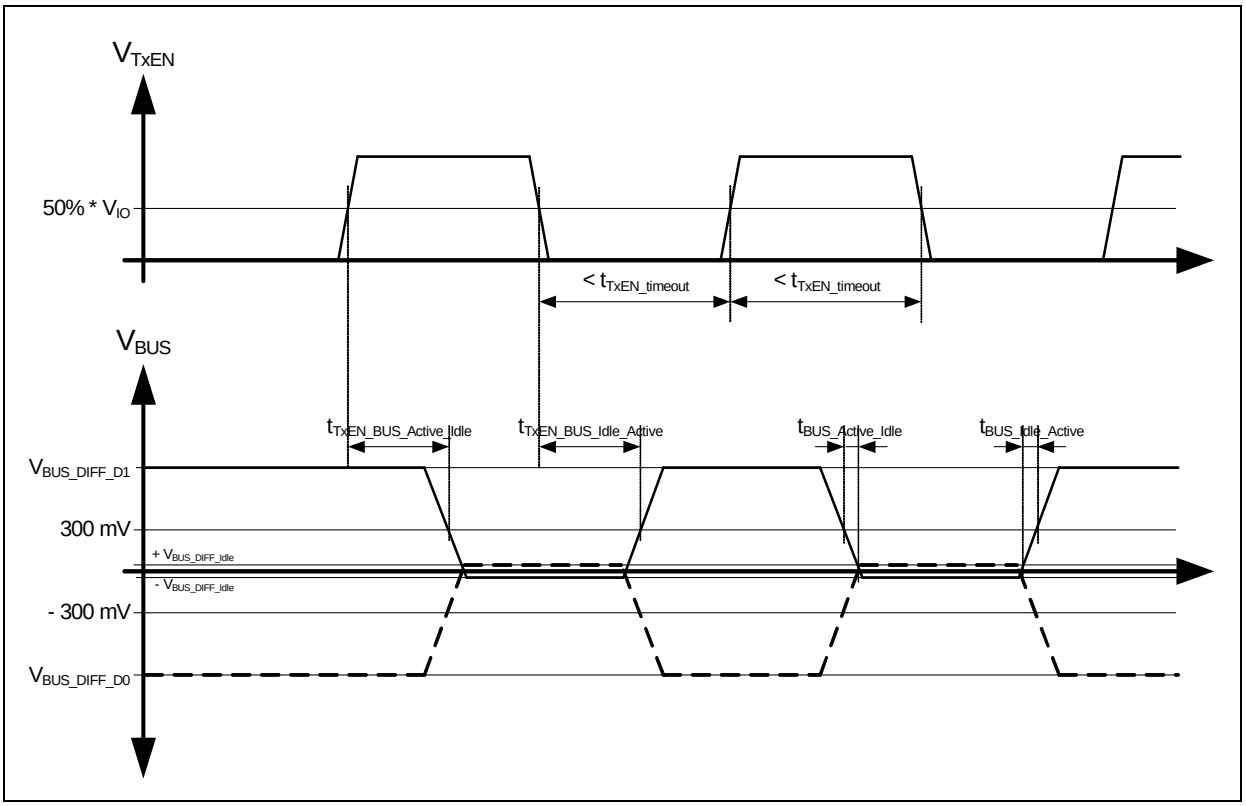
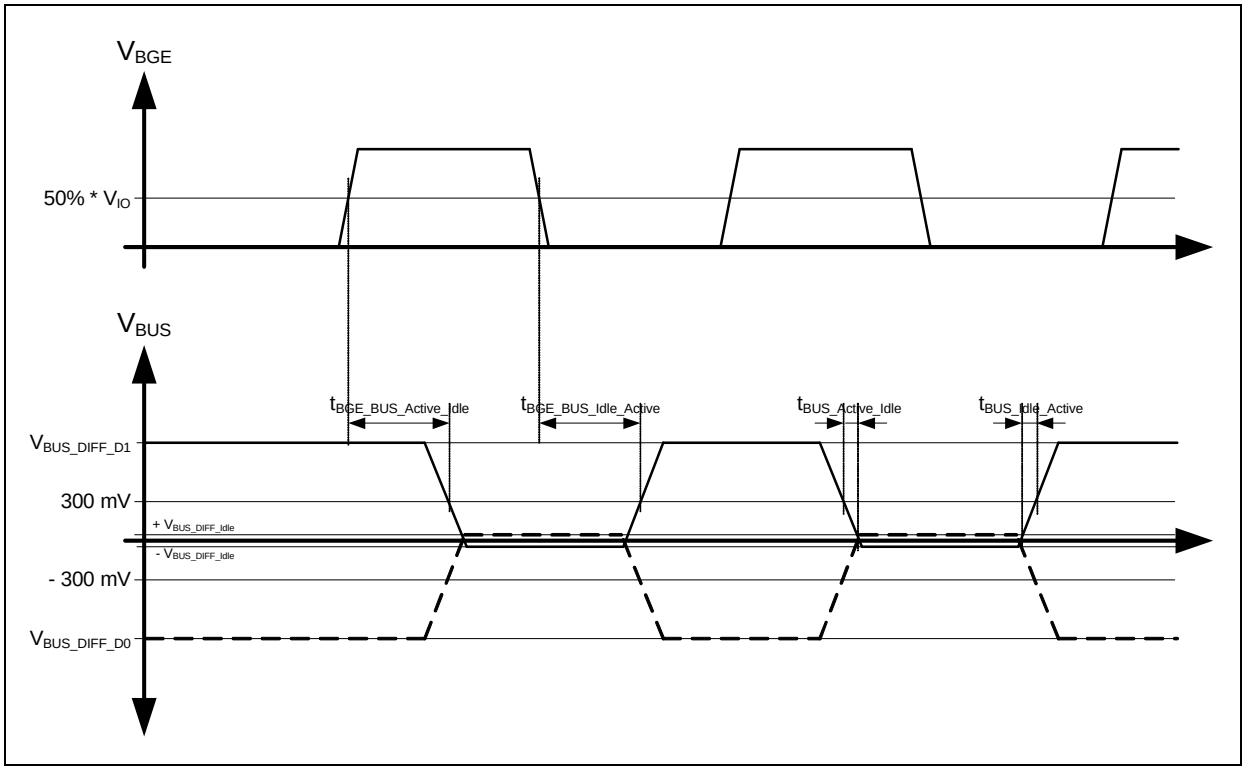


Figure 15. Timing characteristics (BGE → BUS)

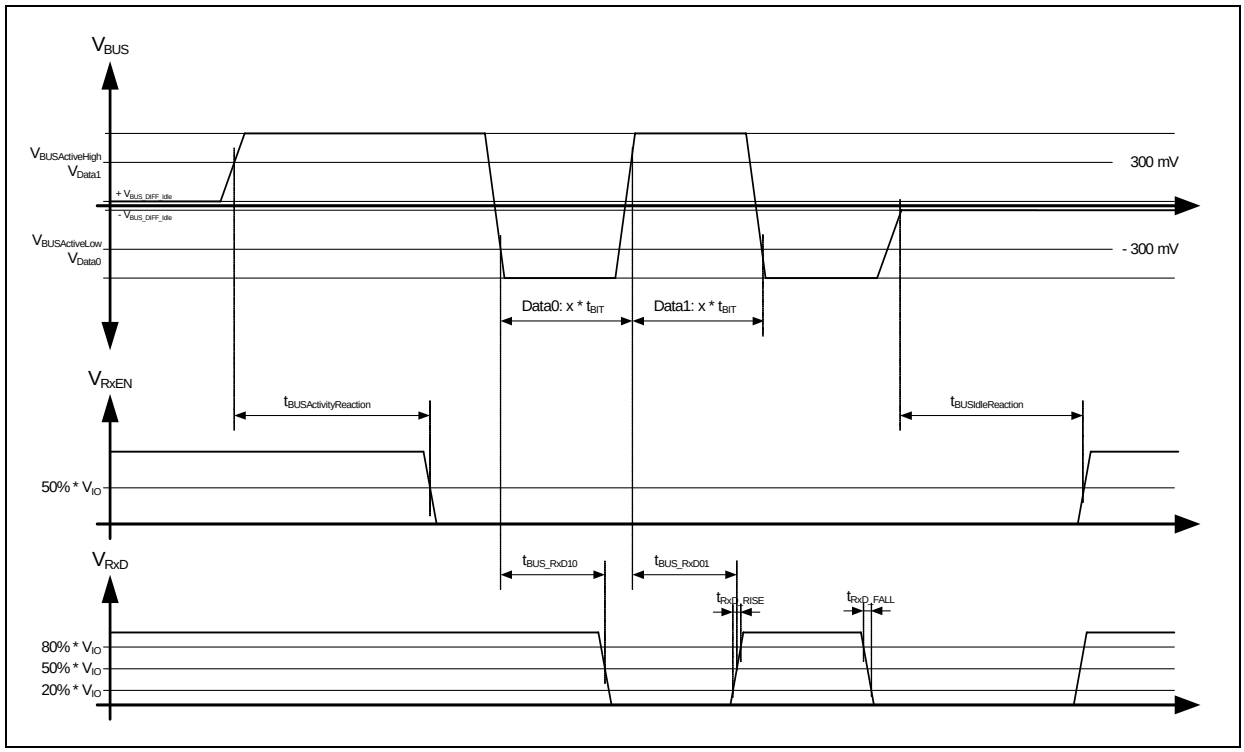


In NORMAL and RECEIVE ONLY mode the transmitter drives on the bus Idle in case no data are transmitted. In STANDBY, GO TO SLEEP and SLEEP mode the transmitter drives Idle_LP (idle low power) on the bus pins. In POWER OFF mode the bus pins shows Idle_HZ (idle high impedance).

Receiver

The receiver generates from the FlexRay differential bus voltage a digital signal on the RxD and RxEN pins. RxD shows the data (Data0 and Data1) and RxEN shows the bus idle and activity status received on the bus pins. The receiver is only active in NORMAL and RECEIVE ONLY mode.

Figure 16. Timing characteristics of the bus signals to RxD and RxEN



Bus activity and idle detection (only in NORMAL and RECEIVE ONLY mode)

If the absolute differential bus voltage is higher than VBUSActiveLow and less than $V_{BUSActiveHigh}$ for a time longer than $t_{BUSIdleDetection}$, bus Idle is detected, RxEN and RxD are switched to logical high after a time $t_{BUSIdleReaction}$.

If the absolute differential bus voltage is higher than $V_{BUSActiveHigh}$ or lower than $V_{BUSActiveLow}$ for a time loner than $t_{BUSActivitiyDetection}$, bus Activity is detected, RxEN is switched to logical low and RxD is following the detected bus data states as indicated below with a time $t_{BUSActivityReaction}$.

Table 11. Logic table for receiver bus signal detection

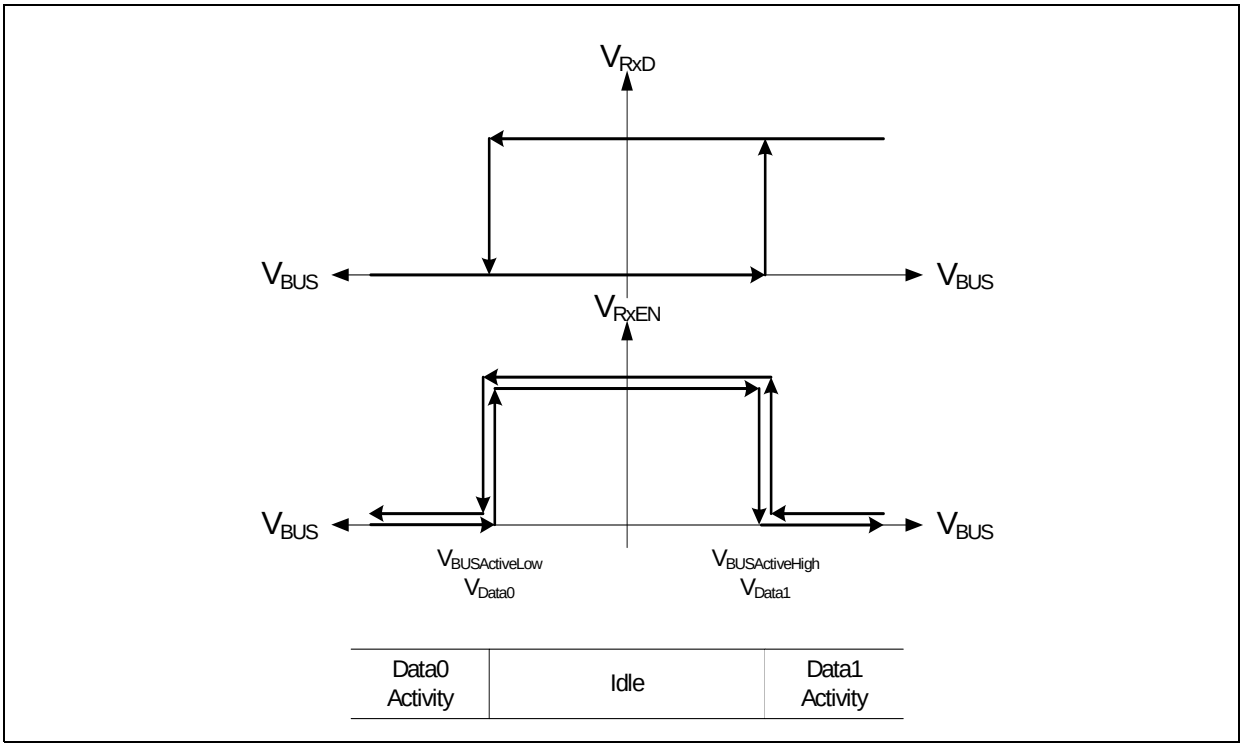
Receiver Operation mode	Bus signals	RxEN	RxD
Normal power modes (NORMAL and RECEIVE ONLY mode)	Idle	H	H
	Data0	L	L
	Data1	L	H

Bus data detection (only in NORMAL and RECEIVE ONLY mode)

If, after the activity detection the differential bus voltage is higher than VData1, RxD will be high after a time t_{BUS_RxD01}.

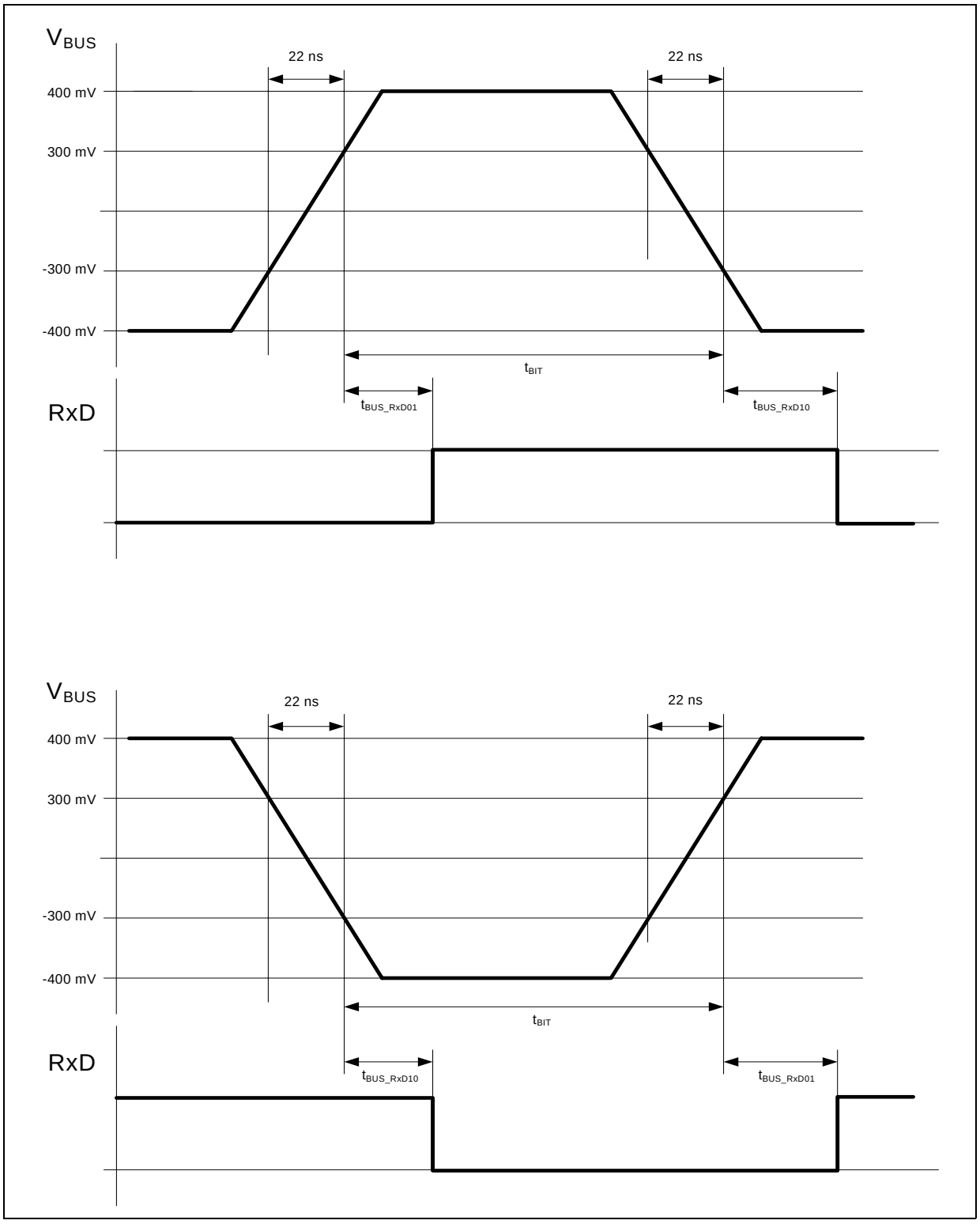
If, after the activity detection the differential bus voltage is lower than VData0, RxD will be low after a time t_{BUS_RxD10}.

Figure 17. Receiver characteristics (BUS → RxD, RxEN)



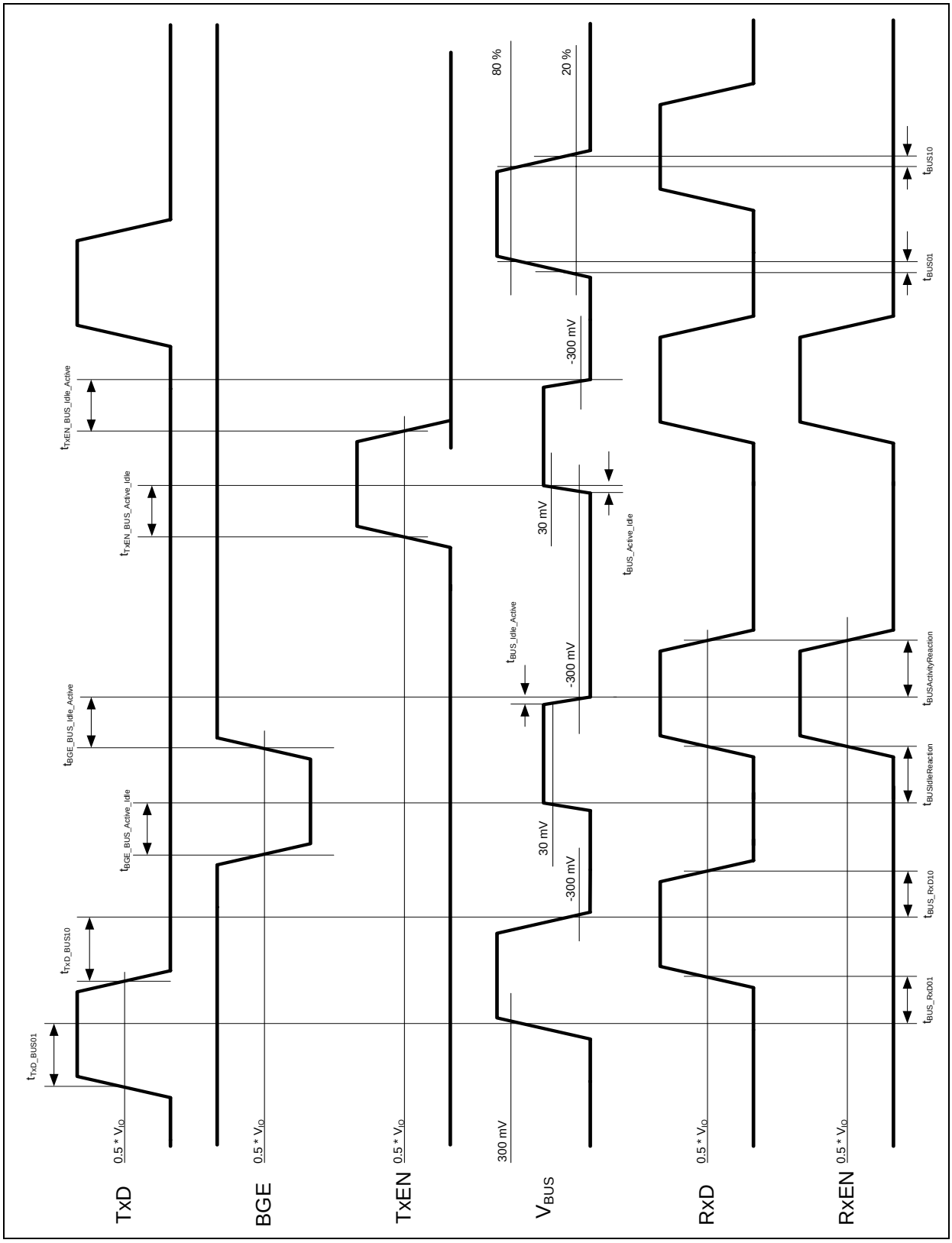
Receiver test signal

Figure 18. Receiver test signal



Transceiver Timing

Figure 19. Timing Diagram



Test Circuits

Figure 20. Test Circuit for Automotive Transients

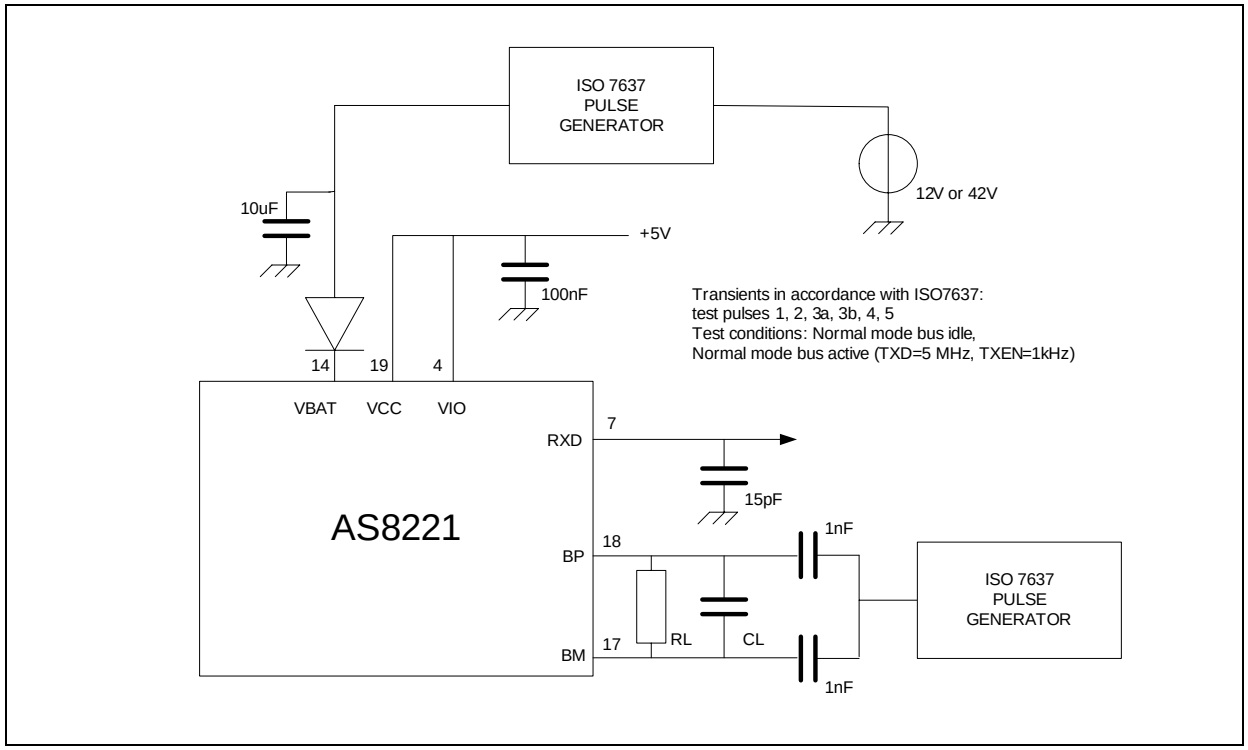
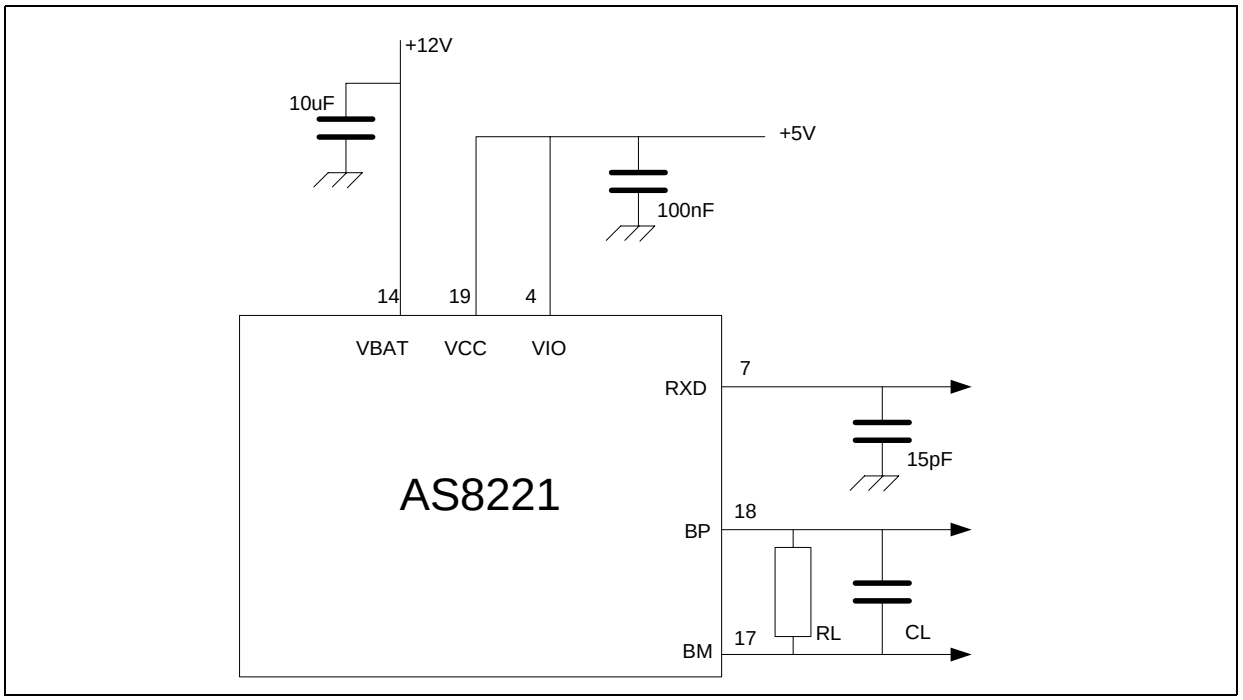


Figure 21. Test circuit for dynamic characteristics



9 Appendix

FlexRay Functional Classes

The AS8221 device comprises following Functional Classes according the FlexRay Electrical Physical Layer Specification V2.1 Rev. B:

- Functional Class “BD Voltage Regulator Control”
- Functional Class “Bus Driver - Bus Guardian Control Interface”
- Functional Class “Bus Driver Internal Voltage Regulator”
- Functional Class “Bus Driver Logic Level Adaptation”

FlexRay Parameter Comparison

The following table shows the comparison of conventions used in AS8221 datasheet and FlexRay Electrical Physical Layer Specification V2.1 Rev. B.

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
Absolute Maximum Ratings			
-	Battery Supply Voltage (V_{BAT})	-	-
-	Supply Voltage (V_{CC})	-	-
-	Supply Voltage (V_{IO})	-	-
-	DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-	-
-	DC Voltage on pin WAKE, INH1, INH2	-	-
-	DC Voltage at BP and BM	-	-
-	Input current (latchup immunity)	-	-
-	Electrostatic discharge at bus lines BP, BM, V_{BAT}, WAKE	uESDExt	ESD protection on pins that lead to ECU external terminals
-	Electrostatic discharge	uESDint	ESD on all other pins
-	Transient voltage on BP, BM	-	-
-	Transient voltage on V_{BAT}	-	-
-	Total power dissipation (all supplies and outputs)	-	-
-	Storage temperature	-	-
-	Junction temperature	-	-
-	Package body temperature	-	-
-	Humidity non-condensing	-	-
Supply Voltage			
Tamb	Ambient temperature	T	Ambient temperature
V_{CC} - V_{IO}	Difference of supplies	-	-
I_{BAT}	V_{BAT} current consumption	-	-

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
I_{CC}	V_{CC} current consumption	-	-
I_{IO}	V_{IO} current consumption	-	-
State Transitions			
t_{STBN_RxD}	Delay STBN high to RxD high with wake flag set	-	-
t_{STBN_RxEN}	Delay STBN high to RxEN high with wake flag set	-	-
t_{SLEEP_INH1}	Delay STBN high to INH1 high	-	-
$t_{STANDBY\_INH2}$	Delay STBN high to INH2 high	-	-
t_{SLEEP}	go-to-sleep hold time	-	-
Transmitter			
$V_{BUS\_DIFF\_D0}$	Differential bus voltage low in NORMAL mode (Data0)	$uBDTx_{active}$	Absolute value of uBus while sending
$V_{BUS\_DIFF\_D1}$	Differential bus voltage high in NORMAL mode (Data1)	$uBDTx_{active}$	Absolute value of uBus while sending
V_{BUS_DIFF}	Matching between Data0 and Data1 differential bus voltage in NORMAL mode	-	-
$V_{BUS\_COM\_D0}$	Common mode bus voltage in case of Data0 in non low power modes	-	-
$V_{BUS\_COM\_D1}$	Common mode bus voltage in case of Data1 in non low power modes	-	-
V_{BUS_COM}	Matching between Data0 and Data1 common mode voltage	-	-
$V_{BUS\_DIFF\_Idle}$	Absolute differential bus voltage in idle mode	uBDTxidle	Absolute value of uBus, while Idle
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute max current when BP is shorted to BM	$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute maximum output current when BP shorted to BM
$IBP_{GNDShortMax}$	Absolute max current when BP is shorted to GND	$IBP_{GNDShortMax}$	Absolute maximum output current when shorted to GND
$IBM_{GNDShortMax}$	Absolute max current when BM is shorted to GND	$IBM_{GNDShortMax}$	Absolute maximum output current when shorted to GND
$IBP_{-5VShortMax}$	Absolute max current when BP is shorted to -5 V	$IBP_{-5VShortMax}$	Absolute maximum output current when shorted to -5V
$IBM_{-5VShortMax}$	Absolute max current when BM is shorted to -5 V	$IBM_{-5VShortMax}$	Absolute maximum output current when shorted to -5V
$IBP_{27VShortMax}$	Absolute max current when BP is shorted to 27 V	$IBP_{BAT27VShortMax}$	Absolute maximum output current when shorted to 27V

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
$IBM_{27VShortMax}$	Absolute max current when BM is shorted to 27 V	$IBM_{BAT27VShortMax}$	Absolute maximum output current when shorted to 27V
$IBP_{48VShortMax}$	Absolute max current when BP is shorted to 48 V	$IBP_{BAT48VShortMax}$	Absolute maximum output current when shorted to 48V
$IBM_{48VShortMax}$	Absolute max current when BM is shorted to 48 V	$IBM_{BAT48VShortMax}$	Absolute maximum output current when shorted to 48V
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	dBDTx10	Transmitter delay, negative edge
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	dBDTx01	Transmitter delay, positive edge
$t_{TxD\_MISMATCH}$	Delay time from TxD to BUS mismatch	dTxAsym	Transmitter delay mismatch | dBDTx10 - dBDTx01 |
t_{BUS_10}	Fall time differential bus voltage	dBusTx10	Fall time differential bus voltage (80% → 20%)
t_{BUS_01}	Rise time differential bus voltage	dBusTx01	Rise time differential bus voltage (20% → 80%)
$t_{TxEN\_BUS\_Idle\_Active}$	Delay time from TxEN to bus active	dBDTxia	Propagation delay idle →active
$t_{TxEN\_BUS\_Active\_Idle}$	Delay time from TxEN to bus idle	dBDTxai	Propagation delay active → idle
$t_{TxEN\_MISMATCH}$	Delay time from TxEN to bus mismatch	dBDTxDM	| dBDTxia - dBDTxai |
$t_{BGE\_BUS\_Idle\_Active}$	Delay time from BGE to bus active	dBDTxia	Propagation delay idle → active
$t_{BGE\_BUS\_Active\_Idle}$	Delay time from BGE to bus idle	dBDTXai	Propagation delay active → idle
$t_{BUS\_Idle\_Active}$	Differential bus voltage transition time: idle to active	dBusTxia	Transition time idle → active
$t_{BUS\_Active\_Idle}$	Differential bus voltage transition time: active to idle	dBusTxai	Transition time active → idle
$t_{TxEN\_timeout}$	TxEN timeout	-	-
Receiver			
R_{BP}, R_{BM}	BP, BM input resistance	RCM1, RCM2	Receiver common mode input resistance
R_{DIFF}	BP, BM differential input resistance	-	-
V_{BPidle}, V_{BMidle}	Idle voltage in non low power modes on pin BP,BM	uBias	Bus bias voltage during BD_Normal mode
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in low power modes on pin BP, BM	uBias	Bus bias voltage during low power modes
I_{BPidle}	Absolute idle output current on pin BP	-	-
I_{BMidle}	Absolute idle output current on pin BM	-	-

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	iBPLeak, iBMLeak	Absolute leakage current, when not powered
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	uBusActiveHigh	Upper receiver threshold for detecting activity
$V_{BUSActiveLow}$	Activity detection differential input voltage low	uBusActiveLow	Lower receiver threshold for detecting activity
V_{Data1}	Data1 detection differential input voltage	uData1	Receiver threshold for detecting Data_1
V_{Data0}	Data0 detection differential input voltage	uData0	Receiver threshold for detecting Data_0
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	uData	Mismatch of receiver thresholds
$V_{RECEIVE\_COM}$	Max. common mode voltage range when receiving	uCM	Common mode voltage range (with respect to GND) that does not disturb the receive function
t_{BUS_RxD10}	Delay from bus to RxD negative edge	dBDRx10	Receiver delay, negative edge
t_{BUS_RxD01}	Delay from bus to RxD positive edge	dBDRx01	Receiver delay, positive edge
t_{BIT}	Bit time	-	-
t_{RxD_ASYM}	Delay time from bus to RxD mismatch	dRxAsym	Receiver delay mismatch | dBDRx10 – dBDRx01 |
t_{RxD_FALL}	Fall time RxD voltage	dRxSlope	Fall and rise time 20%-80%
t_{RxD_RISE}	Rise time RxD voltage	dRxSlope	Fall and rise time 20%-80%
$t_{BUSIdleDetection}$	Idle detection time	dIdleDetection	Filter-time for idle detection
$t_{BUSActivityDetection}$	Activity detection time	dActivityDetection	Filter-time for activity detection
$t_{BUSIdleReaction}$	Idle reaction time	dBDRxai	Idle reaction time
$t_{BUSActivityReaction}$	Activity reaction time	dBDRxia	Activity reaction time
Wake-Up Detector			
t_{BWU_D0}	Data0 detection time in remote wake-up pattern	dWU0Detect	Acceptance timeout for detection of a Data_0 phase in wake-up pattern
t_{BWU_Idle}	Idle or Data1 detection time in remote wake-up pattern	dWUIdleDetect	Acceptance timeout for detection of a Idle phase in wake-up pattern
t_{BWU_Detect}	Total remote wake-up detection time	dWUTimeout	Acceptance timeout for wake-up pattern recognition
V_{BWUTH}	Bus wake-up detection threshold	-	-

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
V_{LWUTH}	Local wake-up detection threshold	-	-
I_{LWUL}	Low level input current on local WAKE pin	-	-
I_{LWUH}	High level input current on local WAKE pin	-	-
$t_{LWUFilter}$	Local wake filter time	dWakePulseFilter	Wake pulse filter time (spike rejection)
-	V_{BAT} operating range V_{BAT} = +6.5 to + 50V	V_{BAT} for WU detector	Battery voltage required for wake-up detector operation
Supply Voltage Monitor			
V_{BATTHH}	V_{BAT} undervoltage recovery threshold	-	-
V_{BATTHL}	V_{BAT} undervoltage detection threshold	uUVBAT	Undervoltage detection threshold
V_{CCTHH}	V_{CC} undervoltage recovery threshold	-	-
V_{CCTHL}	V_{CC} undervoltage detection threshold	uUVCC	Undervoltage detection threshold
V_{IOTHH}	V_{IO} undervoltage recovery threshold	-	-
V_{IOTHL}	V_{IO} undervoltage detection threshold	uUVIO	Undervoltage detection threshold
t_{UV_DETECT}	Detection time for undervoltage at V_{BAT}, V_{CC}, V_{IO}	dUVBAT, dUVCC, dUVIO	Undervoltage reaction time
t_{UV_REC}	Detection time for undervoltage recovery at V_{BAT}, V_{CC}, V_{IO}	-	-
Bus Error Detection			
I_{THL}	Absolute bus current for low current detection	-	-
I_{THH}	Absolute bus current for high current detection	-	-
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	-	-
t_{BUS_ERROR}	Bus error detection time	-	Detection only required while actively transmitting a data frame, error indication to host latest when transmission stops.
Over Temperature			
OT_{TH}	Over temperature threshold	-	-
OT_{TL}	Over temperature hysteresis	-	-

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
Power Supply Interface			
V_{OINH}	High level voltage drop on INH1, INH2	-	-
$\lvert I_{IL} \rvert$	Leakage current	-	-
Communication Controller Interface			
V_{TxDIH}	Threshold for detecting TxD as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{TxDIL}	Threshold for detecting TxD as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{TxDIH}	TxD high level input current	-	-
I_{TxDIL}	TxD low level input current	-	-
V_{TxENIH}	Threshold for detecting TxEN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{TXENIL}	Threshold for detecting TxEN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{TxENIH}	TxEN high level input current	-	-
I_{TxENIL}	TxEN low level input current	-	-
V_{RxDOH}	RxD high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{RxDOL}	RxD low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Host Interface			
V_{STBNIH}	Threshold for detecting STBN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{STBNIL}	Threshold for detecting STBN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{STBNIH}	STBN high level input current	-	-
I_{STBNIL}	STBN low level input current	-	-
$t_{STBN\_DEB\_LP}$	STBN de-bouncing time low power modes	-	-
$t_{STBN\_DEB\_NLP}$	STBN de-bouncing time non low power modes	-	-
V_{ENIH}	Threshold for detecting EN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high

Table 12. Comparison table

AS8221C Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	**Parameter**	**Name**	**Description**
V_{ENIL}	Threshold for detecting EN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{ENIH}	EN high level input current	-	-
I_{ENIL}	EN low level input current	-	-
$t_{EN\_DEB\_LP}$	EN de-bouncing time low power modes	-	-
$t_{EN\_DEB\_NLP}$	EN de-bouncing time non low power modes	-	-
V_{ERRNOH}	ERRN high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{ERRNOL}	ERRN low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Bus Guardian Interface			
V_{BGEIH}	Threshold for detecting BGE as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{BGEIL}	Threshold for detecting BGE as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{BGEIH}	BGE high level input current	-	-
I_{BGEIL}	BGE low level input current	-	-
V_{RXENOH}	RxEN high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{RXENOL}	RxEN low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Read Out Interface			
$t_{RO\_EN\_ERRN}$	Propagation delay falling edge EN to ERRN	-	-
$t_{RO\_EN\_TIMEOUT}$	Error read out time out	-	-

10 Package Drawings and Markings

Figure 22. package Diagram

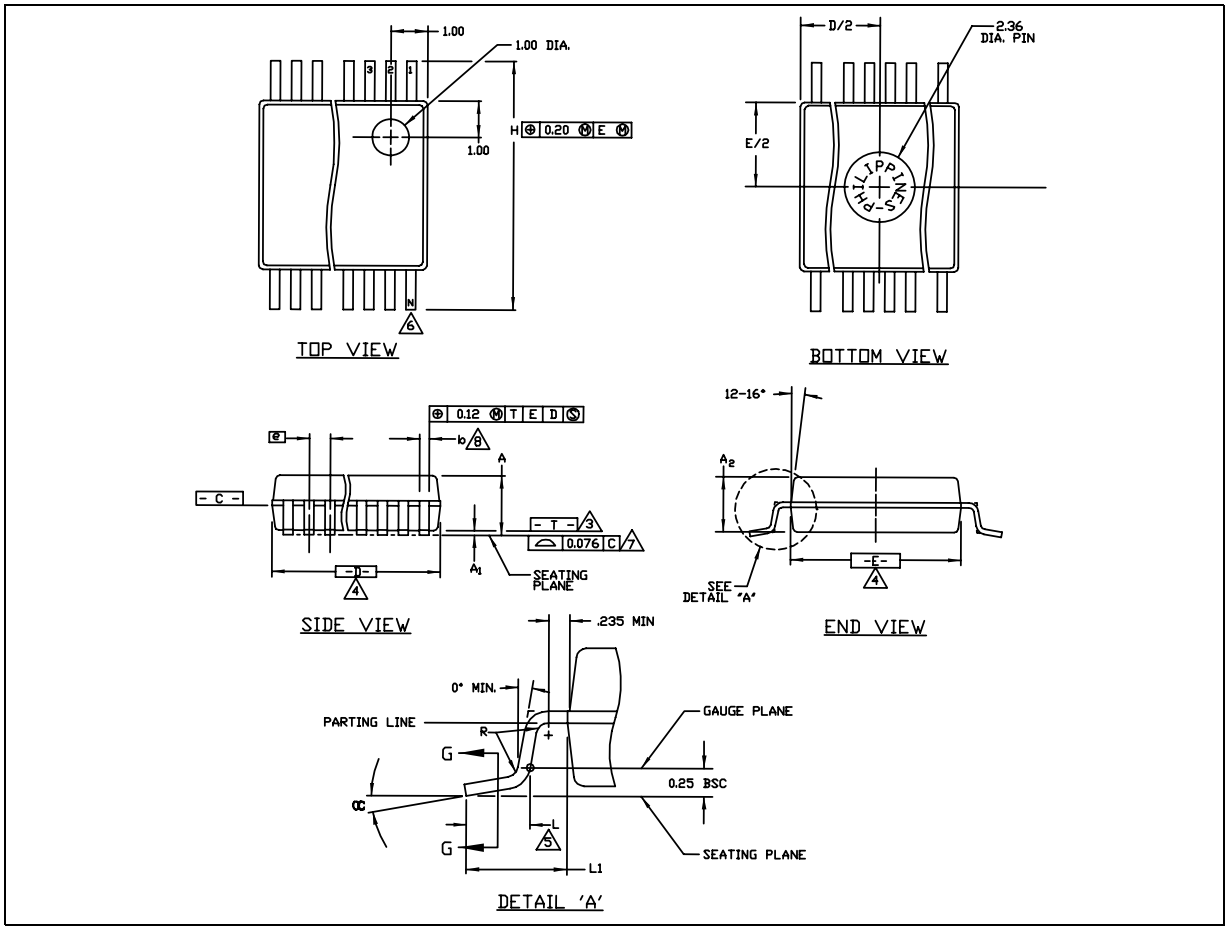


Table 13. package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max	
A	1.73	1.86	1.99	L1	1.25 REF			
A1	0.05	0.13	0.21	N	See Variations			
A2	1.68	1.73	1.78	α	0º	4º	8º	
b	0.25	-	0.38	R	0.09	0.15		
b1	0.25	0.30	0.33	**Variations:**				
C	0.09	-	0.20		D			N
C1	0.09	0.15	0.16	AA	6.07	6.20	6.33	14
D	See Variations			AB	6.07	6.20	6.33	16
E	5.20	5.30	5.38	AC	7.07	7.20	7.33	20
e	0.65 BSC			AD	8.07	8.20	8.33	24
H	7.65	7.80	7.90	AE	10.07	10.20	10.33	28
L	0.63	0.75	0.95	AF	10.07	10.20	10.33	30

Note:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminals.

11 Ordering Information

Table 14. Ordering Information

Type	Marking	Description	Delivery Form	Package

Copyrights

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