Doc No. TA4-EA-06144
Revision. 3

Panasonic

AN33017UA

VIN = 5 to 39 V, 1-channel DC-DC Step down Regulator integrated N-channel Power MOSFET

FEATURES

- Current Feedback Function compensates output voltage drop due to external USB cable loss
- Internal reference voltage is within ±1% accuracy.
- Input Voltage Range : PVCC , VCC: 5 V to 39 V
- Switching frequency is adjustable within the range of 200 kHz to 2 MHz by an external resistor.
- Standby mode consumes less than 1μA current.
- Adjustable Output Voltage Range with external Resistor : 1.2 V ~ 9 V.
- Output over voltage protection (OVP1) function.
- Output ground short protection function.
- Input over voltage protection (OVP2) function.
- Over current protection (OCP) with adjustable threshold.
- Over current detection level with switchable.
- Power supply under-voltage lockout (UVLO) function.
- Thermal Shut-Down (TSD) function.
- Adjustable soft-start function.
- 48 pin Plastic Quad Flat Package With Heat Sink. (QFP Type)

DESCRIPTION

AN33017UA is 1-channel DC-DC Step down Regulator integrated N-channel Power MOSFET and employs the voltage mode switching control system.

This IC can be operated with wide input voltage range and is build in several protection functions, so this IC can provide high reliability power supply system.

Since it is possible to use up to 2MHz switching frequency and it is unnecessary to add external parts for High Side Switch, this IC realizes downsizing of set and reducing in the number of external parts.

For USB applications, this IC can controlled USB supplied voltage level with external resistor for USB load current monitor (Current Feedback Function), and it can provide suitable power supply system for external USB with no voltage drop due to USB cable loss.

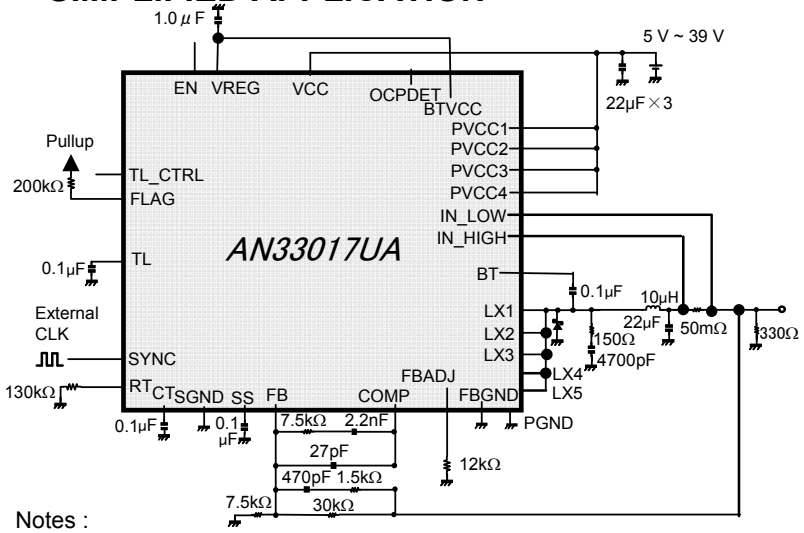
Maximum current is 2.1 A.

APPLICATIONS

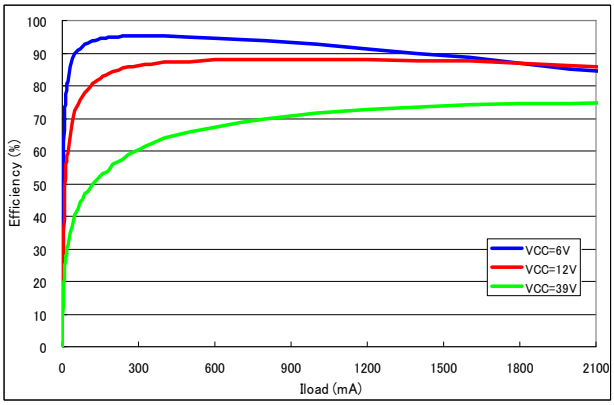
High Input Voltage Power Systems for USB such as

- Car-Audio system
- Car-Navigation system
- OA Equipment
- Home Appliances etc.

SIMPLIFIED APPLICATION



EFFICIENCY CURVE



Condition :
V_{IN} = 6 V, 12 V, 39 V
V_{OUT} = 5 V, L_O = 10 μH, C_O = 22 μF
Frequency = 490 kHz

Notes :

- This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.
- This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.
- These components should be put without fail for reducing the ringing of LX1~5 in light load condition. Please use snubber resistance over 0.5W. Please refer to “OPERATION13.Snubber circuit value setting” for setting specific value.
- Load resistance, Rload should be put without fail. Load resistance under 330Ω is recommended in VOUT=5V condition. Please refer to “OPERATION14.Load resistance, Rload setting” for setting specific value.
- SS pin capacitor, CSS and TL pin capacitor CTL should be put 0.1uF. If you change these components, please keep “ CTL > CSS × 0.9 “ relation.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	60	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*3
Storage temperature	T_{stg}	– 55 to + 150	°C	*3
Input Voltage Range	V_{BT}	– 0.3 to (V_{CC}+ V_{REG})	V	*1, *4
	V_{EN}	– 0.3 to (V_{CC}+ 0.3)	V	*1, *4
	V_{FB} , V_{BTVCC} , V_{TL_CTRL} V_{SYNC} , V_{OCPDET} , V_{RT}, V_{TL}, V_{SS}	– 0.3 to + 5.5	V	*1
	V_{IN_HIGH} , V_{IN_LOW}	– 0.3 to + 10.0	V	*1
Output Voltage Range	V_{FLAG}, V_{COMP}, V_{CT}	– 0.3 to + 5.5	V	*1
	V_{LX1} , V_{LX2} , V_{LX3} , V_{LX4} , V_{LX5}	– 0.3 to (V_{CC}+ 0.3)	V	*1, *4
Input / Output Voltage Range	V_{FBADJ}	– 0.3 to + 5.5	V	*1
ESD	HBM	2	kV	—
	MM	200	V	—

Notes: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1 :The values under the condition not exceeding the power dissipation.
V_{CC} is voltage for VCC, PVCC1, PVCC2, PVCC3, PVCC4
VCC = PVCC1 = PVCC2 = PVCC3 = PVCC4.

*2 :Without power dissipation (P_D) and area of safety operation (ASO) constraint.
$I_{CC} = I_{VCC} + I_{PVCC1} + I_{PVCC2} + I_{PVCC3} + I_{PVCC4}$.

*3 :Except for the operating ambient temperature, operating junction temperature and storage temperature, all ratings are for T_a = 25 °C.

*4 :(V_{CC} + V_{REG}) V, (V_{CC} + 0.3) V must be not exceeded 60 V.

POWER DISSIPATION RATING

PACKAGE	θ_{j-a}	θ_{j-c}	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
48 pin Plastic Quad Flat Package with Heat Sink (QFP Type)	51.6 °C / W	4.1 °C / W	2.425 W	1.261 W	*1

Note: For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1 : Glass-Epoxy(4 layers): 50×50×0.8 (mm) , heat dissipation Die-pad , the state where is mounted with solder.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{CC}	5	12	39	V	*1
	PV_{CC1}					
	PV_{CC2}					
	PV_{CC3}					
	PV_{CC4}					
Input Voltage Range	V_{BT}	– 0.3	—	$V_{CC} + V_{REG}$	V	*1 *2
Input Voltage Range	V_{EN}	– 0.3	—	$V_{CC} + 0.3$	V	*1 *2
Input Voltage Range	V_{FB}	– 0.3	—	5.5	V	*1
	V_{BTVCC}					
	V_{TL_CTRL}					
	V_{SYNC}					
	V_{OCPDET}					
	V_{RT}					
	V_{TL}					
	V_{SS}					
	V_{IN_HIGH}	– 0.3	—	10	V	*1
	V_{IN_LOW}					
Output Voltage Range	V_{LX1}	– 0.3	—	$V_{CC} + 0.3$	V	*1 *2
	V_{LX2}					
	V_{LX3}					
	V_{LX4}					
	V_{LX5}					
	V_{COMP}					
	V_{CT}					
	V_{FLAG}	– 0.3	—	5.5	V	*1
Input / Output Voltage Range	V_{FBADJ}	– 0.3	—	5.5	V	*1

Note) Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for SGND, PGND. SGND = PGND
V_{CC} is voltage for VCC, PVCC1 and PVCC2. VCC = PVCC1 = PVCC2.
*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : ($V_{CC} + V_{REG}$) V, (V_{CC}+ 0.3) V must not be exceeded 60 V.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V , V_{OUT} = 5.0 V , R_T = 130 kΩ , R_{ADJ} = 12 kΩ , R_{SENSE} = 50 mΩ
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Notes
			Min	Typ	Max		
Current Consumption							
Quiescent current	I_{CQ}	No Switching V_{FB} = 1.1 V V_{EN} = 3.3 V	—	1.2	1.9	mA	—
Standby current	I_{STB}	V_{EN} = 0.4 V	—	—	1	μA	—
BGR							
Feedback voltage	V_{REF}	FB connected to COMP	0.99	1.0	1.01	V	—
Enable (EN)							
Low input threshold	V_{IL1}	—	—	—	0.4	V	—
High input threshold	V_{IH1}	—	2.0	—	—	V	—
EN terminal input current	V_{IC1}	V_{EN} = 3.3 V	—	33	70	μA	—
TL CTRL PIN Threshold							
TL_CTRL pin Low input threshold	V_{IL2}	—	—	—	0.4	V	—
TL_CTRL pin High input threshold	V_{IH2}	—	2.0	—	—	V	—
SYNCHRONIZATION (SYNC)							
Low input threshold	V_{IL3}	—	—	—	0.4	V	—
High input threshold	V_{IH3}	—	2.0	—	—	V	—
SYNC terminal input current	V_{IC3}	V_{SYNC} = 3.3 V	—	33	60	μA	—
Oscillator							
Oscillator frequency	f_{OUT1}	R_T = 130 kΩ	465	490	515	kHz	—
Oscillator frequency range	f_{OUT2}		200	—	2000	kHz	—
External sync frequency range	f_{SYNC}	R_T = 130 kΩ f_{OUT1} = 490 kHz	520	—	730	kHz	—
Over-current protection							
Over-current threshold voltage 1	V_{OCP1}	(IN_HIGH – IN_LOW) OCPDET=0 V	110	125	140	mV	*1
Over-current threshold voltage 2	V_{OCP2}	(IN_HIGH – IN_LOW) OCPDET=3.3V	66	75	84	mV	*1
OCPDET pin Low input threshold	V_{IL4}	—	—	—	0.4	V	—
OCPDET pin High input threshold	V_{IH4}	—	2.0	—	—	V	—
OCPDET pin input current	V_{IC3}	V_{OCPDET} = 3.3 V	—	20	70	μA	—

Note: *1 : This parameter is tested with DC measurement.

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12 V , V_{OUT} = 5.0 V , R_T = 130 kΩ , R_{ADJ} = 12 kΩ , R_{SENSE} = 50 mΩ
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Notes
			Min	Typ	Max		
Over-voltage protection							
Over-voltage threshold voltage for VFB	V_{OVP1}	For FB	1.04	1.12	1.20	V	—
Over-voltage threshold voltage for VCC	V_{OVP2}	For VCC	40	45	50	V	—
Internal regulator							
Internal regulator output voltage	V_{REG}	C_{REG} = 1 uF	4.5	4.9	5.3	V	—
GND short protection							
Short detection voltage	V_{SCP}	Monitor FB	0.15	0.3	0.45	V	—
Current feedback function							
Current feedback output voltage1	V_{CFB1}	Monitor FBADJ V_{IN_HIGH} = 5 V,V_{FB} = 1.1 V at IN_HIGH – IN_LOW = 50 mV	180	200	220	mV	*1
Current feedback output voltage2	V_{CFB2}	Monitor FBADJ V_{IN_HIGH} = 5 V,V_{FB} = 1.1 V at IN_HIGH – IN_LOW = 105 mV	400	420	440	mV	*1
Current feedback factor	V_{CFBF}	$(V_{CFB2} - V_{CFB1})/\{4 \times (105\ mV - 50\ mV)\}$ No Switching	0.96	1	1.04	—	—

Note: *1 : This parameter is tested with DC measurement.

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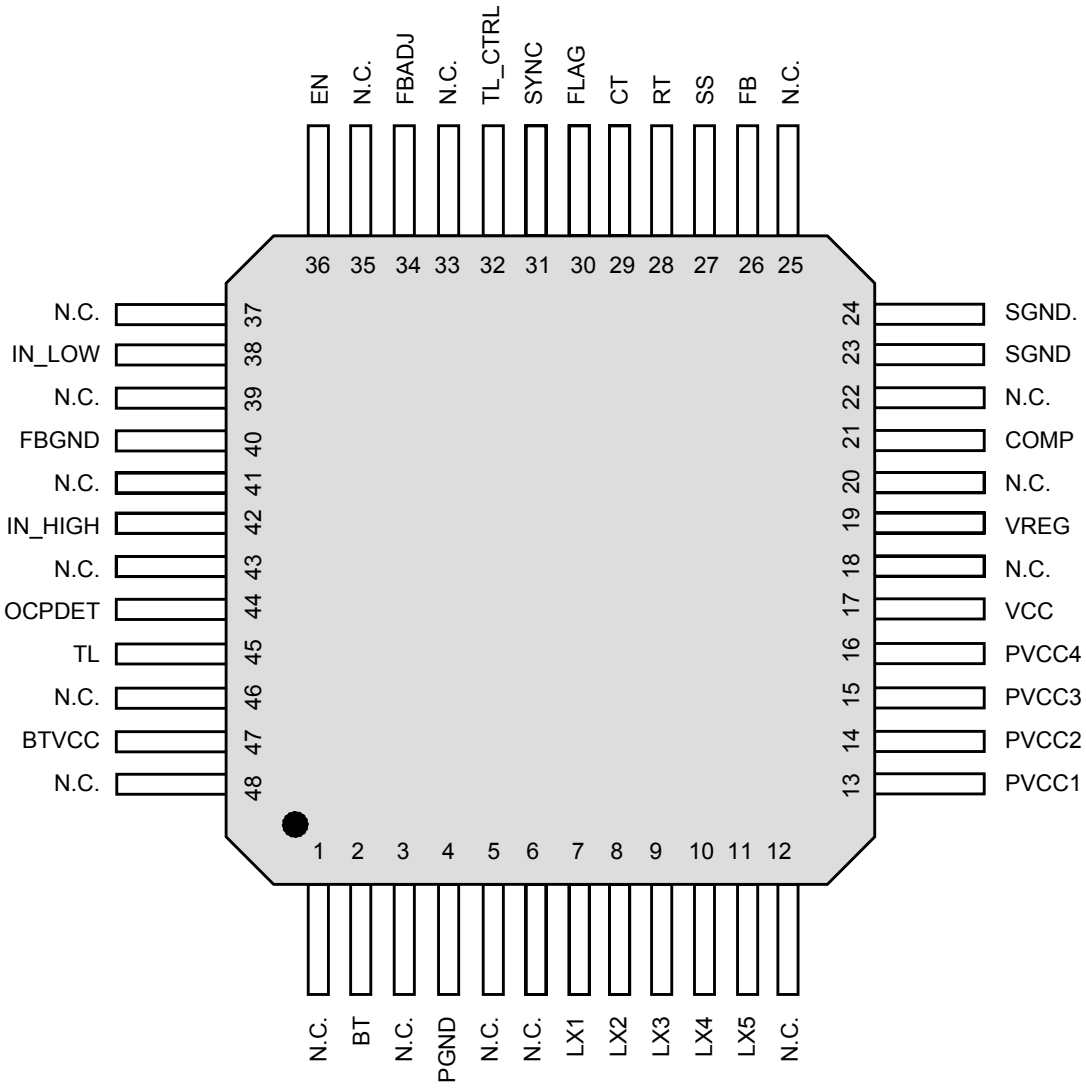
PIN CONFIGURATION

Top View



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PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	N.C.	—	No connection.
2	BT	Input	Connect to an external capacitor for Boot strap. Function for Boot strap to make the gate drive voltage of the built-in power MOSFET. Please connect capacitor between BT and LX. For noise prevention, please consider shortest possible wiring patterns on PCB.
3	N.C.	—	No connection.
4	PGND	Ground	Power ground pin.
5	N.C.	—	No connection.
6	N.C.	—	No connection.
7	LX1	Output	Power MOSFET output terminal. Function for switching operation between PVCC and GND. Please connect with external inductor and schottky diode. Impedance of wiring patterns is cause of low efficiency and noise, because large current flows with large amplitude. Therefore, please consider shortest possible wiring patterns on PCB.
8	LX2	Output	Power MOSFET output terminal. This pin is the same as above, Pin No.7.
9	LX3	Output	Power MOSFET output terminal. This pin is the same as above, Pin No.7.
10	LX4	Output	Power MOSFET output terminal. This pin is the same as above, Pin No.7.
11	LX5	Output	Power MOSFET output terminal. This pin is the same as above, Pin No.7.
12	N.C.	—	No connection.
13	PVCC1	Power Supply	Power supply terminal for Internal driver.
14	PVCC2	Power Supply	Power supply terminal for Internal driver.
15	PVCC3	Power Supply	Power supply terminal for Internal driver.
16	PVCC4	Power Supply	Power supply terminal for Internal driver.
17	VCC	Power Supply	Power supply terminal for Internal driver.
18	N.C.	—	No connection.
19	VREG	Output	Connect to external capacitor for internal regulator. It is Output pin of Power supply (LDO) for internal control circuit. Please connect capacitor between VREG and GND.
20	N.C.	—	No connection.
21	COMP	Output	Error amplifier output. Please connect external resistor and capacitor between COMP and FB for phase compensation.
22	N.C.	—	No connection.

Note : Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

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PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
23	SGND	Ground	Ground pin.
24	SGND	Ground	Ground pin.
25	N.C.	—	No connection.
26	FB	Input	Feedback terminal. The output voltage is fed back to this pin through a resistor divider network.
27	SS	Input	Soft-start capacitor connection pin. The output voltage at a start up is smoothly controlled by adjusting Soft Start time. Please connect capacitor between SS and GND.
28	RT	Input	Connect to an external resistor for adjustment of oscillation frequency. Please connect resistor between RT and GND. Basic output frequency is set up with above resistor value. If you are using SYNC function, please set input clock frequency higher than the reference frequency.
29	CT	Output	Low Pass filter function pin for PLL. Please connect capacitor between CT and GND. The capacitor value determines amount of output fluctuation during transient switch of external frequency. If you set larger capacitor, switching time is slower and hence smaller output fluctuation. It is no problem to set this pin open if you don't use it.
30	FLAG	Output	Error flag output pin This pin outputs low if DCDC continues to operate in OCP or SCP state longer than the timer latch duration. Please connect to pull-up resistor to High level voltage. FLAG is 5V cell. Please don't connect this pin over 5V directly.
31	SYNC	Input	External clock input for adjustment of oscillation frequency. Please input clock frequency which you use to in this pin, if you use SYNC function.
32	TL_CTRL	Input	Connect to high to disable shut-down function by OCP/SCP. If DCDC continue to detect OCP or SCP, FLAG is output over timer latch setting time. DCDC is turned off at the same time as outputting FLAG, when this pin input Low. DCDC continue to operate only outputting FLAG, when this pin input High. Please turn it off by EN control after FLAG is output.
33	N.C.	—	No connection.
34	FBADJ	Input / Output	Connect to an external resistor for adjustment of current feedback. Please connect resistor between FBADJ and GND.
35	N.C.	—	No connection.

Note : Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

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PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
36	EN	Input	Enable pin. DC-DC is stopped at Low level input, and it is started at High level input.
37	N.C.	—	No connection.
38	IN_LOW	Input	Connection to current sensing port. Please connect external resistor for current monitoring. Detection of over current and correction of current feed back by different voltage with IN_HIGH pin.
39	N.C.	—	No connection.
40	FBGND	Ground	Ground pin.
41	N.C.	—	No connection.
42	IN_HIGH	Input	Connection to current sensing port. Please connect external resistor for current monitoring. Detection of over current and correction of current feed back by different voltage with IN_LOW pin.
43	N.C.	—	No connection.
44	OCPDET	Input	Over current limit switch pin.
45	TL	Input	Connect to an external capacitor for adjustment of over-current detection time. Please connect capacitor between TL and GND. Set timer latch time by this capacitor value. It is no problem to set open this pin, if you don't use TL function.
46	N.C.	—	No connection.
47	BTVCC	Input	Boot strap output pin. This pin is power supply for the boot strap function that makes the gate drive voltage. Please connect with VREG.
48	N.C.	—	No connection.

Note : Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

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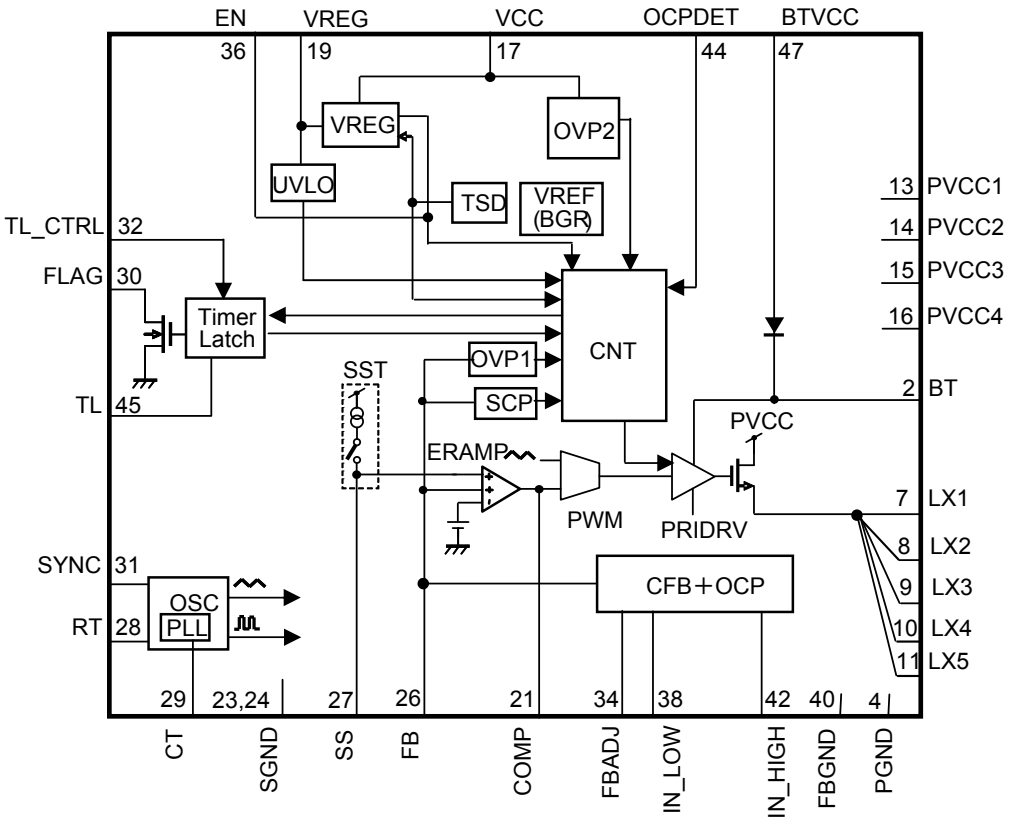
FUNCTIONAL BLOCK DIAGRAM



Notes : This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

1. Power ON/OFF timing

AN33017UA consists of one channel and it can be turned ON and OFF by using the EN pin.

EN ≥ 2.0 V : Enabled
EN ≤ 0.4 V : Disabled

1) Power ON Sequence :

V_{CC} rises to a desired voltage level.
(10 µs rise time or more is recommended to control and limit any abnormal current flow via the power transistor when V_{CC} is rising.)
Apply a voltage level of 2.0 V or higher at EN pin after V_{CC} is steady, and the DC-DC will begin to operate.
(It is possible to connect the EN pin to V_{CC} through a resistor, and, in that case, when V_{CC} rises, DC-DC will begin to operate.)
When V_{REG} voltage reaches 4.3 V and above, and after a delay time (charging time of the soft start capacitor) decided by an external capacitor, the DC-DC will start to operate.

2) Power OFF Sequence :

To turn OFF the DC-DC output, apply a voltage of 0.4 V or lower to EN pin.
V_{OUT} will drop after EN pin becomes Low.
(The discharge time is dependent on the applied load current and the feedback resistance connected at the output.)
The DC-DC will turn OFF if the V_{CC} level becomes low even before EN pin becomes low.
The above scenario occurs when the V_{REG} voltage decreases to 4.0 V or less.
(However, the DC-DC output voltage will also decrease with V_{CC} when the V_{CC} level drops below a certain minimum level required to maintain the output voltage level.)

3) Points to take note of when re-starting the DC-DC :

Please allow a waiting time of 10 ms or more for the discharge time of the soft start capacitor when starting up the DCDC again after turning it OFF.
The output voltage might overshoot without the soft start function working properly if the DC-DC is re-started immediately after it is turned OFF.

4) Points to take note of when shut down :

Please apply a voltage of Low level or lower to EN PIN when turn OFF the DC-DC.

5) Points to take note of pin connection :

VREG is utilized for internal circuits. Do not use it as power supply for other device.
Please put the external parts of RT pin and CT pin as closed as possible in the LSI terminal and arrange in such a way that the effect of noise will be reduced, such noise coming from LX pin and etc.

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OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

2. Start / Stop Control Timing Chart

1) EN pin ON/OFF operation sequence

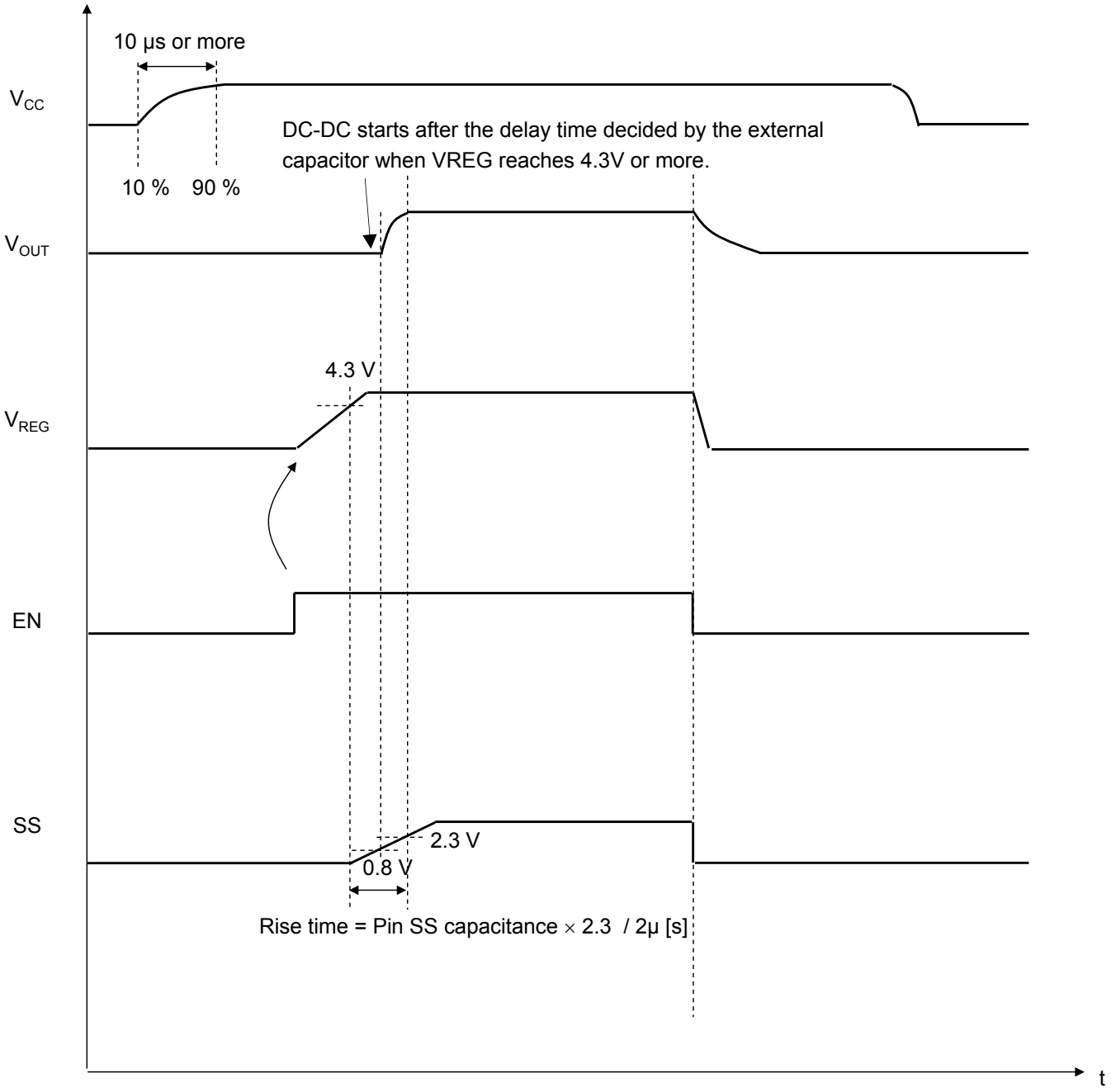

Figure : Power ON/OFF sequence by EN

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OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

2. Start / Stop Control Timing Chart (Continued)

2) ON/OFF operation sequence by VCC pin control (EN pin is connected to VCC).

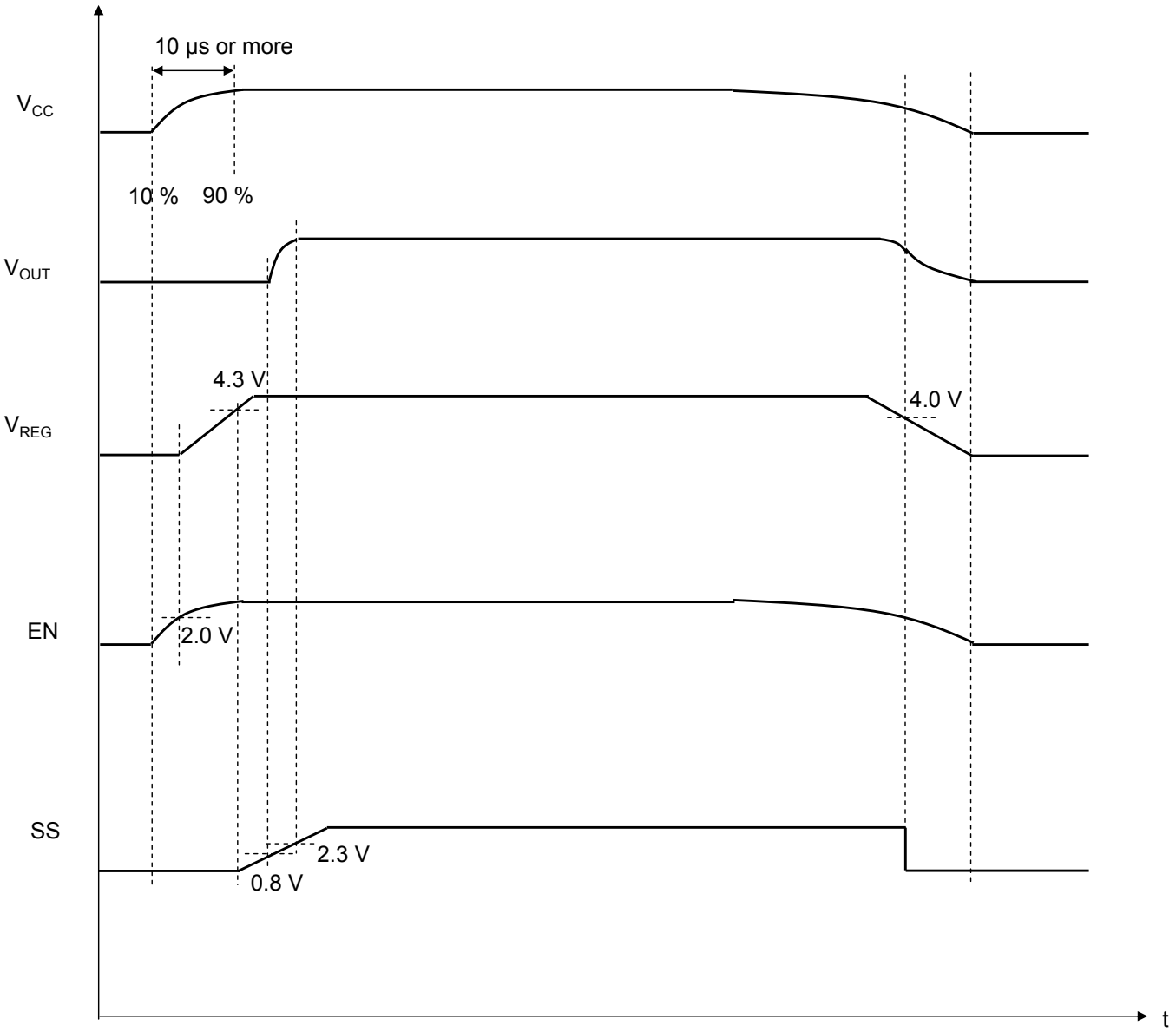

Figure : Power ON/OFF Timing (2)

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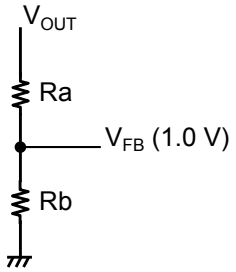
OPERATION (Continued)

3. Output voltage setting

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The output voltage of AN33017UA is set with the external feedback resistance divider arranged between the terminal FB and GND between the DC-DC output and the terminal FB. The output voltage is decided depending on the following equation.

$$Vout = 1.0 \times \left[1 + \frac{Ra}{Rb} \right]$$



4. Min/Max Duty Operation

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

MinDuty is decided by the minimum ON time. The minimum ON time, Ton (min), is the time that this IC can turn on the high side switch. This is decided by the gate capacitance of the high side switch and the internal timing delay. The following attention is necessary because in applications where the Input/Output voltage difference is great, and the switching frequency is high, there is a possibility to reach the limiting value of the minimum ON time. The minimum ON time, Ton (min), is about 200ns (max).

This IC has the function of MaxDuty, which will not exceed a certain definite value for safety reasons in case of abnormal circumstances. The following attention is necessary because in applications where the Input/Output voltage difference is close, and the switching frequency is high, there is a possibility to reach the limiting value of the minimum OFF time. The minimum OFF time, Toff (min), is about 200ns (max).

$$Ton(\min) < \frac{Vout}{Vin} \times \frac{1}{F}$$

$$Toff(\min) < (1 - \frac{Vout}{Vin}) \times \frac{1}{F}$$

*) F : Switching frequency

When operating near the Min/Max limited duty, the ripple voltage and the inductor current ripple increases even if the output voltage is stabilized. It is recommended to use on the condition when the turn on switching time and turn off switching time are 200ns or more.

*) Please take note of the output voltage setting when the switching frequency is high.

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OPERATION (Continued)

5. Oscillation Frequency

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The switching frequency of the built-in oscillator circuit can be set from 200 kHz to 2000 kHz, determined by the resistance of the terminal RT, set by external resistance. The setting accuracy of the frequency is approximately ±5%. The equation and the corresponding table are described as follows.

RT [kΩ]	OSC Frequency (kHz)	RT [kΩ]	OSC Frequency (kHz)
22	2022	91	674
24	1910	100	620
27	1764	110	569
30	1640	120	527
33	1530	130	490
36	1434	150	430
39	1352	160	406
43	1254	180	364
47	1169	200	330
51	1096	220	302
56	1015	240	278
62	934	270	249
68	864	300	225
75	796	330	206
82	738	360	190

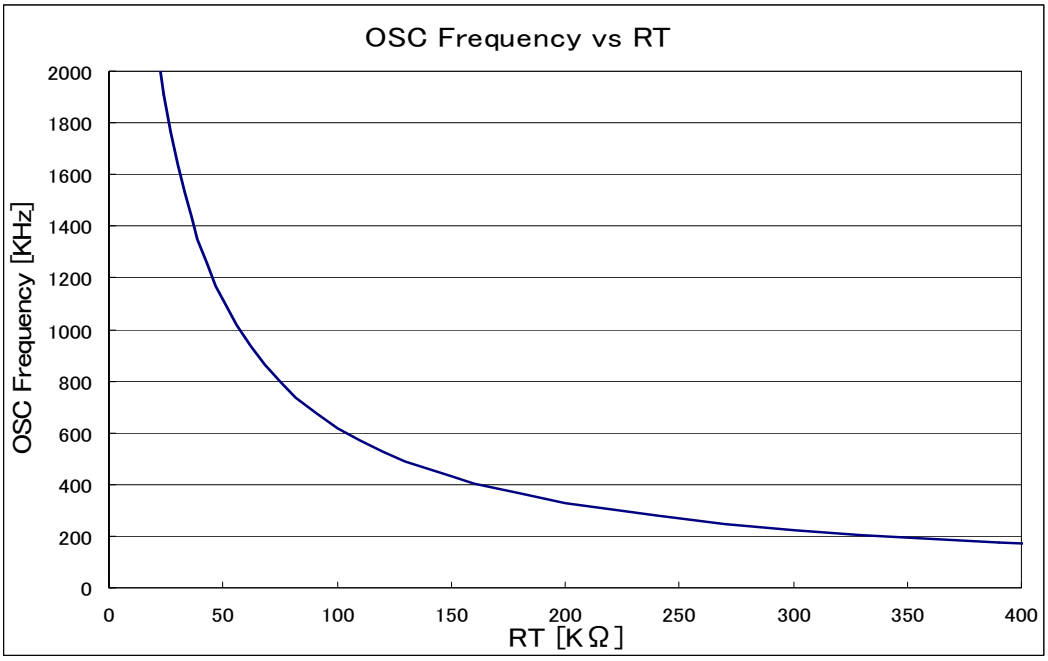

Figure : switching frequency vs external resistance

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OPERATION (Continued)

6. Over-Current Protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

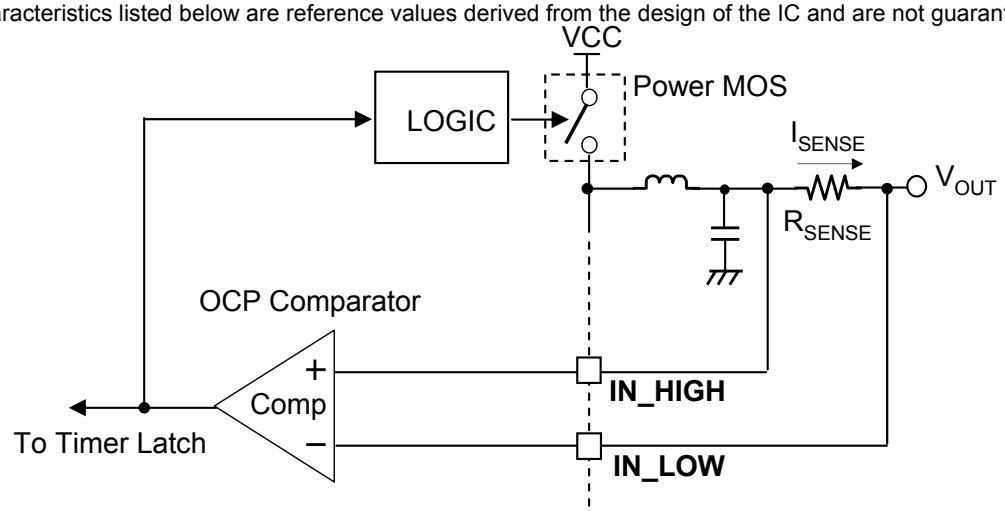

Figure : Over-Current Protection circuit block diagram

Over-current protection function (OCP) restrain output current level when IC detect that DC-DC output current is higher than setting level. It turns off the Power MOS in IC when the voltage difference of external resistance R_{SENSE} exceeds 125mV(Typ.) so as to stop the supply to DC-DC output. Detection current I_{SENSE} can be calculated as:

$$I_{SENSE} = 125mV / R_{SENSE}$$

For safety reason, OCP function is necessary. Please placed sense resistor (≥ 39mΩ) between IN_HIGH and IN_LOW as indicated in above figure.

The operation after OCP detection is different according to setting of TL_CTRL terminal.

The timing chart in case FLAG terminal pulled-up to VREG is shown in below.

[1] at TL_CTRL＝High

DC-DC continue to ON and OFF when OCP detect. It restrain average level of DC-DC output voltage and DC-DC output current.

[2] at TL_CTRL＝Low

FLAG output become low when you keep abnormal condition longer than setting time of Timer Latch function. For safety reason, please disable DC-DC by EN control when FLAG output become low.

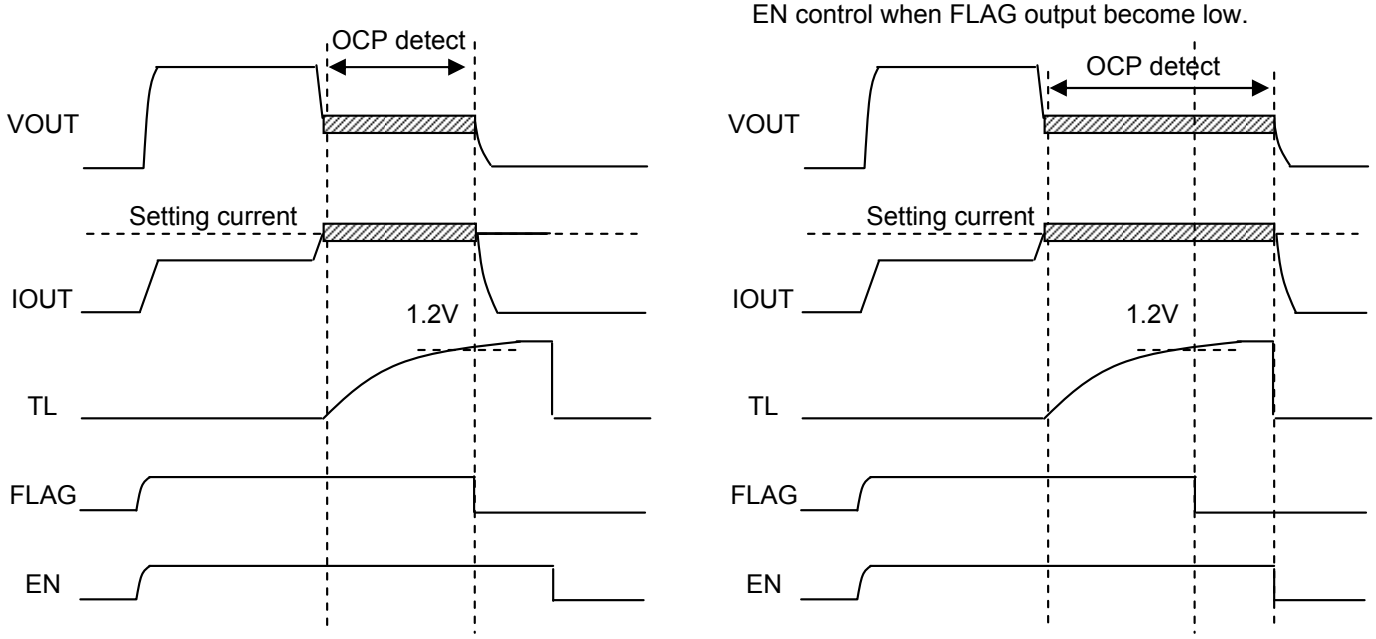

Figure : Method of detection of Over-Current Protection function

Established : 2012-11-29
Revised : 2013-06-10

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

7. Current Feedback function

This LSI includes a current feedback function whereby the suitable voltage can be provided V_USB which corrected a voltage descent at impedance Rcable of external connection cables. (Refer the following diagram.)
This function corrects the output voltage depending on a value of IOUT by feeding back to the voltage of FB by current feedback amplifier CFB, and controlling voltage differences of current sense resistor R_{SENSE} between both terminals so that it is expressed in the next expression.

$$\Delta V(adj) = \frac{4 \cdot R_{SENSE} \cdot Ra}{R_{RADJ}} \cdot I_{OUT}[V]$$

ΔV(adj) can be adjusted by the current feedback adjustment resistance (R_{RADJ}).
Therefore, The voltage variation of V_USB can control by offsetting with a voltage descent by the cable resistance by setting it like a following expression.

$$\frac{4 \cdot R_{SENSE} \cdot Ra}{R_{RADJ}} \cdot I_{OUT} = Rcable \cdot I_{OUT}$$

From the above expression, RRADJ shows as the following expression.

$$R_{RADJ} = \frac{4 \cdot R_{SENSE} \cdot Ra}{Rcable}$$

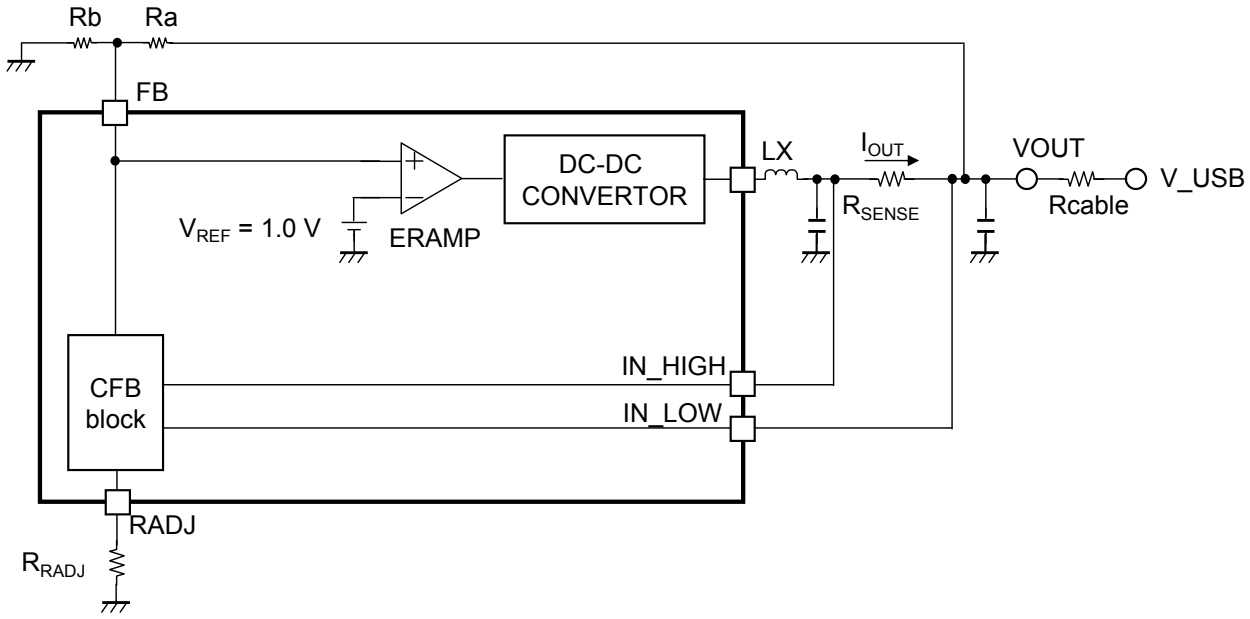

Figure : The diagram of current feed back function

Notes
- When you change a value of over current detection by current sense resistor R_{SENSE}, please be careful because output voltage variation is affected.
- When you change a setting of output voltage by resistance Ra, please be careful because output voltage variation is affected.
- Please refer to the figure of "I_{OUT} dependence of the permission level of the cable resistance" for the upper limit level of Rcable where voltage correction functions.

Established : 2012-11-29
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OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

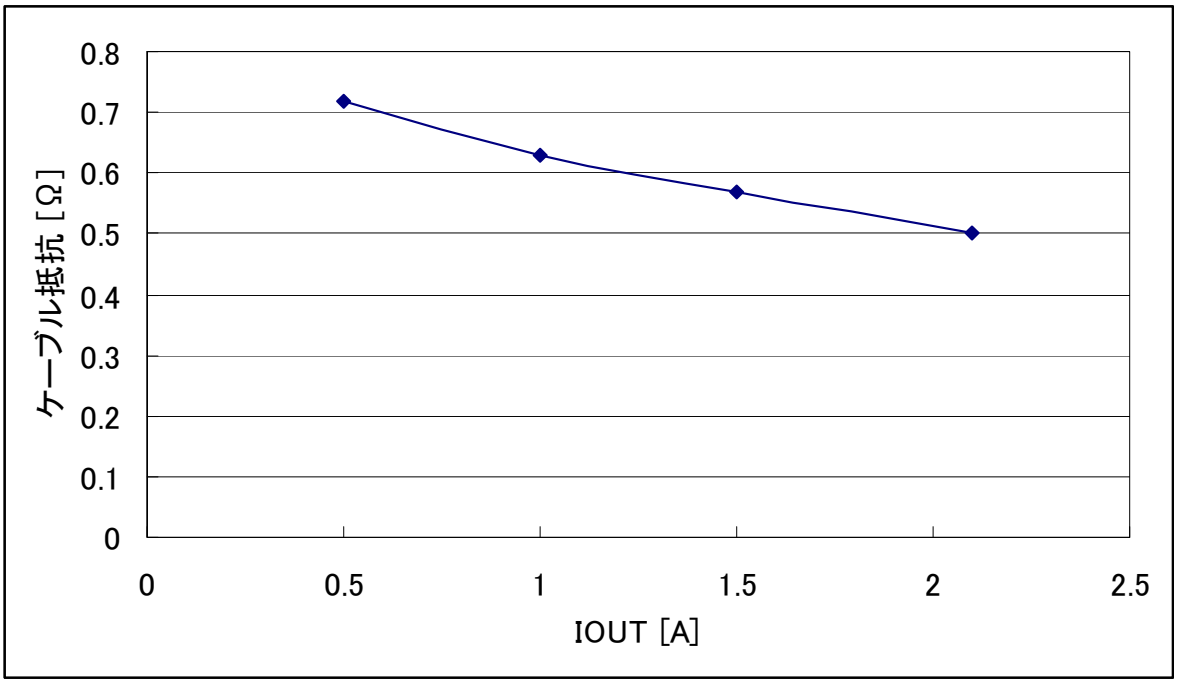
7. Current Feedback function (continued)

V_USB voltage is the following expression, which becomes the expression from the setting voltage by the FB resistance (Ra and Rb) and the expressions from both voltage descent and voltage correction by the cable resistance.

$$V\_USB = \left\{\left(1+\frac{R_a}{R_b}\right)\times 1.0\right\} - R_{cable}\cdot I_{OUT} + \frac{4\cdot R_{SENSE}\cdot R_a\cdot I_{OUT}}{R_{RADJ}}[V]$$

"× 1.0" of above expression indicates the reference voltage.

Precision of the V_USB voltage fluctuates depending on unevenness of the standard voltage or the each resistance. The upper limit level of Rcable when Ra, Rb and R_{SENSE} are respectively 30.8kΩ±0.05%, 7.5kΩ±0.05% and 50mΩ±1% shows the following figures, where V_USB voltage becomes the value at 5.25V from 4.97V in USB standard.
R_{RADJ}（±0.05%）of following figure is respectively 8.55kΩ, 9.77kΩ, 10.8kΩ and 12.3kΩ at IOUT＝0.5A、1.0A、1.5A and 2.1A.



Figure：I_{OUT} dependence of the permission level of the cable resistance

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OPERATION (Continued)

8. Over current protection setting

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

As a safety measure, a sensing resistor must be inserted between IM_HIGH pin & IN_LOW pin to enable the over-current protection function. Sensing resistor value of more than 39 mΩ is recommended.
If sensing resistor is set at less than 39 mΩ, the capacitor at TL pin should be as small as possible or open to minimize reaction time of Timer Latch block. Please consider the implementation of full evaluation and verification for this setting.
Take notice the power dissipation of Sensing resistor.

9. Over current detection level with switchable

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Over current detection level is switchable by OCPDET pin. The following expression shows voltage to detect over current at each conditions.

OCPDET	Voltage to detect over current	Over current at RSense=50mΩ
GND (Low input)	125mV	2.5A
VREG (High input)	75mV	1.5A

List : Settings of OCPDET pin

10. FLAG function after Over current / Short current detection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Stop this product by forcing EN pin to Low when detect OCP or SCP condition by FLAG pin.
In situation when IN_HIGH IN_LOW are less than 1.1V, do note that only SCP detection is active.

When FB is equal or lower than 0.3 V, short current detection is triggered, FLAG pin will be pull to Low state. The response timing is determined by TL pin capacitor value CTL (The response timing = CTL / 2μA ×1.2V).
Note that the pull down current drivability of FLAG pin is 1.2 mA.
Adjusting of FLAG response time in event of “over current” or “short current” condition is make possible by changing the capacitance of TL pin.
In the event of over current detection, FLAG pin will be pull to Low state. Once FLAG is pull to Low state, it will remained at Low state until IC is reset through EN pin.

11. Thermal Shut Down (TSD)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

When the LSI internal temperature becomes more than about 165℃, TSD operates and DC-DC turns off.

12. Input Over Voltage protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

When VCC is equal or higher than 45V overvoltage detection is triggered, Power MOS will be off and LX will stop switching.

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OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

13. Soft Start Timing and Setting

This LSI includes a soft start function whereby start-up time can be set to desired timing by adjusting the SS terminal capacitor (C_{SS}). By adjusting the soft-start time, rush current from the Power supply terminal can be limited and the start-up timing of the output voltage can be changed. The timing chart and the method of selecting the external capacitor value is shown in below.

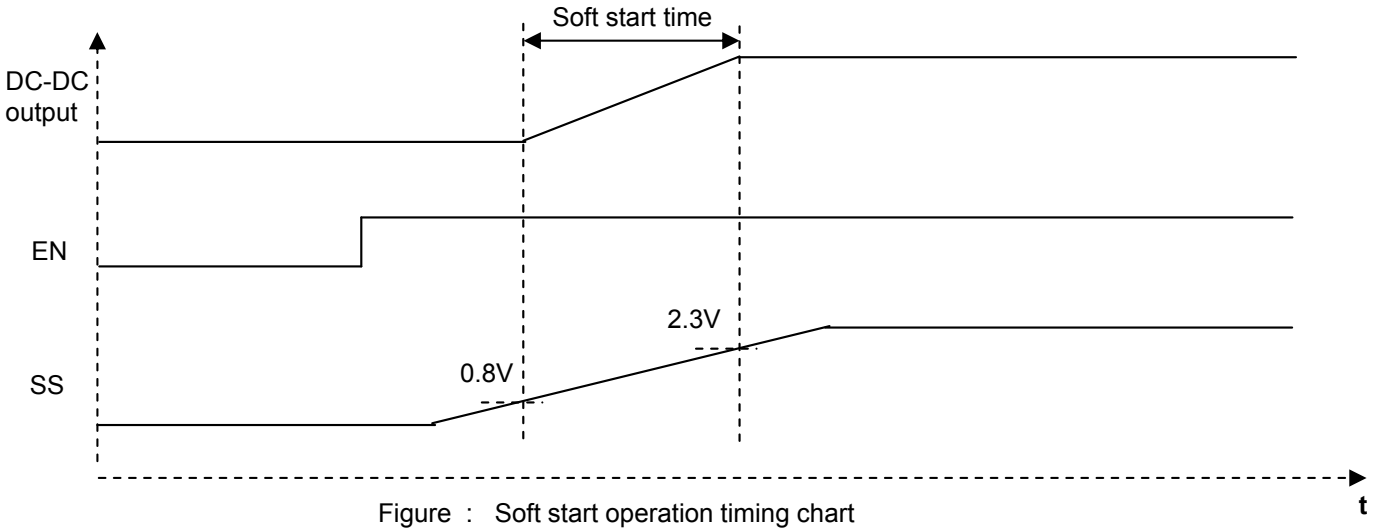

Figure : Soft start operation timing chart

Equation to set soft start time by C_{SS} : $\text{Soft-Start Time (s)} \approx \frac{1.5}{2.2\,\mu} \cdot C_{ss}$

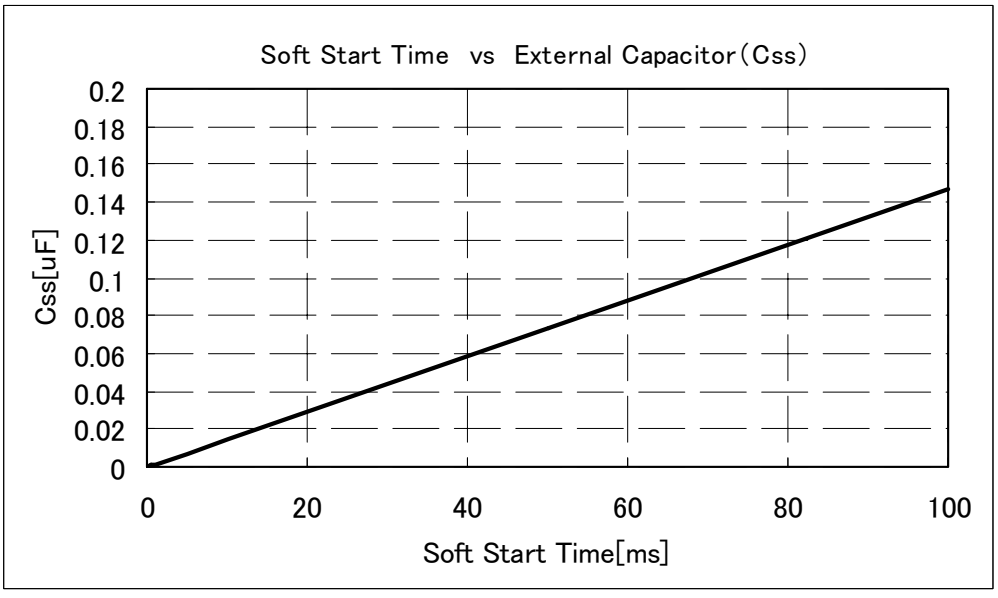

Figure : Soft Start Time vs C_{SS} Value (External Capacitor)

When this LSI is used for power supply of communication with external equipment, the communication may not possible during the soft-start period. Depending on the type of external equipment connected, in some cases, when the DC-DC is turned on, even though the soft start maybe halfway through, the voltage level is high enough to enable the communication to start. In such cases, the micro-controller may not recognize the equipment normally and therefore it is required to set the micro-controller to access all possible equipment after the above soft-start setting time.

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OPERATION (Continued)

14. Snubber circuit value Setting

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.
Snubber circuit should be put without fail for reducing the ringing of LX1~5 in light load condition.
Please use snubber resistance over 0.5W. Please refer to below for setting specific value.

This IC operate with discontinuous mode in light load condition. When DCDC operate with discontinuous mode and both schottky barrier diode and power transistor don't have conduction, ringing happens to LX pin in the end of every switching period by resonance circuit formed with inductor and parasitic capacitor. It is possible to reduce the ringing generated in LX pin by adding snubber circuit. The procedure below shows snubber circuit value setting. In addition, design snubber circuit with load resistance consideration.

Procedure1. Measure LX ringing frequency with discontinuous mode. Figure shows ringing frequency of 2.3MHz.

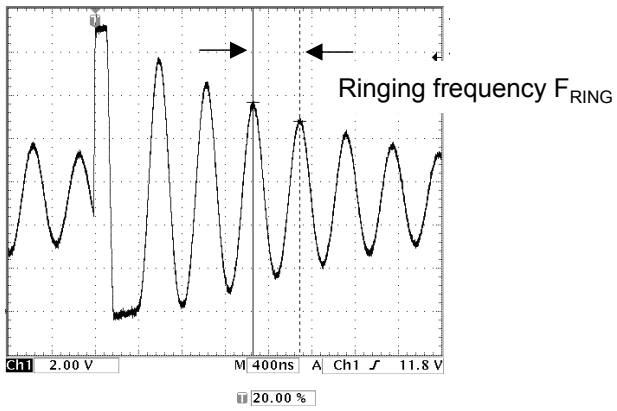

Figure : LX waveform with discontinuous mode. (without snubber circuit)

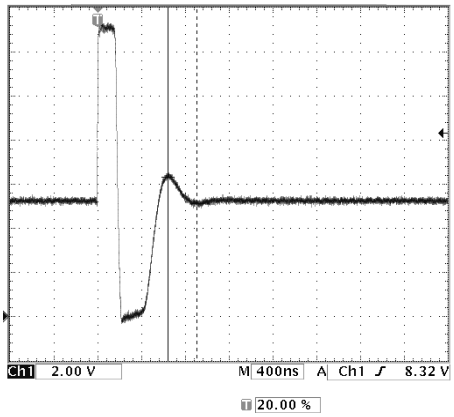

Figure : LX waveform with discontinuous mode. (with snubber circuit)

Procedure2. Parasitic capacitor between LX to GND of board that mounts IC and Ringing frequency F_{RING} has the following relational expression.

$$F_{RING} = \frac{1}{2\pi\sqrt{(L+L_p)\times Cp}}[Hz]$$

Cp is calculated with the above expression. It is assumed Lp (parasitic inductor) is low enough compared with L.
Cp is calculated 480pF with Ringing frequency=2.3MHz and L=10uH condition.
C1 needs to be 5～10 times of Cp capacitor. The larger capacitor value is, the more ringing decreases.
Therefore 4700pF is selected.

Procedure3. Impedance R1 is calculated by parasitic capacitor Cp.

$$R1 = \sqrt{(L/C_p}[\Omega]$$

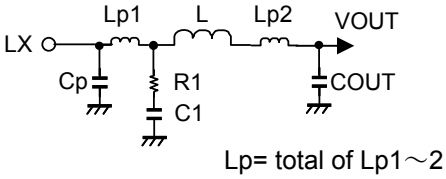

Figure : Snubber circuit value

Using the expression above, R1=150Ω is calculated.
Please use snubber resistance over 0.5W.

Figure shows decreased LX pin ringing waveform with snubber circuit.
Added snubber circuit value depends on board pattern. Therefore ringing frequency F_{RING} is confirmed and calculated and used optimum value from the above expression.

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OPERATION (Continued)

15. Load resistance, Rload setting

Note) The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

Load resistance, Rload is selected by the following confirmation of BT-LX voltage.
Figure in below shows BT waveform, LX waveform, BT-LX voltage.

Condition: Vcc=13.2V, VOUT=5V, Iload=0A

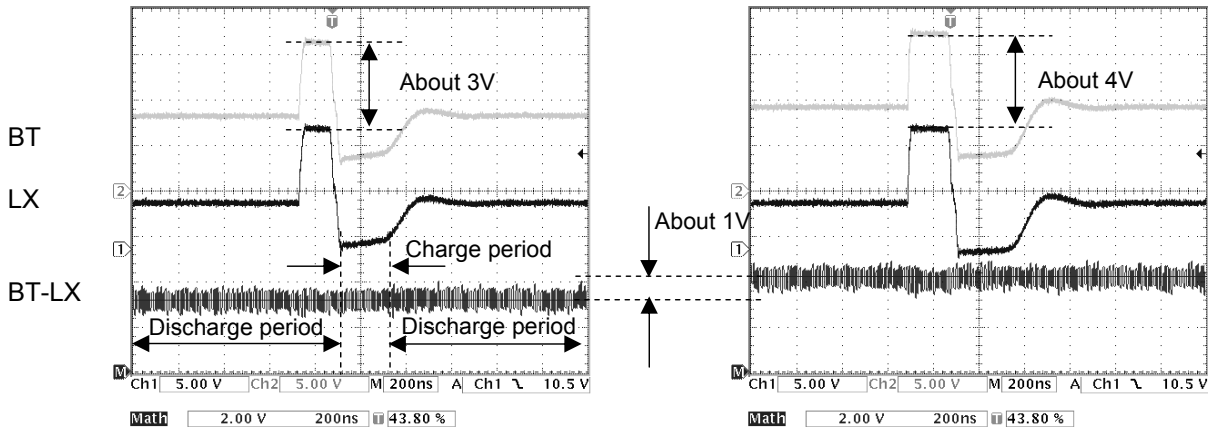

Figure : BT waveform, LX waveform, BT-LX voltage (without Rload condition)

Figure : BT waveform, LX waveform, BT-LX voltage (with 330Ω condition)

When LX is Low, Boot strap capacitor is charged from BTVCC. And then it will be discharged. Discharge period is longer in no load condition, therefore BT-LX voltage level goes down and it becomes about 3V.(Refer to Figure above left） The larger the load current is, the shorter the discharge period is, therefore BT-LX voltage level goes up and it reaches desired voltage.(about 4V) (Refer to Figure above right)
Load resistance, Rload is calculated by the load current, Iload and the following expressions.

$$R_{LOAD} = \frac{VOUT}{I_{LOAD}} [\Omega]$$

Example) When VOUT=5V, Iload=15mA condition, the calculated Rload=330 Ω.

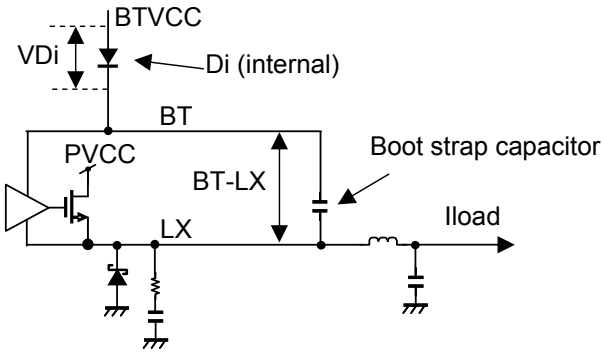

Figure : Boot Strap external circuit

Desired voltage is determined by BTVCC voltage and internal diode shown in Figure.
Example） When BTVCC is connected to VREG, the voltage level is about 4.2V, where BTVCC=4.9V and VDi=0.7V.

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APPLICATIONS INFORMATION

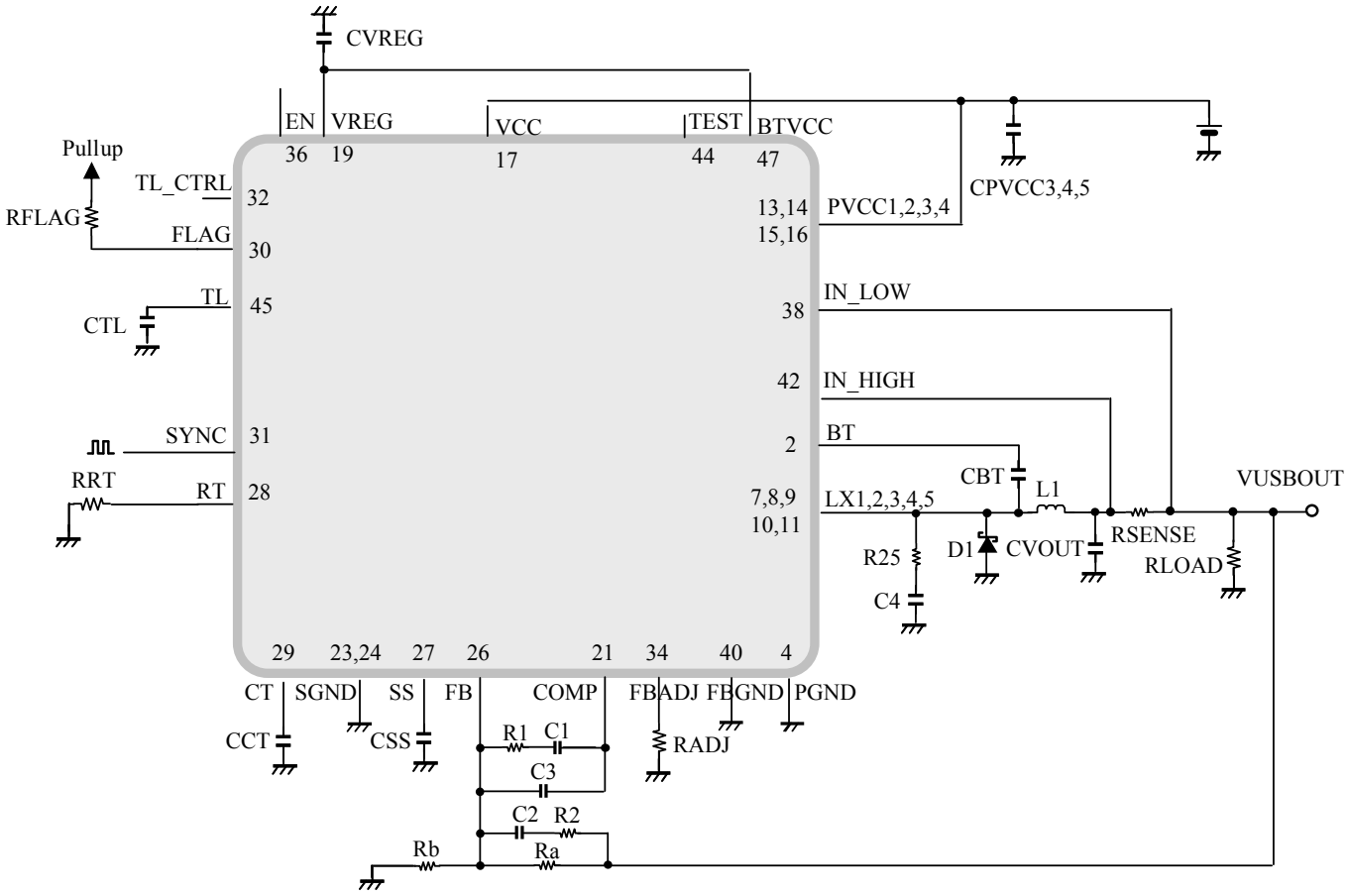

Figure : Application circuit

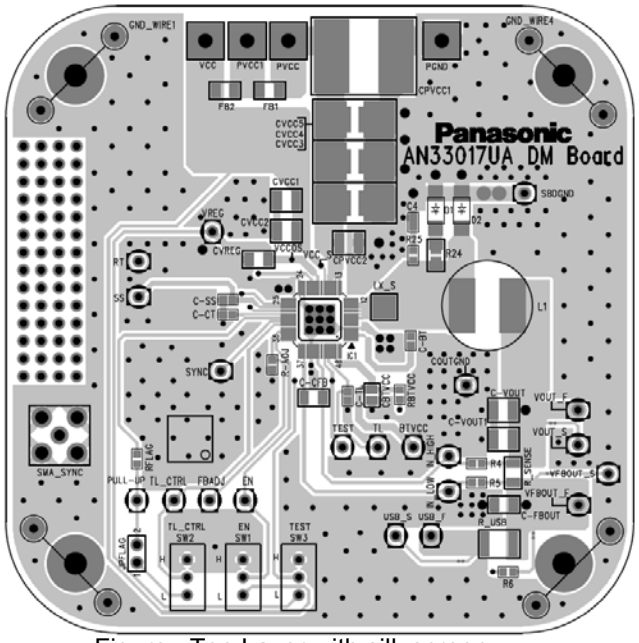

Figure : Top Layer with silk screen
(Top View) with Evaluation board

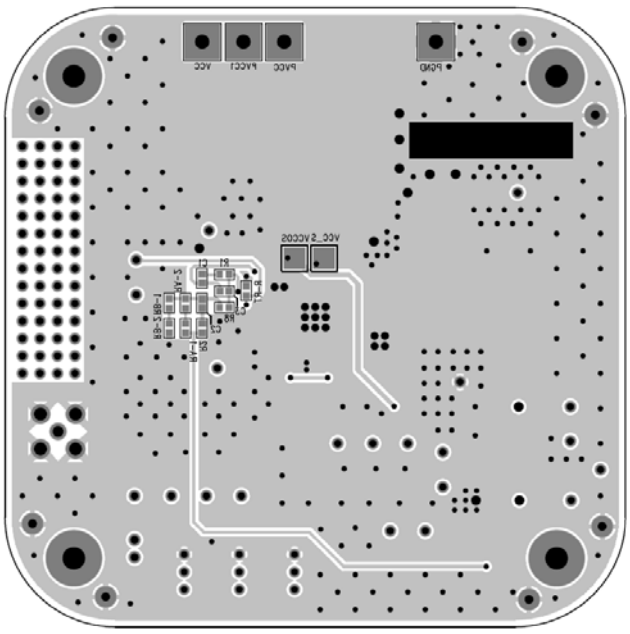

Figure : Bottom Layer with silk screen
(Bottom View) with Evaluation board

Notes) This application circuit and layout is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

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APPLICATIONS INFORMATION (Continued)

Table : Recommended component

Reference	Part Name	size	Value	Maker	Description
CBT,CCT,CSS,CTL	GCM188R11C104KA01J	JIS1608_[EIA0603]	0.1uF	Murata	Setting Capacitor
C1	GCM1882C1H222JA01J	JIS1608_[EIA0603]	2.2nF	Murata	Compensation Capacitor
C2	GCM1882C1H471JA01J	JIS1608_[EIA0603]	470pF	Murata	Compensation Capacitor
C3	GCM1882C1H270JA01J	JIS1608_[EIA0603]	27pF	Murata	Compensation Capacitor
C4	GRM188B11H472KA01	JIS1608_[EIA0603]	4700pF	Murata	Snubber Capacitor
CVREG	GCM188R71C105KA49J	JIS1608_[EIA0603]	1uF	Murata	VREG Capacitor
CPVCC3,4,5	CKG57NX7R1H226MT	JIS5750[EIA2220]	22uF	TDK	Input Capacitor
CVOUT	TMK325C7226MM-T	JIS3225_[EIA1210]	22uF	TAIYO,YUDEN	Output Capacitor
L1	CDRH8D43-100NC	8.3(L) x 8.3(W)	10uH	SUMIDA	Inductor
IC1	AN33017UA	9.0(L) x 9.0 (W)	-	Panasonic	1ch DC-DC Converter
D1	DB24602	3.8(L) x 2.4(W)	-	Panasonic	Schottky Diode
R1	ERA3AEB752V	JIS1608_[EIA0603]	R=7.5K	Panasonic	Compensation & Feedback Resistor
R2	ERA3AEB152V	JIS1608_[EIA0603]	R=1.5K	Panasonic	Compensation & Feedback Resistor
R25	ERJ14YJ151U (150ohm 0.5W)	JIS3225_[EIA1210	R=150	Panasonic	Snubber Resistor
Ra	ERA3AEB303V	JIS1608_[EIA0603]	R=30K	Panasonic	Compensation & Feedback Resistor
Rb	ERA3AEB752V	JIS1608_[EIA0603]	R=7.5K	Panasonic	Compensation & Feedback Resistor
RFLAG	ERA3AEB204V	JIS1608_[EIA0603]	R=200K	Panasonic	Pull-up Resistor
RT	ERA3AEB134V	JIS1608_[EIA0603]	R=130K	Panasonic	OSC Setting Resistor
RADJ	ERA3AEB123V	JIS1608_[EIA0603]	R=12K	Panasonic	CFB Adjust Resistor
RLOAD	ERJ3GEYJ331	JIS1608_[EIA0603]	R=330	Panasonic	Load Resistor
RSENSE	ERJ8BWFR050V	JIS3216[EIA1206]	R=50m	Panasonic	OCP Sense Resistor

Notes)
- Snubber circuit should be put without fail for reducing the ringing of LX1~5 in light load condition. Please use snubber resistance over 0.5W. Please refer to “OPERATION13.Snubber circuit value setting” for setting specific value.
- SS pin capacitor, CSS and TL pin capacitor CTL should be put 0.1uF. If you change these components, please keep “ CTL > CSS × 0.9 “ relation.

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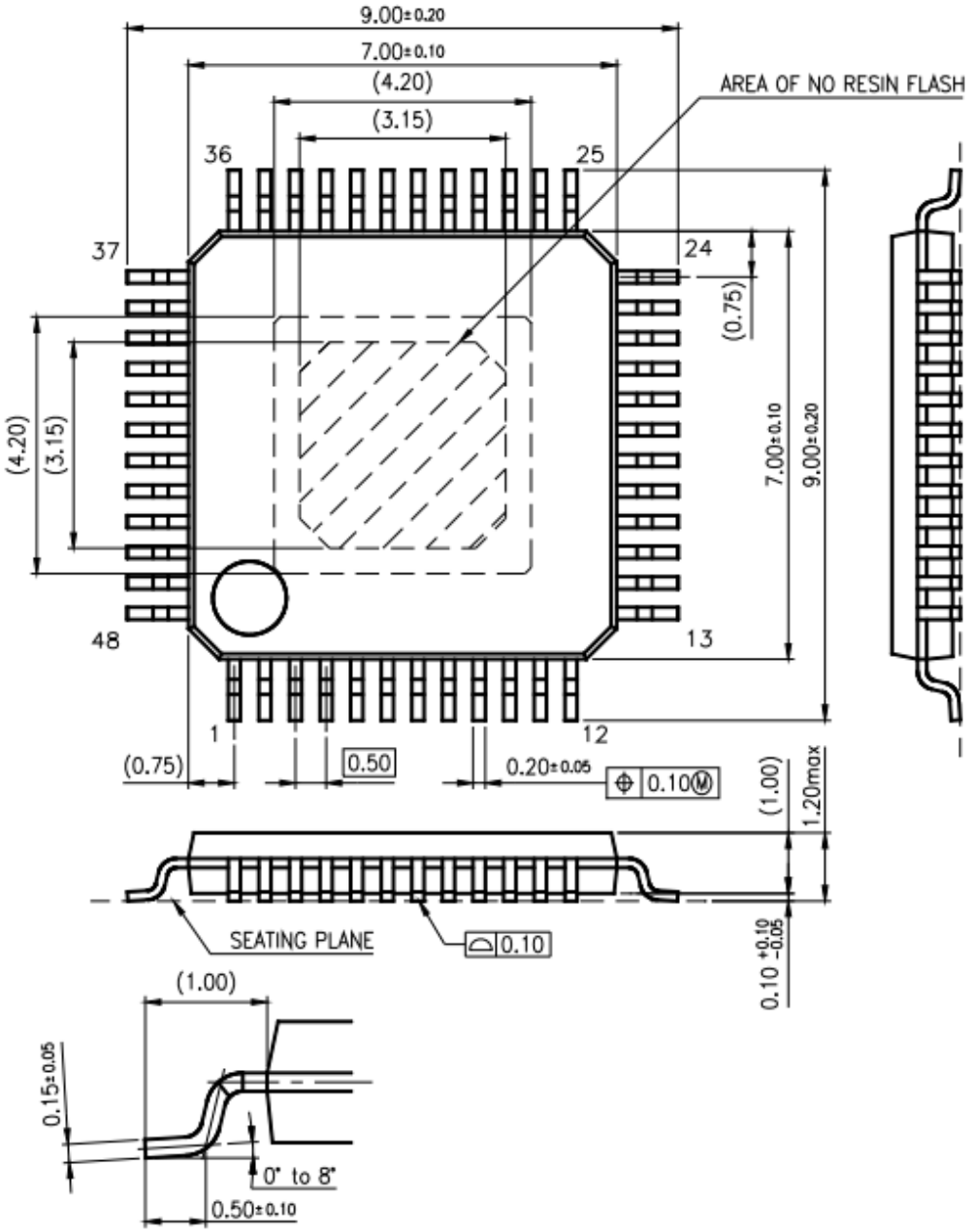
PACKAGE INFORMATION (Reference Data)

Outline Drawing

Package Code : HQFP048-P-0707B

Unit : mm



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

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IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
4. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
5. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
6. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
7. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
8. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
9. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
10. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
11. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
12. Verify the risks which might be caused by the malfunctions of external components.
13. Connect the metallic plate (fin) on the back side of the IC to the GND potential. The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.
14. Do not apply voltage to the metallic plate (fin) on the back side of the IC and do not connect it to the GND pattern.

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Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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