Application Note
APT0201 Rev. B
July 1, 2002

IGBT Tutorial

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Introduction

With the combination of an easily driven MOS gate and low conduction loss, IGBTs quickly displaced power bipolar transistors as the device of choice for high current and high voltage applications. The balance in tradeoffs between switching speed, conduction loss, and ruggedness is now being ever finely tuned so that IGBTs are encroaching upon the high frequency, high efficiency domain of power MOSFETs. In fact, the industry trend is for IGBTs to replace power MOSFETs except in very low current applications. To help understand the tradeoffs and to help circuit designers with IGBT device selection and application, this application note provides a relatively painless overview of IGBT technology and a walkthrough of Advanced Power Technology IGBT datasheet information.

How to Select an IGBT

This section is intentionally placed before the technical discourse. Answers to the following set of burning questions will help determine which IGBT is appropriate for a particular application. The differences between Non Punch-Through (NPT) and Punch-Through (PT) devices as well as terms and graphs will be explained later.

1. What is the operating voltage? The highest voltage the IGBT has to block should be no more than 80% of the V_{CES} rating.
2. Is it hard or soft switched? A PT device is better suited for soft switching due to reduced tail current, however a NPT device will also work.
3. What is the current that will flow through the device? The first two numbers in the part number give a rough indication of the usable current. For hard switching applications, the usable frequency versus current graph is helpful in determining whether a device will fit the application. Differences between datasheet test conditions and the application should be taken into account, and an example of how to do this will be given later. For soft switching applications, the I_{C2} rating could be used as a starting point.
4. What is the desired switching speed? If the answer is “the higher, the better”, then a PT device is the best choice. Again, the usable frequency versus current graph can help answer this question for hard switching applications.
5. Is short circuit withstand capability required? For applications such as motor drives, the answer is yes, and the switching frequency also tends to be relatively low. An NPT device would be required. Switch mode power supplies often don’t require short circuit capability.

IGBT Overview

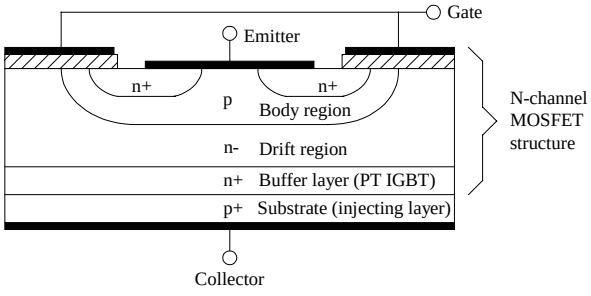

Figure 1 N-Channel IGBT Cross Section

An N-channel IGBT is basically an N-channel power MOSFET constructed on a p-type substrate, as illustrated by the generic IGBT cross section in Figure 1. (PT IGBTs have an additional n+ layer as well as will be explained.) Consequently, operation of an IGBT is very similar to a power MOSFET. A positive voltage applied from the emitter to gate terminals causes electrons to be drawn toward the gate terminal in the body region. If the gate-emitter voltage is at or above what is called the threshold voltage, enough electrons are drawn toward the gate to form a conductive channel across the body region, allowing current to flow from the collector to the emitter. (To be precise, it allows electrons to flow from the emitter to the collector.) This flow of electrons draws positive ions, or holes, from the p-type substrate into the drift region toward the emitter. This leads to a couple of simplified equivalent circuits for an IGBT as shown in Figure 2.

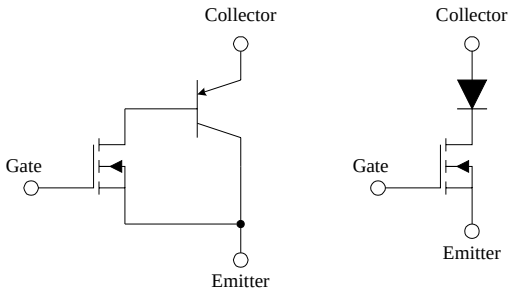

Figure 2 IGBT Simplified Equivalent Circuits

The first circuit shows an N-channel power MOSFET driving a wide base PNP bipolar transistor in a Darlington configuration. The second circuit simply shows a diode in series with the drain of an N-channel power MOSFET. At first glance, it would seem that the on state voltage across the IGBT would be one diode drop higher than for the N-channel power MOSFET by itself. It is true in fact that the on state voltage across an IGBT is always at least one diode drop. However, compared to a power MOSFET of the same die size and operating at the same temperature and current, an IGBT can have significantly lower on state voltage. The reason for this is that a MOSFET is a majority carrier device only. In other words, in an N-channel MOSFET only electrons flow. As mentioned before, the p-type substrate in an N-channel IGBT injects holes into the drift region. Therefore, current flow in an IGBT is composed of both electrons and holes. This injection of holes (minority carriers) significantly reduces the effective resistance to current flow in the drift region. Stated otherwise, hole injection significantly increases the conductivity, or the conductivity is modulated. The resulting reduction in on state voltage is the main advantage of IGBTs over power MOSFETs.

Nothing comes for free of course, and the price for lower on state voltage is slower switching speed, especially at turn-off. The reason for this is that during turn-off the electron flow can be stopped rather abruptly, just as in a power MOSFET, by reducing the gate-emitter voltage below the threshold voltage. However, holes are left in the drift region, and there is no way to remove them except by voltage gradient and recombination. The IGBT exhibits a tail current during turn-off until all the holes are swept out or recombined. The rate of recombination can be controlled, which is the purpose of the n+ buffer layer shown in Figure 1. This buffer layer quickly absorbs trapped holes during turn-off. Not all IGBTs incorporate an n+ buffer layer; those that do are called punch-through (PT), those that do not are called non punch-through (NPT). PT IGBTs are sometimes referred to as asymmetrical, and NPT as symmetrical.

The other price for lower on state voltage is the possibility of latchup if the IGBT is operated well outside the datasheet ratings. Latchup is a failure mode where the IGBT can no longer be turned off by the gate. Latchup can be induced in any IGBT through misuse. Thus the latchup failure mechanism in IGBTs warrants some explanation.

The basic structure of an IGBT resembles a thyristor, namely a series of PNPN junctions. This can be explained by analyzing a more detailed equivalent circuit model for an IGBT shown in Figure 3.

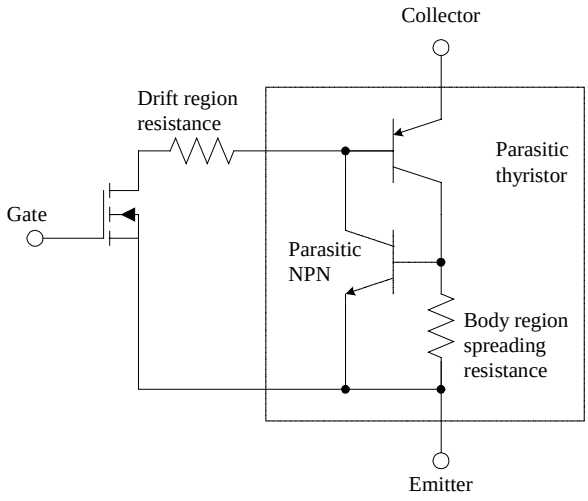

Figure 3 IGBT Model Showing Parasitic Thyristor

A parasitic NPN bipolar transistor exists within all N-channel power MOSFETS and consequently all N-

channel IGBTs. The base of this transistor is the body region, which is shorted to the emitter to prevent it from turning on. Note however that the body region has some resistance, called body region spreading resistance, as shown in Figure 3. The P-type substrate and drift and body regions form the PNP portion of the IGBT. The PNPN structure forms a parasitic thyristor. If the parasitic NPN transistor ever turns on and the sum of the gains of the NPN and PNP transistors are greater than one, latchup occurs. Latchup is avoided through design of the IGBT by optimizing the doping levels and geometries of the various regions shown in Figure 1.

The gains of the PNP and NPN transistors are set so that their sum is less than one. As temperature increases, the PNP and NPN gains increase, as well as the body region spreading resistance. Very high collector current can cause sufficient voltage drop across the body region to turn on the parasitic NPN transistor, and excessive localized heating of the die increases the parasitic transistor gains so their sum exceeds one. If this happens, the parasitic thyristor latches on, and the IGBT cannot be turned off by the gate and may be destroyed due to over-current heating. This is static latchup. High dv/dt during turn-off combined with excessive collector current can also effectively increase gains and turn on the parasitic NPN transistor. This is dynamic latchup, which is actually what limits the safe operating area since it can happen at a much lower collector current than static latchup, and it depends on the turn-off dv/dt. By staying within the maximum current and safe operating area ratings, static and dynamic latchup are avoided regardless of turn-off dv/dt. Note that turn-on and turn-off dv/dt, overshoot, and ringing can be set by an external gate resistor (as well as by stray inductance in the circuit layout).

PT versus NPT Technology

Conduction Loss

For a given switching speed, NPT technology generally has a higher $V_{CE(on)}$ than PT technology. This difference is magnified further by fact that $V_{CE(on)}$ increases with temperature for NPT (positive temperature coefficient), whereas $V_{CE(on)}$ decreases with temperature for PT (negative temperature coefficient). However, for any IGBT, whether PT or NPT, switching loss is traded off against $V_{CE(on)}$. Higher speed IGBTs have a higher $V_{CE(on)}$; lower speed IGBTs have a lower $V_{CE(on)}$. In fact, it is possible that a very fast PT device can have a higher $V_{CE(on)}$ than a NPT device of slower switching speed.

Switching Loss

For a given $V_{CE(on)}$, PT IGBTs have a higher speed switching capability with lower total switching energy. This is due to higher gain and minority carrier lifetime reduction, which quenches the tail current.

Ruggedness

NPT IGBTs are typically short circuit rated while PT devices often are not, and NPT IGBTs can absorb more avalanche energy than PT IGBTs. NPT technology is more rugged due to the wider base and lower gain of the PNP bipolar transistor. This is the main advantage gained by trading off switching speed with NPT technology. It is difficult to make a PT IGBT with greater than 600 Volt V_{CES} whereas it is easily done with NPT technology. Advanced Power Technology does offer a series of very fast 1200 Volt PT IGBTs, the Power MOS 7® IGBT series.

Temperature Effects

For both PT and NPT IGBTs, turn-on switching speed and loss are practically unaffected by temperature. Reverse recovery current in a diode however increases with temperature, so temperature effects of an external diode in the power circuit affect IGBT turn-on loss.

For NPT IGBTs, turn-off speed and switching loss remain relatively constant over the operating temperature range. For PT IGBTs, turn-off speed degrades and switching loss consequently increases with temperature. However, switching loss is low to begin with due to tail current quenching.

As mentioned previously, NPT IGBTs typically have a positive temperature coefficient, which makes them well suited for paralleling. A positive temperature coefficient is desirable for paralleling devices because a hot device will conduct less current than a cooler device, so all the parallel devices tend to naturally share current. It is a misconception however that PT IGBTs cannot be paralleled because of their negative temperature coefficient. PT IGBTs can be paralleled because of the following:

- Their temperature coefficients tend to be almost zero and are sometimes positive at higher current.
- Heat sharing through the heat sink tends to force devices to share current because a hot device will heat its neighbors, thus lowering their on voltage.
- Parameters that affect the temperature coefficient tend to be well matched between devices.

IGBTs from Advanced Power Technology

Advanced Power Technology offers three series of IGBTs to cover a broad range of applications:

- Power MOS 7® Series – 600V and 1200V PT technology IGBTs designated by 'GP' in the part number, one of the fastest IGBTs on the market, designed for operation at high frequencies and/or for tail current sensitive applications such as soft switching.
- Thunderbolt® Series – 600V only NPT technology IGBTs designated by 'GT' in the part number, fast IGBTs capable of 150kHz in hard switching applications, short circuit rated rugged devices suitable for switch-mode power supplies as well as motor drives.
- Fast Series – 600V and 1200V NPT technology IGBTs designated by 'GF' in the part number, short circuit rated rugged devices with low on voltage suitable for hard switching operation below 100kHz such as in motor drives.

Power MOS 7® IGBTs from APT are unique in that they are designed to switch extremely fast, and they incorporate a proprietary metal gate and open cell structure. The result is extremely low internal equivalent gate resistance (EGR), typically a fraction of an Ohm; one to two orders of magnitude lower than for poly-silicon gate devices. Low EGR enables faster switching and consequently lower switching loss. The metal gate and open cell structure also result in extremely uniform and fast excitation of the gate, minimizing hot spots during switching transients and improving reliability. An open cell structure is also more tolerant of defects induced during the manufacturing process.

Datasheet Walkthrough

The intent of datasheets provided by APT is to include relevant information that is useful and convenient for the power circuit designer, both for selection of the appropriate device as well as predicting its performance in an application. Graphs are provided to enable the designer to extrapolate from one set of operating conditions to another. It should be noted though that test results are very strongly circuit dependent, especially on stray emitter inductance but also on stray collector inductance and gate drive circuit design and layout. Different test circuits yield different results.

The following walkthrough provides definition of terms in APT datasheets as well as further details on IGBT characteristics.

Heading

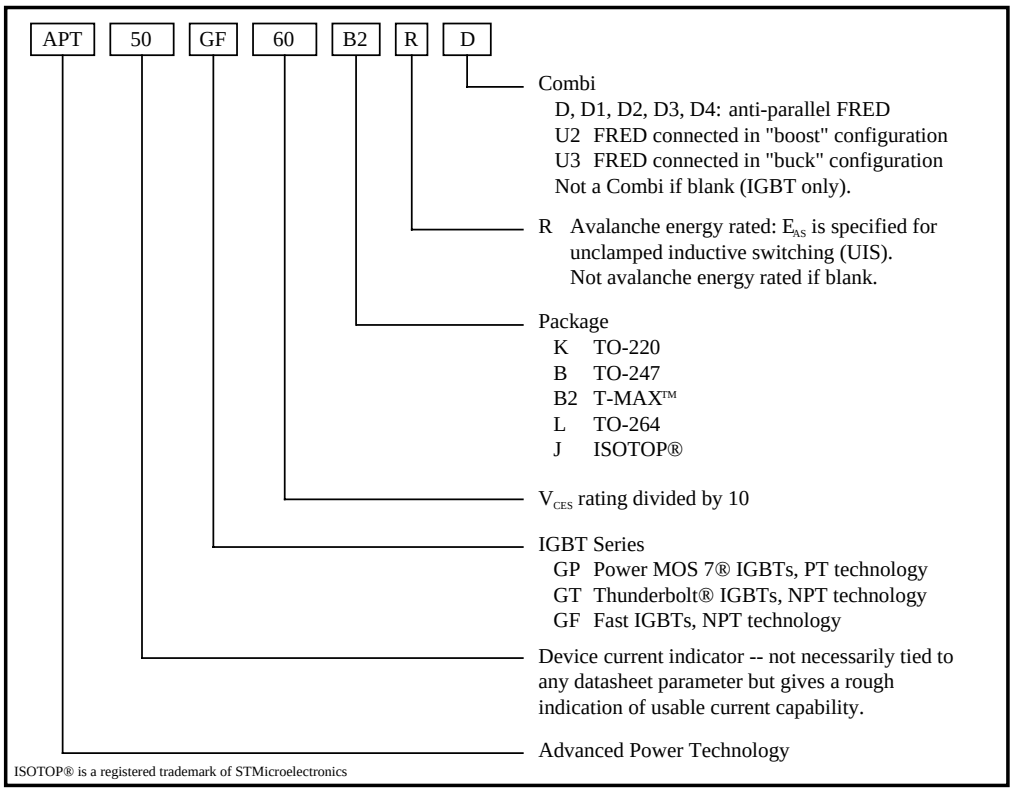

Figure 4 APT Part Numbering for IGBTs

Maximum Ratings

V_{CES} – Collector-Emitter Voltage

This is a rating of the maximum voltage between the collector and emitter terminals with the gate shorted to the emitter. This is a maximum rating, and depending on temperature, the maximum permissible collector-emitter voltage could actually be less than the V_{CES} rating. See the description of BV_{CES} in Static Electrical Characteristics.

V_{GE} – Gate-Emitter Voltage

V_{GE} is a rating of the maximum continuous voltage between the gate and emitter terminals. The purposes of this rating are to prevent breakdown of the gate oxide and to limit short circuit current. The actual gate oxide breakdown voltage is significantly higher than this, but staying within this rating at all times ensures application reliability.

V_{GEM} – Gate Emitter Voltage Transient

V_{GEM} is the maximum pulsed voltage between the gate and emitter terminals. The purpose of this rating is to prevent breakdown of the gate oxide.

Transients on the gate can be induced not only by the applied gate drive signal but often more significantly by stray inductance in the gate drive circuit as well as feedback through the gate-collector capacitance. If there is more ringing on the gate than V_{GEM}, stray circuit inductances probably need to be reduced, and/or the gate resistance should be increased to slow down the switching speed. In addition to the power circuit layout, gate drive circuit layout is critical in minimizing the effective gate drive loop area and resulting stray inductances. See Figure 9.

If a clamping zener is used, it is recommended to connect it between the gate driver and the gate resistor rather than directly to the gate terminal. Negative gate drive is not necessary but may be used to achieve the utmost in switching speed while avoiding dv/dt induced turn-on. See application note APT9302 for more information on gate drive design.

I_{C1}, I_{C2} – Continuous Collector Current

I_{C1} and I_{C2} are ratings of the maximum continuous DC current with the die at its maximum rated junction temperature. They are based on the junction to case thermal resistance rating $R_{\theta JC}$ and the case temperature as follows:

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} = V_{CE(on)} \cdot I_C \quad (1)$$

This equation simply says that the maximum heat that can be dissipated, $\frac{T_{J(max)} - T_C}{R_{\theta JC}}$, equals the maximum allowable heat generated by conduction loss, $V_{CE(on)} \cdot I_C$. There are no switching losses involved in I_{C1} and I_{C2}. Solving for I_C:

$$I_C = \frac{T_{J(max)} - T_C}{R_{\theta JC} \cdot V_{CE(on)}} \quad (2)$$

Of course $V_{CE(on)}$ depends upon I_C (as well as junction temperature). Except at relatively low current, the relationship between I_C and $V_{CE(on)}$ is fairly linear, as shown in Figure 5. Thus a linear approximation can be used to relate I_C to $V_{CE(on)}$.

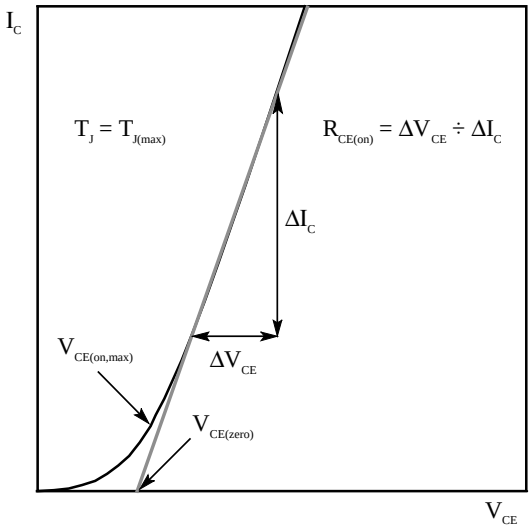

Figure 5 Linear Approximation of I_C versus $V_{CE(on)}$

The curve of $V_{CE(on)}$ is with the die at elevated temperature. (To calculate datasheet values, APT uses the maximum $V_{CE(on)}$, which is higher than the typical $V_{CE(on)}$ to account for normal variations between parts.) The equation relating $V_{CE(on)}$ to I_C is:

$$V_{CE(on)} = I_C \cdot R_{CE(on)} + V_{CE(zero)} \quad (3)$$

This equation is substituted into (2) for $V_{CE(on)}$ to solve for I_C:

$$I_C = \frac{T_{J(max)} - T_C}{R_{\theta JC} \cdot V_{CE(on)}} = \frac{T_{J(max)} - T_C}{R_{\theta JC}\left(I_C \cdot R_{CE(on)} + V_{CE(zero)}\right)} \Rightarrow$$

$$I_C{}^2 \cdot R_{CE(on)} + I_C \cdot V_{CE(zero)} = \frac{T_{J(max)} - T_C}{R_{\theta JC}} \qquad (4)$$

This is in the form of the familiar quadratic equation $x = \frac{-b \pm \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a}$ with

$a = R_{CE(on)}$, $b = V_{CE(zero)}$, and $c = \frac{-\left(T_{J(max)} - T_C\right)}{R_{\theta JC}}$. The solution is:

$$I_C = \frac{-V_{CE(zero)} + \sqrt{V_{CE(zero)}{}^2 + 4 \cdot R_{CE(on)} \cdot \left(\frac{T_{J(max)} - T_C}{R_{\theta JC}}\right)}}{2 \cdot R_{CE(on)}} \qquad (5)$$

I_C in (5) represents the continuous DC current (with the device fully on) that causes the die to heat up to its maximum rated junction temperature. I_{C1} is the solution to (5) with T_C equal to 25 ºC. I_{C2} is the solution to (5) with T_C at an elevated temperature. This is a more useful rating than the traditional I_{C1} rating since operating at a case temperature of only 25 ºC is seldom feasible, however I_{C2} still does not take switching losses into account.

Graph of I_C versus T_C

To assist designers in the selection of devices for a particular application, APT provides a graph of maximum collector current versus case temperature. This graph is simply the solution to (5) over a range of case temperatures. Figure 6 shows an example. Note that in this case, the package leads limit the current to 100 Amps at low temperature, not the die.

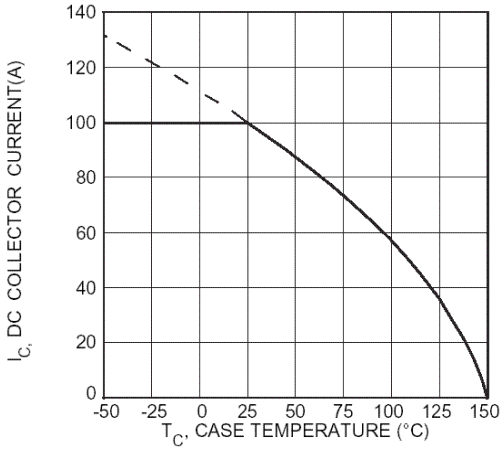

Figure 6 Maximum Collector Current versus Case Temperature

Using the I_{C1} and I_{C2} Ratings

The I_{C1} and I_{C2} ratings and the graph of maximum collector current versus case temperature simply indicate the *maximum theoretical continuous DC current* that the device can carry, based on the maximum junction to case thermal resistance. Their purpose is mainly as figures of merit for comparing devices. For a soft switching application, I_{C2} is a good starting point for selecting a device. In a hard or soft switching application, the device might safely carry more or less current depending upon:

- switching losses
- duty cycle
- switching frequency
- switching speed
- heat sinking capacity
- thermal impedances and transients

The point is that you cannot simply assume that the device can safely carry the same current in a switch-mode power converter as is indicated in the I_{C1} or I_{C2} ratings or in the graph of maximum collector current versus case temperature. APT offers application support if you require assistance with selecting devices or modules that are appropriate for your application.

I_{CM} – Pulsed Collector Current

This rating indicates how much pulsed current the device can handle, which is significantly higher than the rated continuous DC current. The purposes of the I_{CM} rating are:

- To keep the IGBT operating in the "linear" region of its transfer characteristic. See Figure 7. There is a maximum collector current for a corresponding gate-emitter voltage that an IGBT will conduct. If the operating point at a given gate-emitter voltage goes above the linear region "knee" in Figure 7, any further increase in collector current results in a significant rise in collector-emitter voltage and consequent rise in conduction loss and possible device destruction. The I_{CM} rating is set below the "knee" for typical gate drive voltages.
- To prevent burnout or latchup. Even if the pulse width is theoretically too short to overheat the die, significantly exceeding the I_{CM} rating can cause enough localized die feature heating to result in a burnout site or latchup.
- To prevent overheating the die. The footnote "*Repetitive rating: Pulse width limited by maximum junction temperature*" implies that I_{CM} is based on a thermal limitation depending on pulse width. This is always true for two reasons: 1) there is some margin in the I_{CM} rating before risk

of damage other than by the die exceeding its maximum junction temperature, and 2) no matter what the failure mechanism really is, overheating is almost always the observed end result anyway.

- To avoid problems with excessive current through the bond wires, although there would probably first be problems related to excessive current through the die.

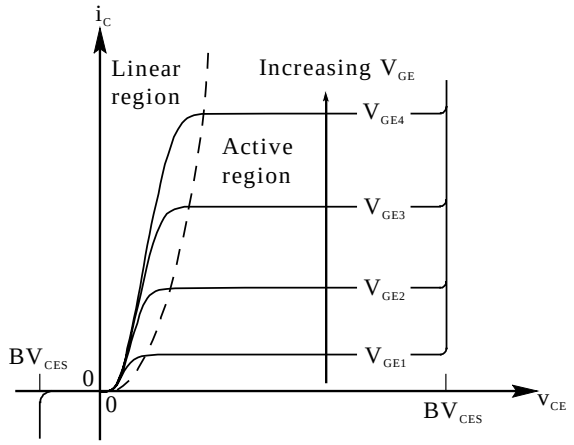

Figure 7 IGBT Transfer Characteristic

Regarding the thermal limitation on I_{CM}, temperature rise depends upon the pulse width, time between pulses, heat dissipation, and $V_{CE(on)}$ as well as the shape and magnitude of the current pulse. Simply staying within the I_{CM} limit does not ensure that the maximum junction temperature will not be exceeded. See the discussion of the Maximum Effective Transient Thermal Impedance curve for a procedure to estimate junction temperature during a current pulse.

I_{LM}, RBSOA, and SSOA – Safe Operating Areas

These ratings are all related. I_{LM} is the amount of clamped inductive load current the device can safely switch in a snubberless hard switching application. Test circuit conditions are specified (case temperature, gate resistance, clamp voltage, etc.) The I_{LM} rating is limited by the turn-off transient, where the gate was positive-biased and switches to zero or negative bias. Hence the I_{LM} rating and the Reverse Bias Safe Operating Area (RBSOA) are similar. The I_{LM} rating is a maximum current, RBSOA is a maximum current at a specified voltage.

Switching safe operating area (SSOA) is simply RBSOA at the full V_{CES} voltage rating. Forward bias safe operating area (FBSOA), which covers the turn-on transient, is typically much higher than the RBSOA and is therefore typically not listed in the datasheet.

The circuit designer does not need to worry about snubbers, minimum gate resistance, or limits on dv/dt as long as these ratings are not exceeded.

E_{AS} – Single Pulse Avalanche Energy

All devices that are avalanche energy rated have an E_{AS} rating. Avalanche energy rated is synonymous with unclamped inductive switching (UIS) rated. E_{AS} is both thermally limited and defect limited and indicates how much reverse avalanche energy the device can safely absorb with the case at 25 ºC and the die at or below the maximum rated junction temperature. The open cell structure used in Power MOS 7® mitigates the defect limitation on E_{AS}. On the other hand, a defect in a closed cell structure can cause the cell to latchup under avalanche condition. Do not operate an IGBT intentionally in avalanche condition without thorough testing.

Conditions for a test circuit are stated in a footnote, and the E_{AS} rating is equal to $\frac{L \cdot i_C^2}{2}$ where L is the value of an inductor carrying a peak current i_C, which is suddenly diverted into the collector of the device under test. It is the inductor's voltage, which exceeds the breakdown voltage of the IGBT, that causes the avalanche condition. An avalanche condition allows the inductor current to flow through the IGBT, even though the IGBT is in the off state. Energy stored in the inductor is analogous to energy stored in leakage and/or stray inductances and is dissipated in the device under test. In an application, if ringing due to leakage and stray inductances does not exceed the breakdown voltage, then the device will not avalanche and hence does not need to dissipate avalanche energy. Avalanche energy rated devices offer a safety net depending on the margin between the voltage rating of the device and system voltages, including transients.

P_D – Total Power Dissipation

This is a rating of the maximum power that the device can dissipate and is based on the maximum junction temperature and the thermal resistance $R_{\theta JC}$ at a case temperature of 25 ºC.

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} \quad (6)$$

At case temperatures above 25 ºC, the linear derating factor is simply the inverse of $R_{\theta JC}$.

T_J,T_{STG} – Operating and Storage Junction Temperature Range

This is the range of permissible storage and operating junction temperatures. The limits of this range are set to ensure a minimum acceptable device service life. Operating away from the limits of this range can significantly enhance the service life. It's actually an exponential function relating device life to junction temperature, but as a "rule of thumb", for thermally induced effects only, every 10 ºC reduction in junction temperature doubles the device life.

Static Electrical Characteristics

BV_{CES} – Collector-Emitter Breakdown Voltage

Measuring the actual collector-emitter breakdown voltage is practically impossible without destroying the device. Therefore, BV_{CES} is the collector-emitter voltage at which no more than the specified collector current will flow at the specified temperature. This tracks the actual breakdown voltage.

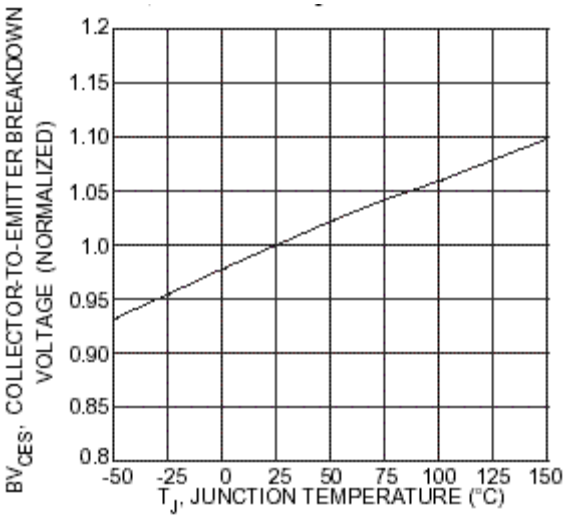

Figure 8 Normalized Breakdown Voltage vs. Junction Temperature

As shown in Figure 8, BV_{CES} has a positive temperature coefficient. At a fixed leakage current, an IGBT can block more voltage when hot than when cold. In fact, when cold, the BV_{CES} specification is less than the V_{CES} rating. For the example shown in Figure 8, at -50 ºC, BV_{CES} is about 93% of the nominal 25 ºC specification.

RBV_{CES} – Reverse Collector-Emitter Breakdown Voltage

This is the reverse collector-emitter breakdown voltage specification, i.e., when the emitter voltage is positive with respect to the collector. As with BV_{CES}, RBV_{CES} is the emitter-collector voltage at which no more than the specified emitter current will flow at the specified temperature. A typical value is about 15 Volts, however RBV_{CES} is often not specified since an IGBT is not designed for reverse voltage blocking. Even though in theory an NPT IGBT can block as much reverse voltage as forward voltage, in general it cannot due to the manufacturing process. A PT IGBT cannot block very much reverse voltage due to the n+ buffer layer.

$V_{GE(th)}$ – Gate Threshold Voltage

This is the gate-source voltage at which collector current begins to flow. Test conditions (collector current, collector-emitter voltage, junction temperature) are also specified. All MOS gated devices exhibit variation in $V_{GE(th)}$ between devices, which is normal. Therefore, a range of $V_{GE(th)}$ is specified, with the minimum and maximum representing the edges of the $V_{GE(th)}$ distribution. $V_{GE(th)}$ has a negative temperature coefficient, meaning that as the die heats up, the IGBT will turn on at a lower gate-emitter voltage. This temperature coefficient is typically about minus 12mV/ºC, the same as for a power MOSFET.

$V_{CE(on)}$ – Collector-Emitter On Voltage

This is the collector-emitter voltage across the IGBT at a specified collector current, gate-emitter voltage, and junction temperature. Since $V_{CE(on)}$ is temperature dependent, it is specified both at room temperature and hot.

Graphs are provided that show the relationships between typical (not maximum) collector-emitter voltage and collector current, temperature, and gate-emitter voltage. From these graphs, a circuit designer can estimate conduction loss and the temperature coefficient of $V_{CE(on)}$. Conduction power loss is $V_{CE(on)}$ times collector current. The temperature coefficient is the slope of $V_{CE(on)}$ versus temperature. NPT IGBTs have a positive temperature coefficient, meaning that as the junction temperature increases, $V_{CE(on)}$ increases. PT IGBTs on the other hand tend to have a slightly negative temperature coefficient. For both types, the temperature coefficient tends to increase with increasing collector current. As current increases, the temperature coefficient of a PT IGBT can actually transition from negative to positive.

I_{CES} – Collector Cutoff Current

This is the leakage current that flows from collector to emitter when the device is off, at a specified collector-emitter and gate-emitter voltage. Since leakage current increases with temperature, I_{CES} is specified both at room temperature and hot. Leakage power loss is I_{CES} times collector-emitter voltage.

I_{GES} – Gate-Emitter Leakage Current

This is the leakage current that flows through the gate terminal at a specified gate-emitter voltage.

Dynamic Characteristics

Figure 9 shows an equivalent IBGT model that includes the capacitances between the terminals. Input, output, and reverse transfer capacitances are combinations of these capacitances. See application note APT0103 for more details. Test conditions to measure capacitances are specified in the datasheet.

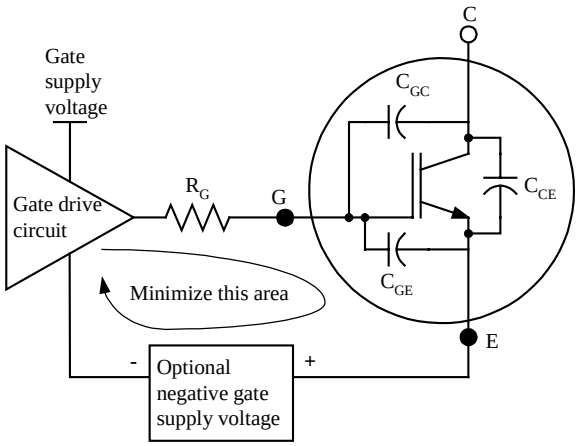

Figure 9 IGBT Capacitances

C_{ies} – Input Capacitance

This is the input capacitance measured between the gate and emitter terminals with the collector shorted to the emitter for AC signals. C_{ies} is made up of the gate to collector capacitance (C_{GC}) in parallel with the gate to emitter capacitance (C_{GE}), or

$$C_{ies} = C_{GE} + C_{GC}$$

The input capacitance must be charged to the threshold voltage before the device begins to turn on, and discharged to the plateau voltage before the device begins to turn off. Therefore, the impedance of the drive circuitry and C_{ies} have a direct relationship to the turn on and turn off delays.

C_{oes} – Output Capacitance

This is the output capacitance measured between the collector and emitter terminals with the gate shorted to the emitter for AC voltages. C_{oes} is made up of the collector to emitter capacitance (C_{CE}) in parallel with the gate to collector capacitance (C_{GC}), or

$$C_{oes} = C_{CE} + C_{GC}$$

For soft switching applications, C_{oes} is important because it can affect the resonance of the circuit.

C_{res} – Reverse Transfer Capacitance

This is the reverse transfer capacitance measured between the collector and gate terminals with the emitter connected to ground. The reverse transfer capacitance is equal to the gate to collector capacitance.

$$C_{res} = C_{GC}$$

The reverse transfer capacitance, often referred to as the Miller capacitance, is one of the major parameters affecting voltage rise and fall times during switching.

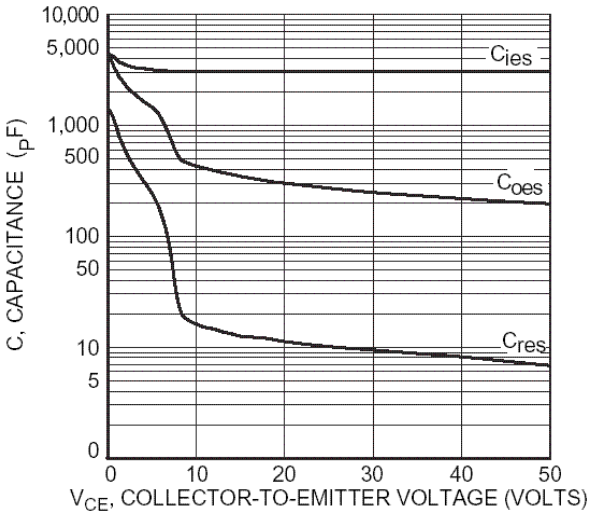

Figure 10 Capacitance vs. Collector-Emitter Voltage

Figure 10 shows an example graph of typical capacitance values versus collector-emitter voltage. The capacitances decrease over a range of increasing collector-emitter voltage, especially the output and reverse transfer capacitances. This variation is the 'raison d'être' for gate charge data, as will be explained.

V_{GEP} – Plateau Voltage

Figure 11 shows the gate-emitter voltage as a function of gate charge. The turn-on sequence traverses this curve from left to right, turn-off traverses from right to left. The method for measuring gate charge is described in JEDEC standard 24-2. The gate plateau voltage V_{GEP} is defined as the gate-emitter voltage when the slope of the gate-emitter voltage first reaches a minimum during the turn-on switching transition for a constant gate current drive condition. In other words, it is the gate-emitter voltage where the gate charge curve first straightens out after the first inflection in the curve, as shown in Figure 11. Alternatively, V_{GEP} is the gate-emitter voltage at the last minimum slope during turn-off.

The plateau voltage increases with current but not with temperature. Beware when replacing power MOSFETs with IGBTs. A 10 or 12 Volt gate drive might work fine for a high voltage power MOSFET, but depending upon its plateau voltage, an IGBT at high current might switch surprisingly slowly or not even completely turn on unless the gate drive voltage is increased.

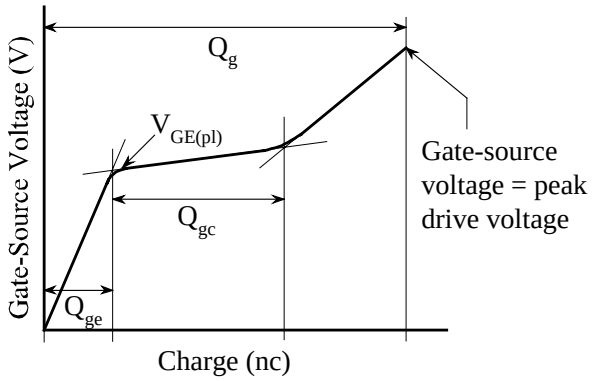

Figure 11 v_{GE} as a Function of Gate Charge

Q_{ge}, Q_{gc}, and Q_g – Gate Charge

Referring to Figure 11, Q_{ge} is the charge from the origin to the first inflection in the curve, Q_{gc} is the charge from the first to second inflection in the curve (also known as the "Miller" charge), and Q_g is the charge from the origin to the point on the curve at which v_{GE} equals the peak drive voltage.

Gate charge values vary with collector current and collector-emitter voltage but not with temperature. Test conditions are specified. In addition, a graph of gate charge is typically included in the datasheet showing gate charge curves for a fixed collector current and different collector-emitter voltages. The gate charge values reflect charge stored on the inter-terminal capacitances described earlier. Gate charge is often used for designing gate drive circuitry since it takes into account the changes in capacitance with changes in voltage during a switching transient. Refer to application note APT0103 for more information on gate charge.

Switching Times and Energies

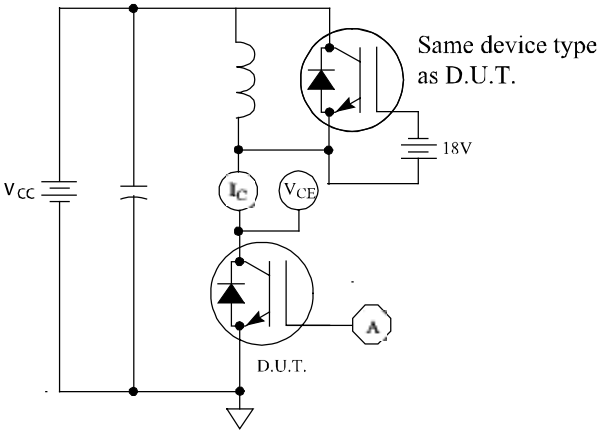

Figure 12 Inductive Switching Loss Test Circuit

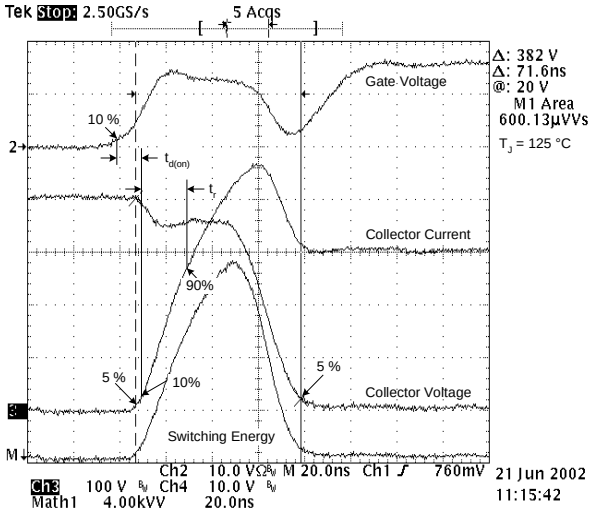

Figure 13 Turn-on Waveforms and Definitions

Switching times and energies are not always easy to predict for IGBTs, so APT provides switching times and energies in the datasheet for hard-switched clamped inductive switching. Test circuits and definitions are included in each datasheet. Figure 12 shows a test circuit used to measure switching times and energies and Figure 13 shows the associated waveforms and definitions. The following test conditions are specified in the Dynamic Characteristics table: V_{CC} in Figure 12, inductor current, gate drive voltage, gate resistance, and junction temperature. Note that gate resistance includes the resistance of the gate driver IC. Since switching times and energies

vary with temperature (except E_{on1}), data is provided both at room temperature and hot. Graphs are also often provided showing the relationships between switching times and energies to collector current, junction temperature, and gate resistance.

In general, turn-on speed and energy are relatively independent of temperature, or actually increasing in speed (decreasing in energy) very slightly with increasing temperature. Diode reverse recovery current increases with temperature, resulting in the increase in E_{on2} with temperature. E_{on1} and E_{on2} are defined below. Turn-off speed decreases with increasing temperature, corresponding to an increase in turn-off energy. Switching speed, both turn-on and turn-off, decreases with increasing gate resistance, corresponding to an increase in switching energies. Switching energy can be scaled directly for variation between application voltage and the datasheet switching energy test voltage. So if the datasheet tests were done at 400 Volts for example, and the application is at 300 Volts, simply multiply the datasheet switching energy values by the ratio 300/400 to extrapolate.

Switching times and energies also vary strongly with stray inductances in the circuit, including the gate drive circuit. In particular, stray inductance in series with the emitter significantly affects switching times and energies. Therefore, switching time and energy values and graphs in the datasheet are representative only and may vary from observed results in an actual power supply or motor drive circuit.

$t_{d(on)}$, – Turn-on Delay Time

Turn-on delay time is the time from when the gate-emitter voltage rises past 10% of the drive voltage to when the collector current rises past 10% of the specified inductor current. See Figure 13.

$t_{d(off)}$, – Turn-off Delay Time

Turn-off delay time is the time from when the gate-emitter voltage drops below 90% of the drive voltage to when the collector current drops below 90% of the specified inductor current. This gives an indication of the delay before current begins to transition in the load. See Figure 14.

t_r – Current Rise Time

Current rise time is the time between the collector current rising from 10% to 90% start to stop of the specified inductor current. See Figure 13.

t_f – Current Fall Time

Current fall time is the time between the collector current dropping from 90% to 10% start to stop of the specified inductor current. See Figure 14.

E_{on2} – Turn-on Switching Energy with Diode

This is the clamped inductive turn-on energy that includes a commutating diode reverse recovery current in the IGBT turn-on switching loss. A Combi device (IGBT combined with anti-parallel diode) with the same type IGBT as the DUT is used for the clamping diode as shown in the test circuit in Figure 12.

Turn-on switching energy is the integral of the product of collector current and collector-emitter voltage over the interval from when the collector current rises past 5% of the test current to when the voltage falls below 5% of the test voltage. The 5% of current rise and voltage fall definitions for the integration interval in the waveforms in Figure 13 accommodate the resolution of the instrumentation while providing a reliable means of duplicating the measurement that does not compromise accuracy.

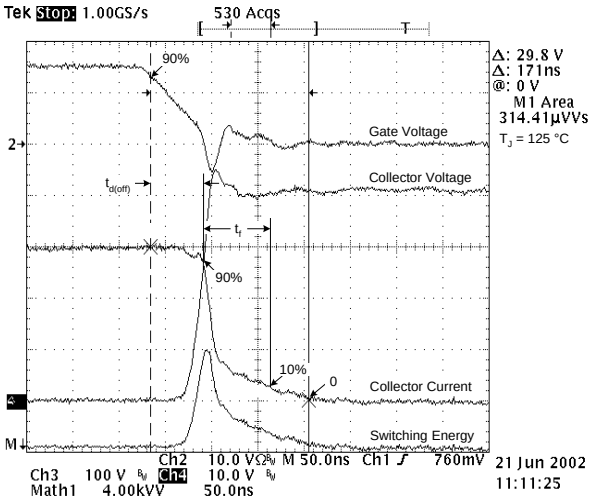

Figure 14 Turn-off Waveforms and Definitions

E_{off} – Turn-off Switching Energy

This is the clamped inductive turn-off energy. Figure 12 shows the test circuit and Figure 14 shows the waveforms and definitions. E_{off} is the integral of the product of collector current and collector-emitter voltage over the interval starting from when the gate-emitter voltage drops below 90% to when the collector current reaches zero. This is in accordance with JEDEC standard 24-1 for measuring turn-off energy. Older datasheets show E_{off} measured from the beginning of the switching transient and going on for 2 µs. The method used for each device is shown in its datasheet.

E_{on1} – Turn-on Switching Energy

This is the clamped inductive turn-on energy of the IGBT only, without the effect of a commutating diode reverse recovery current adding to the IGBT turn-on loss. Figure 15 shows a test circuit. The definition for the integration interval of E_{on1} is the same as for E_{on2} in Figure 13.

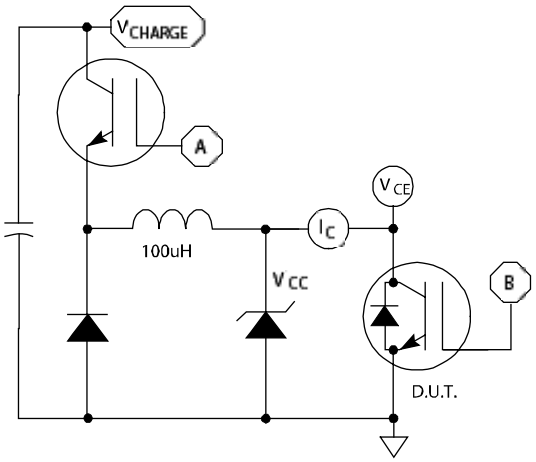

Figure 15 E_{on1} Test Circuit

g_{fe} – Forward Transconductance

Forward transconductance relates collector current to gate-emitter voltage. Forward transconductance varies with collector current, collector-emitter voltage, and temperature. High transconductance corresponds to low plateau voltage and fast current rise and fall times. Transconductance is important for bipolar transistors. IGBTs on the other hand are thermally limited long before the transconductance drops off, so this specification is not all that useful.

It is important to note however that IGBTs exhibit relatively high gain even at high gate-emitter voltage. This is because increasing the flow of electrons by increasing the gate-emitter voltage also increases the flow of holes. The gain of a high voltage power MOSFET however is very insensitive to gate voltage once fully on.

Thermal & Mechanical Characteristics

$R_{\theta JC}$ – Junction to Case Thermal Resistance

This is the thermal resistance from the junction of the die to the outside of the device case. Heat is the result of power lost in the device itself, and thermal resistance relates how hot the die gets based on this power loss. It is called thermal resistance because an electrical model is used to predict temperature rise based on steady state power loss as shown in Figure 16.

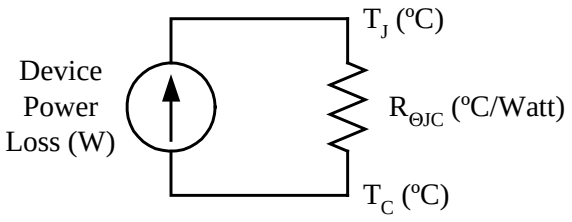

Figure 16 Thermal Resistance Model

Power loss, modeled as current, flowing through a thermal resistance, modeled as a resistor, creates a temperature rise, which is modeled as a voltage rise. Additional resistors could be added in series to model case-to-sink and sink-to-ambient thermal resistances. The temperature at various physical locations is analogous to the voltage at nodes in the thermal resistance circuit model. Thus, on a steady-state basis, junction temperature can be calculated as

$$T_J = T_C + P_{Loss} \cdot R_{\theta JC} \qquad (7)$$

Device power loss is the sum of averaged switching, conduction, and leakage losses. Typically, leakage losses can be ignored. Since case-to-sink and sink-to-ambient thermal resistances depend entirely upon the application (thermal compounds, heat sink type, etc.), only $R_{\theta JC}$ is specified in the datasheet. Sometimes $R_{\theta JA}$ is also specified even though typical applications always require heat sinking.

Ratings such as maximum continuous DC current, total power dissipation, and frequency versus current are based on a maximum $R_{\theta JC}$ value. The maximum $R_{\theta JC}$ value is used because it incorporates margin to account for normal manufacturing variations and provide some application margin as well. The industry trend is toward decreasing the margin between the maximum $R_{\theta JC}$ value and the typical value, which is usually not published.

$Z_{\theta JC}$ – Junction to Case Thermal Impedance

Thermal impedance is the dynamic cousin of thermal resistance. Thermal impedance takes into account the heat capacity of the device, so it can be used to estimate instantaneous temperatures resulting from power loss on a transient basis.

Transient thermal impedance is determined by applying power pulses to the device of various magnitudes and durations. The result is the transient

impedance 'family of curves', an example of which is shown in Figure 17. Note that the family of curves is based on the maximum $R_{\theta JC}$ value, which incorporates margin as discussed previously. The method of calculating peak junction temperature is shown in Figure 17. For non-rectangular power pulses, a piecewise linear approximation must be used.

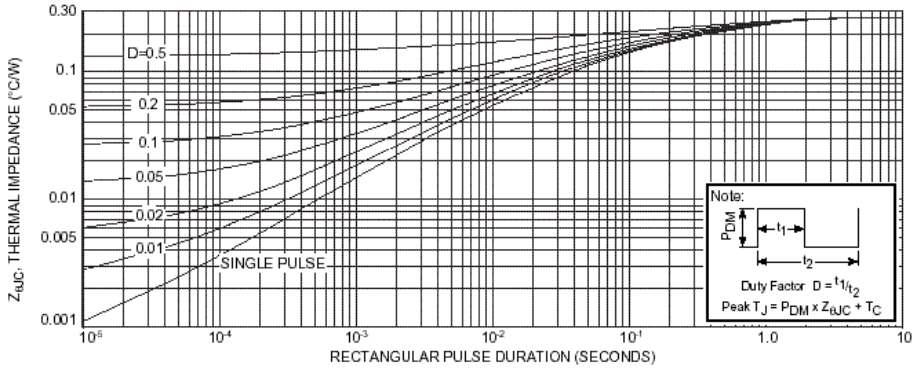

Figure 17 Thermal Impedance 'Family of Curves'

Usable Frequency versus Current

The usable frequency versus current curve is one of the more useful items in the datasheet. Even though it is limited to certain conditions specified in the datasheet (inductive hard switching, 50% duty, fixed case and junction temperatures, fixed test current, voltage, and gate resistance), it provides a realistic indication of how the device will perform in an application. The trend in the industry will likely be toward using usable frequency versus current as a figure of merit for comparing devices rather than relying so much on I_{C1} and I_{C2} ratings.

In an inductive hard switching application, switching frequency is limited by minimum and maximum pulse widths as well as conduction and switching losses. The pulse width limitation is due to transient thermal response in the die. Back-to-back switching transients do not allow the die time to cool between the large hard switching power loss spikes. Also, repetitively not allowing the switching transient to complete before switching the other way can overheat the die. Depending upon operating temperatures and transient thermal impedance, the die junction may become overheated, even if the duty cycle is very small.

The minimum duty cycle limitation is a challenge for motor drives, such as in an electric vehicle, where at very low power, an exceptionally small duty cycle is required unless the switching frequency is dropped into the audible range or some type of pulse skipping scheme is implemented.

To arrive at a frequency limit based on minimum pulse width, APT defines the minimum limit on pulse width such that the total switching time (sum of turn-on and turn-off switching times) must be no more than 5% of the switching period. This is a reasonable limitation in most cases that can be verified by transient thermal analysis. The question is: what is the total switching time? It can be estimated by adding the turn-on and turn-off current delay times and current rise and fall times. Examination of the switching waveforms in Figures 13 and 14 reveals that this gives a good approximation of total switching time. Only the voltage fall time during turn-on is not accounted for, but this is relatively short. The 5% of switching period limitation on total switching time provides plenty of margin for this approximation anyway. So the maximum frequency based on minimum pulse width is

$$f_{max1} = \frac{1}{T_s} = \frac{0.05}{t_{d(on)} + t_{d(off)} + t_r + t_f} \tag{8}$$

The thermal limit to frequency is derived as follows:

$$P_{diss} = \frac{T_J - T_C}{R_{\theta JC}} = P_{cond} + \frac{E_{on2} + E_{off}}{t_{diss}} \tag{9}$$

P_{cond} is the conduction power loss (collector current times $V_{CE(on)}$, at that collector current, times duty cycle) and t_{diss} is the minimum time during which E_{on2} and E_{off} can be dissipated to maintain the specified junction temperature. Since the conduction loss is based on a fixed 50% duty cycle assumption, it is independent of frequency. However, the higher the conduction loss, the more time is required to dissipate the switching losses. So the inverse of t_{diss} is the maximum frequency that we're after.

$$f_{max2} = \frac{1}{t_{diss}} = \frac{\frac{T_J - T_C}{R_{\theta JC}} - P_{cond}}{E_{on2} + E_{off}} \tag{10}$$

Finally, the maximum switching frequency at a given collector current is simply the minimum of f_{max1} and f_{max2}. Frequency is typically limited thermally except at very low current.

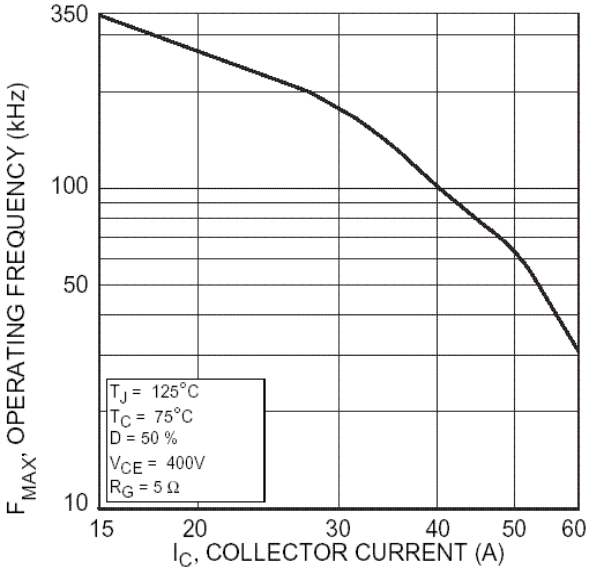

Figure 18 Maximum Frequency Versus Current

Figure 18 shows an example curve of frequency versus current for a 600 Volt PT IGBT. It should be noted again that this curve is for inductive hard switching at one particular set of conditions for both the Device Under Test (DUT) and the clamping diode.

Datasheet Extrapolation Example

Suppose in a switch mode power supply application we want to hard switch 20 Amps at 200 kHz at 300 Volts and 35% duty cycle. The gate drive voltage is 15 Volts, and the gate drive resistor is 15 Ohms. Also, suppose we only want to let the junction reach 112 ºC but can still maintain the case at 75 ºC. With a 600 Volt device, there is a 300 Volt margin between the application voltage and V_{CES}, so avalanche capability would not be required. Short circuit capability is also not required. It is a bridge configuration, so a Combi with integral anti-parallel diode is required. Which device will work?

Since this is a relatively high frequency application that does not require a very rugged device, the Power MOS 7® series would be the best choice.

It looks like the device for which the usable frequency versus current graph in Figure 18 was created might work. However, the application conditions don't match the datasheet test conditions. We can extrapolate the datasheet results to see if it will fit the application.

Since the frequency is most likely to be thermally limited, we'll start by computing f_{max2}. From the output characteristics graph shown in Figure 19, we can look up $V_{CE(on)}$ at 125 ºC, which will be about the same as at 112 ºC.

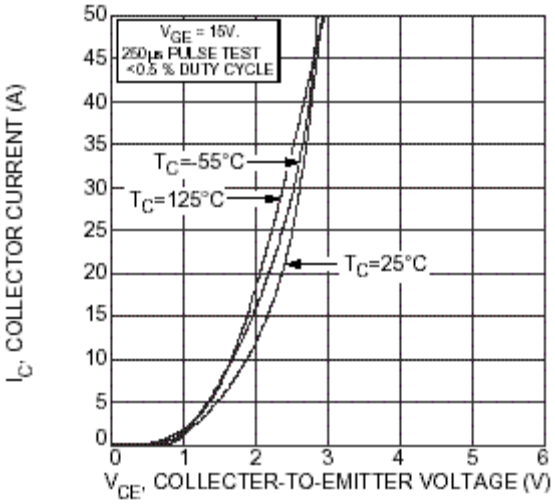

Figure 19 Collector Current vs. Collector-Emitter Voltage

At 20 Amps and 125 ºC, $V_{CE(on)}$ is about 2.1 Volts. So the conduction loss at 20 Amps is about $2.1 \cdot 20 \cdot 0.35 = 14.7$ Watts. The total power that can be dissipated is $\frac{T_J - T_C}{R_{\theta JC}} = \frac{112-75}{0.27} = 137$ Watts. Now we need E_{on2} and E_{off} at 112 ºC and 15 Ohms gate resistance. We can get this from the switching energy versus gate resistance graph, shown in Figure 20.

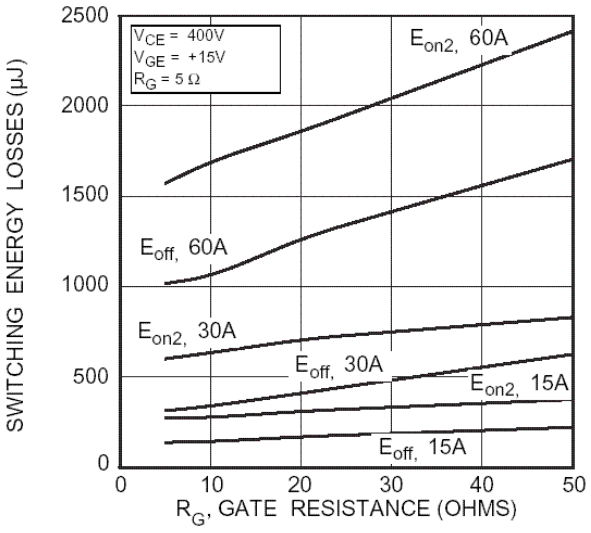

Figure 20 Switching Energy vs. Gate Resistance

At 125 ºC, 20 Amps, and 15 Ohms, E_{on2} is somewhere between the 15 Amp and 30 Amp E_{on2} values of 300 and 700 µJ. Call it 500 µJ. E_{off} will be around 270 µJ. At 112 ºC, these values will be slightly less than this.

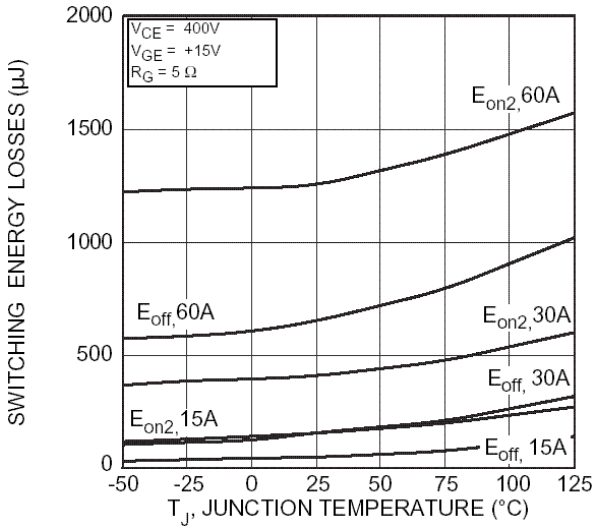

Figure 21 Switching Energy vs. Temperature

By inspection of Figure 21, we can see that E_{on2} and E_{off} at 112 ºC are about 80% of their values at 125 ºC. So E_{on2} and E_{off} will be about 400 and 216 µJ respectively. Finally, we must adjust for the difference in voltage. The datasheet test voltage is 400 Volts, the application voltage is only 300 Volts. So we simply scale E_{on2} and E_{off} accordingly.

$$E_{on2} = \frac{300}{400} \cdot 400\mu J = 300\mu J \text{ and}$$

$$E_{off} = \frac{300}{400} \cdot 216\mu J = 162\mu J.$$

Now we can calculate f_{max2}:

$$f_{max2} = \frac{137 - 14.7}{(300 + 162) \cdot 10^{-6}} = 264718\,Hz$$

Since this is above our target of 200 kHz, so far it seems that this device could work.

It is not really necessary to extrapolate what f_{max1} would be for the application conditions versus the datasheet test conditions. The graphs of delay times and current rise and fall times can be used instead to get an indication of how fast the device will switch. Also, the f_{max1} limit only comes into play at relatively low current. In fact, for some devices, maximum frequency is always thermally limited (f_{max2} is always less than f_{max1}).

It is important to note that datasheet graphs present typical data. There is some normal variation between parts and certainly between test circuits. In this extrapolation example, there is about a 32% margin, at least in terms of operating frequency. What really matters though is how the device performs in the application, and the results indicate that this device would certainly be worthwhile to test. If more design margin is required, then it would be a good idea to test the next larger device as well. So the next step would be to call the APT sales representative to get some devices for testing.