# AKD4616-A

## AK4616 Evaluation Board Rev.3

## GENERAL DESCRIPTION

The AKD4616-A is an evaluation board for AK4616, which is a 24bit CODEC including 3ch ADC, 5ch DAC and microphone amplifier. The control settings of this board may be controlled via USB port, allowing for easy A/D and D/A evaluation. RCA connectors are used for the input and output of the analog signals. This board also has a digital interface which can be connected to the digital audio system via optical connector.

### ■ Ordering guide

AKD4616-A --- Evaluation board for AK4616
Control software included in package

## FUNCTION

- ☐ **Clock generate circuits (AK4118A used)**
- ☐ **Compatible with 2 types of digital audio interface**
  - **Optical input (x1) / Optical output (x1)**
  - **10pin header for interface with external data source**
- ☐ **RCA connector for external clock input**
- ☐ **ADC 3ch input, DAC 5ch output**
- ☐ **USB port and 10pin header for board control**

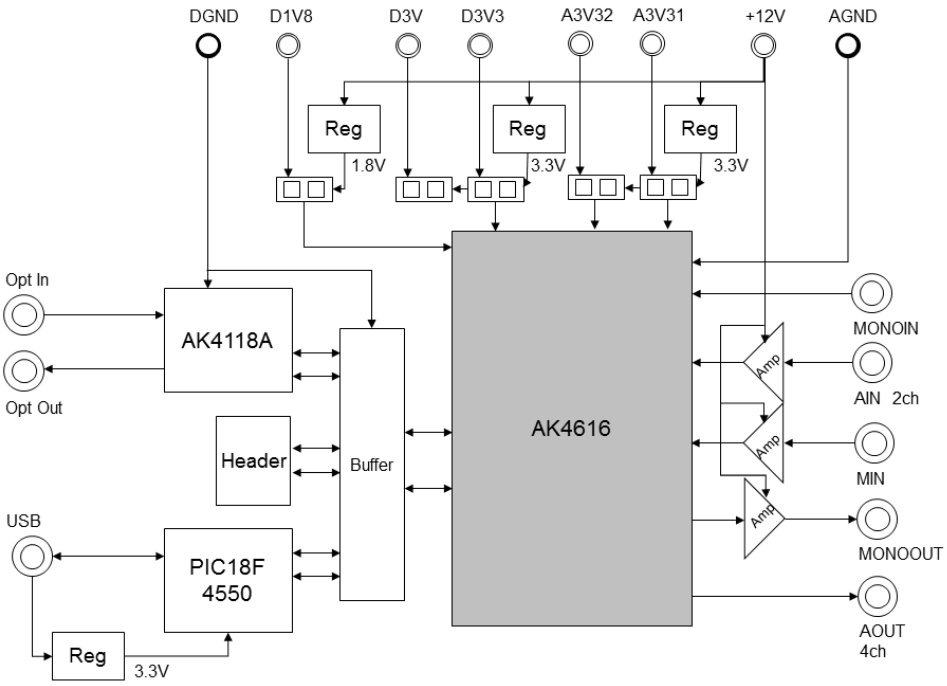



Figure 1. AKD4616-A Block Diagram

## Evaluation Board Diagram

### ■ Board Diagram

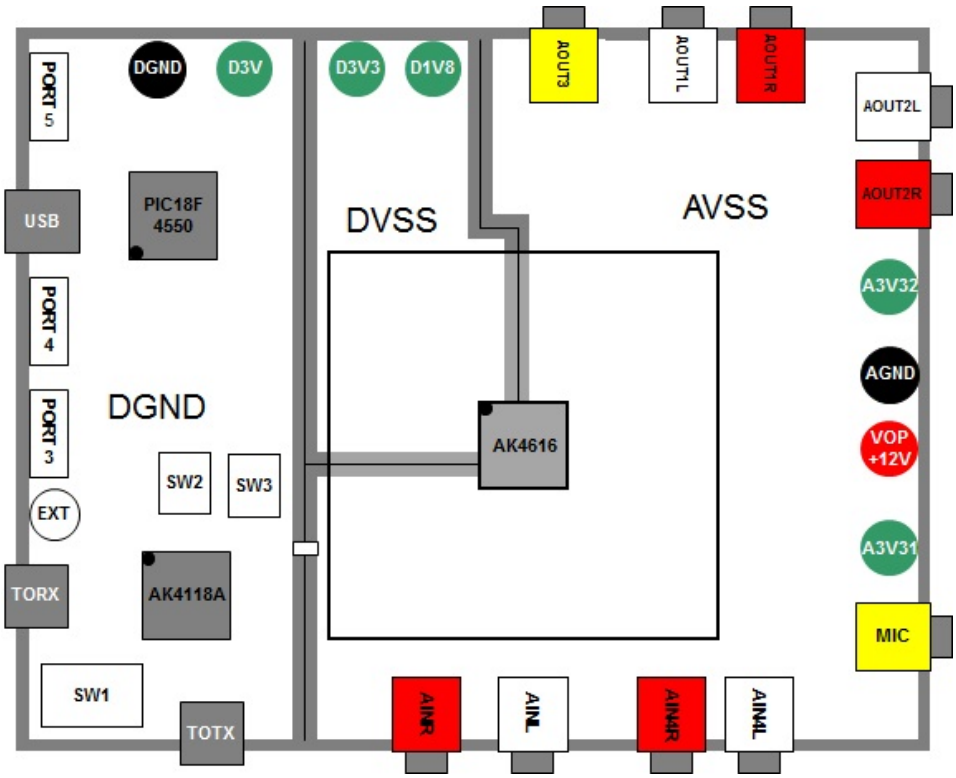



Figure 2. AKD4616-A Board Diagram

### ■ Description

(1) AINL/R; AIN4L/R; MIC; AOUT1L/R; AOUT2L/R; AOUT3 (RCA Jack)
AINL/R: Analog input jacks for AIN1-3. AIN4L/R: Analog input jacks for AIN4.
MIC: Analog input jack for Microphone (Single-end and Differential).
AOUT1-2L/R: Analog output jacks for AOUT1-2L/R. AOUT3: Analog output jack for AOUT3.
White jacks are used for left channel and red ones are for right channel.

(2) AK4118A
AK4118A has DIR, DIT and X'tal oscillator. Transports input data to AK4616 when working in master mode, and output data from AK4616 when working in slave mode.

(3) TOTX/TORX (Optical Connector)
TORX PORT1: Output optical signal from AK4118A
TOTX PORT2: Input optical signal to AK4118A.

(4) VOP +12V/AGNDn/DGNDn (Power supply)
Connect to +12V and GND according to the following operation sequence.

(5) PIC18F4550
USB control chip. Sets up AK4616 registers from PC via USB port.

(6) SW1
DIP type switch. Sets clock and audio format of AK4118A. DIF[2:0] used to set audio interface format and OCKS[1:0] used to master clock frequency. Please refer to Table 3. SW1 Setting, Table 4. Audio format, Table 5. Master Clock Frequency Select for details.

(7) SW2
Toggle type switch. Power-down switch for AK4616. Reset board by bringing down SW2 once upon power-up.

(8) SW3
Toggle type switch. Power-down switch for AK4118A.

(9) PORT3 (10-pin header)
DSP port. Input/output MCLK, BICK, LRCK

(10) PORT4 (10-pin header)
DSP port. Input SDTI1, SDTI2 and output SDTO1, SDTO2, SDTO3.

(11) PORT5 (10-pin header)
DSP port. Input/output SCL and SDA. SDA(ACK) not used. May alternatively be used to write AK4616 registers from PC.

(12) EXT (RCA jack)
Input external clock source.

**Evaluation Board Manual**

## ■ Operation sequence

**[1] Power supply line settings**

**[2] Jumper pins settings**

**[3] DIP switches settings**

**[4] Toggle switches settings**

**[5] LED indication**

**[6] Register control (Serial control)**

**[7] Evaluation modes**

Refer to the following pages for details.

## [1] Power Supply Line Settings

| Name | Color | Voltage Range | Typ Voltages | Function | Comments | Default Settings |
|---|---|---|---|---|---|---|
| VOP+ (12V) | Red | +9~+12V | +12V | Regulator power supply OPAmp +terminal power supply | Should always be connected | +12V |
| A3V31 | Green | +3.0~+3.6V | +3.3V | AK4616 A3V31 | 3.3V regulator is used (JP20 = REG) by default, when jack is used (JP20=A3V31). | REG |
| A3V32 | Green | +3.0~+3.6V | +3.3V | AK4616 A3V32 | 3.3V regulator is used (JP21 = REG) by default, when jack is used (JP21=A3V32). | REG |
| D3V3 | Green | +3.0~+3.6V | +3.3V | AK4616 D3V3 | 3.3V regulator is used (JP22 = REG) by default, when jack is used (JP22=D3V3). | REG |
| D1V8 | Green | +1.7~+1.9V | +1.8V | AK4616 D1V8 | 1.8V regulator is used (JP24 = REG) by default, when jack is used (JP24=D1V8). | REG |
| D3V | Green | +3.0~+3.6V | +3.3V | AK4118 D3V, Logic IC power supply | 3.3V regulator is used (JP23 = REG) by default, when jack is used (JP23=D3V). | REG |
| AGND | Black | 0V | 0V | Analog ground | Should always be connected | 0V |
| DGND | Black | 0V | 0V | Digital ground | Should always be connected | 0V |

Table 1. Power supply line setting

Note 1. Each power supply should be powered up while PDN pin = “L”. The PDN pin may be brought to “H” after all power supplies are powered up. Do not turn off AK4616 while surrounding devices are still powered on and I2C bus is in use. A3V31 and A3V32 must be connected to the same power supply.

<Operation procedure>

1) Connect power supply as above.

2) Set up jumper pin and evaluation mode (See below for details)

3) Power-up
   Reset AK4616 once by bringing SW2 “L” upon power up.
   The dummy command will be executed automatically when ACK isn’t returned.

## [2] Jumper Pin Settings

| No | Names | Default | Functions |
|---|---|---|---|
| 1 | AINLN-SEL | AIN1LN | Select Lch Analog Negative input to AK4616 (U1)<br>AIN1LN: Lch Analog Negative Input 1 Pin (default)<br>AIN2LN: Lch Analog Negative Input 2 Pin<br>AIN3LN: Lch Analog Negative Input 3 Pin |
| 2 | AINRN-SEL | AIN1RN | Select Rch Analog Negative input to AK4616 (U1)<br>AIN1LN: Rch Analog Negative Input 1 Pin (default)<br>AIN2LN: Rch Analog Negative Input 2 Pin<br>AIN3LN: Rch Analog Negative Input 3 Pin |
| 3 | AINLP-SEL | AIN1LP | Select Lch Analog Positive input to AK4616 (U1)<br>AIN1LN: Lch Analog Positive Input 1 Pin (default)<br>AIN2LN: Lch Analog Positive Input 2 Pin<br>AIN3LN: Lch Analog Positive Input 3 Pin |
| 4 | AINRP-SEL | AIN1RP | Select Rch Analog Positive input to AK4616 (U1)<br>AIN1LN: Rch Analog Positive Input 1 Pin (default)<br>AIN2LN: Rch Analog Positive Input 2 Pin<br>AIN3LN: Rch Analog Positive Input 3 Pin |
| 5 | MINN | Open | Select Microphone Negative input to AK4616 (U1)<br>Open: Single-End (MDIF bit = “0”) (default)<br>Short: Differential (MDIF bit = “1”) |
| 6 | LIN1 | | |
| 7 | MIN/MINP | | |
| 8 | BICK-SEL | DIR | Select input to AK4616 (U1) BICK Buffer<br>64fs: 64fs divider6<br>32fs: 32fs divider<br>DIR: DIR-AK4118-BICK (default)<br>10-pin: 10pin-BICK<br>Open: No signal |
| 9 | BICK-PHASE | THR | Select polarity (non-inverted output / inverted output) of 10pin-BICK outputs.<br>THR: Non-inverted output. (default)<br>INV: Inverted output. |
| 10 | LRCK-SEL | DIR | Select input to AK4616 (U1) LRCK Buffer<br>1fs: 1fs divider<br>DIR: DIR-AK4118-BICK (default)<br>10-pin: 10pin-BICK<br>Open: No signal |
| 11 | DAUX-SEL | SDTO1 | Select input to DIT:AK4118 (U12) DAUX<br>SDTO1: AK4616-SDTO1 (pin 1) (default)<br>SDTO2: AK4615-SDTO2 (pin 3)<br>Open: Connect DIT-AK4118-DAUX input side of JP9 to Digital ground with a clip. No signal |
| 12 | SDTI3-SEL | DIR | Select input to AK4616 (U1) SDTI3<br>DIR: DIR-AK4118-SDTO (default)<br>10-pin: 10pin-SDTI3<br>GND: Digital ground |
| 13 | SDTI2-SEL | DIR | Select input to AK4616 (U1) SDTI2<br>DIR: DIR-AK4118-SDTO (default)<br>10-pin: 10pin-SDTI2<br>GND: Digital ground |

| | | | |
|---|---|---|---|
| 14 | SDTI1-SEL | DIR | Select input to AK4616 (U1) SDTI1<br>DIR: DIR-AK4118-SDTO (default)<br>10-pin: 10pin-SDTI1<br>GND: Digital ground |
| 15 | MCKI-SEL | DIR | 10-pin: 10pin-MCKI<br>EXT: External MCLK (JACK: J12) input<br>GND: GND<br>DIR: DIR-AK4118-MCKI (default) |
| 16 | EXT | Short | Open: No input<br>Short: External MCLK(JACK: J11) input (default) |
| 17 | CTRL-SEL | SDA | Select control setting mode<br>SDA/SCL: Serial (default)<br>SDA (ACK): Open ***SDA Ack not used<br>10-pin: Parallel |
| 18 | PIC | Open | Connect PIC microchip connector |
| 20 | A3V31-SEL | REG | Select power supply to A3V31<br>REG: Regulator T2 (default)<br>(When regulator “T2” is selected, power supply jack “A3V31” should be open.)<br>JACK: Power supply jack “A3V31” |
| 21 | A3V32-SEL | REG | Select power supply to A3V32<br>REG: Regulator T2 (default)<br>(When regulator “T2” is selected, power supply jack “A3V32” should be open.)<br>JACK: Power supply jack “A3V32” |
| 22 | D3V3-SEL | REG | Select power supply to D3V3<br>REG: Regulator T3 (default)<br>(When regulator “T3” is selected, power supply jack “D3V3” should be open.)<br>JACK: Power supply jack “D3V3” |
| 23 | D3V-SEL | REG | Select power supply to D3V<br>REG: Regulator T3 (default)<br>(When regulator “T3” is selected, power supply jack “D3V” should be open.)<br>JACK: Power supply jack “D3V” |
| 24 | D1V8-SEL | REG | Select power supply to D1V8<br>REG: Regulator T4 (default)<br>(When regulator “T4” is selected, power supply jack “D1V8” should be open.)<br>JACK: Power supply jack “D1V8” |
| 25 | GND | Short | Select connection / separation between analog ground and digital ground.<br>Open: Separate analog ground from digital ground<br>Short: Connect analog ground to digital ground (default) |

Table 2. Main board Jumper pin setting

## [3] DIP switch setting

**(1). Setting for SW1 (Sets AK4118 (U12) audio format and master clock setting)**

| No. | Switch Name | Function | default |
|---|---|---|---|
| 1 | DIF0 | Set-up of DIF0 pin. (in parallel mode) | H |
| 2 | DIF1 | Set-up of DIF1 pin. (in parallel mode) | L |
| 3 | DIF2 | Set-up of DIF2 pin. (in parallel mode) | H |
| 4 | OCKS1 | Set-up of OCKS1 pin. (in parallel mode) | L |
| 5 | OCKS0 | Set-up of OCKS0 pin. (in parallel mode) | L |

Table 3. SW1 Setting

| Mode | DIF2 pin (SW1_1) | DIF1 pin (SW1_2) | DIF0 pin (SW1_3) | DAUX | SDTO | LRCK | | BICK | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | DIF2 bit | DIF1 bit | DIF0 bit | | | | I/O | | I/O | |
| 0 | 0 | 0 | 0 | 24bit, Left justified | 16bit, Right justified | H/L | O | 64fs | O | |
| 1 | 0 | 0 | 1 | 24bit, Left justified | 18bit, Right justified | H/L | O | 64fs | O | |
| 2 | 0 | 1 | 0 | 24bit, Left justified | 20bit, Right justified | H/L | O | 64fs | O | |
| 3 | 0 | 1 | 1 | 24bit, Left justified | 24bit, Right justified | H/L | O | 64fs | O | |
| 4 | 1 | 0 | 0 | 24bit, Left justified | 24bit, Left justified | H/L | O | 64fs | O | |
| 5 | 1 | 0 | 1 | 24bit, $I^2S$ | 24bit, $I^2S$ | L/H | O | 64fs | O | |
| 6 | 1 | 1 | 0 | 24bit, Left justified | 24bit, Left justified | H/L | I | 64-128fs | I | default |
| 7 | 1 | 1 | 1 | 24bit, $I^2S$ | 24bit, $I^2S$ | L/H | I | 64-128fs | I | |

Table 4. Audio format

| OCKS1 pin (SW1_4) | OCKS0 pin (SW1_5) | (X'tal) | MCKO1 | MCKO2 | fs (max) | |
|---|---|---|---|---|---|---|
| OCKS1 bit | OCKS0 bit | | | | | |
| 0 | 0 | 256fs | 256fs | 256fs | 96 kHz | default |
| 0 | 1 | 256fs | 256fs | 128fs | 96 kHz | |
| 1 | 0 | 512fs | 512fs | 256fs | 48 kHz | |
| 1 | 1 | 128fs | 128fs | 64fs | 192 kHz | |

Table 5. Master Clock Frequency Select

## [4] Toggle switch settings

**SW2, SW3, SW4 Settings**

| | | |
|---|---|---|
| SW2 | DIO-PDN | Power down switch for DIR/T: AK4118 (U6).<br>Reset AK4118 (U6) once by brining SW2 to "L" once upon power-up.<br>Keep "H" when AK4118 is in use; keep "L" when AK4118 is not in use. |
| SW3 | PDN | Power down switch for AK4616 (U1).<br>Reset AK4616 (U1) once by brining SW3 to "L" once upon power-up.<br>Keep "H" during normal operation. |

Table 6. Toggle switch settings

## [5] LED

**LE1 Indication**

| | | |
|---|---|---|
| LE1 | INT0 | DIR: AK4118 (U6) INT0 pin output. Turns on when DIR: AK4118 (U6) is unlocked |

Table 7. LED Indication

## [6] Register control

AKD4616-A can be controlled via USB (serial port) or printer port (parallel port) of IBM-AT. Connect board to PC using the USB cable (U22 – serial) or 10-wire flat cable (Port5 – uP-IF) included with the AKD4616-A. There is a mark on the no.1-pin of the 10-pin connector. See Figure 3. The pin assignments of PORT5 below.

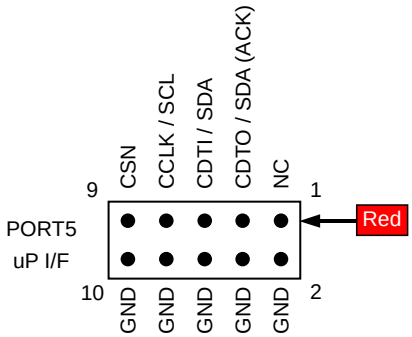



Figure 3. The pin assignments of PORT5

The control software is packed with the evaluation board. The software operation sequence is included in the evaluation board manual.

**[7] Evaluation modes**

**(1) ADC→DAC (Analog → Analog) by internal loop back**

**(2) ADC (Analog → Digital): Stereo ADC and Monaural ADC (Microphone Input)**

**(3) DAC (Digital → Analog)**

### (1) ADC→DAC (Analog → Analog) by internal loop back

■ **Toggle switch setting:**

| SW2 | SW3 |
|---|---|
| H | L→H |
| AK4118(U6) : Used | AK4616(U1) : Used |

Table 8. Toggle switch setting

■ **Start up Control Register Setting**

Set Addr: 00H = "31" to release Internal timing reset and power on ADC and DAC. Other control register settings are default.

Dummy Command will be executed automatically.

RSTN bit: Internal timing reset
0: Reset.
1: Normal operation (default)

PMADC bit: Power management of mono-stereo
0: All ADC's power-down
1: Normal operation (default)

PMDAC bit: Power management of DAC1-3
0: All DAC's power-down. PMDA1-3 bits are invalid.
1: Normal operation (default). PMDA1-3 bits are valid.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management | 0 | PMMB | PMADC | PMDAC | 0 | 0 | 0 | RSTN |
| R/W | | RD | R/W | R/W | R/W | RD | RD | RD | R/W |
| Setting | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

Table 9. Addr 00H control register setting

■ **Analog Input Selector for Stereo ADC**

| AIN1 bit | AIN0 bit | Input Selector |
|---|---|---|
| 0 | 0 | AIN1L/AIN1R (default) |
| 0 | 1 | AIN2L/AIN2R |
| 1 | 0 | AIN3L/AIN3R |
| 1 | 1 | AIN4L/AIN4R |

Table 10a.Input Selector for ADC

**Control Register Setting:**

AIN1-0 bit: ADC Input Table

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Input Selector | 0 | 0 | 0 | DACIN | MOMIX | MDIF | AIN1 | AIN0 |
| R/W | | RD | RD | RD | R/W | R/W | R/W | R/W | R/W |
| Setting | | 0 | 0 | 0 | 0 | 0 | 0 | X | X |

Table 10b. Addr 04H control register setting

Change jumper setting for JP1-4 to corresponding input channel (AIN1-3).

For all stereo ADC Inputs (AIN1-4), analog signal output from both AOUT1 and AOUT2.

## (2) ADC (Analog → Digital): Stereo ADC and Monaural ADC (Microphone Input)

■ **Toggle switch setting:**

| SW2 | SW3 |
|---|---|
| H | L→H |
| AK4118(U6) : Used | AK4616(U1) : Used |

Table 11. Toggle switch setting

■ **Start up Control Register Setting**

Set Addr: 00H = "21" to release Internal timing reset and power on ADC. Other control register settings are default. Dummy Command will be executed automatically.

RSTN bit: Internal timing reset
0: Reset.
1: Normal operation (default)

PMADC bit: Power management of mono-stereo
0: All ADC's power-down
1: Normal operation (default)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management | 0 | PMMB | PMADC | PMDAC | 0 | 0 | 0 | RSTN |
| R/W | | RD | R/W | R/W | R/W | RD | RD | RD | R/W |
| Setting | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

Table 12. Addr 00H control register setting

■ **Analog Input Selector for Stereo ADC**

**Control Register Setting:**

AIN1-0 bit: ADC Input Table

| AIN1 bit | AIN0 bit | Input Selector |
|---|---|---|
| 0 | 0 | AIN1L/AIN1R (default) |
| 0 | 1 | AIN2L/AIN2R |
| 1 | 0 | AIN3L/AIN3R |
| 1 | 1 | AIN4L/AIN4R |

Table 13a.Input Selector for ADC

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Input Selector | 0 | 0 | 0 | DACIN | MOMIX | MDIF | AIN1 | AIN0 |
| R/W | | RD | RD | RD | R/W | R/W | R/W | R/W | R/W |
| Setting | | 0 | 0 | 0 | 0 | 0 | 0 | X | X |

Table 13b. Addr 04H control register setting

■ **Analog Input Selector for Monaural ADC**

**Control Register Setting:**

MDIF bit: Single-ended/Differential Input Select for Microphone Amp
0: Single-ended input to MIN/MINP pin. Leave MINN pin open. (default)
1: Differential input (MINP/MINN pin).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Input Selector | 0 | 0 | 0 | DACIN | MOMIX | MDIF | AIN1 | AIN0 |
| R/W | | RD | RD | RD | R/W | R/W | R/W | R/W | R/W |
| Setting | | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 |

Table 14b. Addr 04H control register setting

◆ For Differential Input Select for Microphone Amp (MDIF="1"):
Change to following jumper setting:
JP5 (MINN) = short
JP11 (DAUX-SEL) = SDTO2

### (3) DAC (Digital → Analog)

■ **Toggle switch setting:**

| SW2 | SW3 |
|---|---|
| H | L→H |
| AK4118(U6) : Used | AK4616(U1) : Used |

Table 15. Toggle switch setting

■ **Start up Control Register Setting**

Set Addr: 00H = "11" to release Internal timing reset and power on DAC. Other control register settings are default. Dummy Command will be executed automatically.

RSTN bit: Internal timing reset
0: Reset.
1: Normal operation (default)

PMDAC bit: Power management of DAC1-3
0: All DAC's power-down. PMDA1-3 bits are invalid.
1: Normal operation (default). PMDA1-3 bits are valid.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management | 0 | PMMB | PMADC | PMDAC | 0 | 0 | 0 | RSTN |
| R/W | | RD | R/W | R/W | R/W | RD | RD | RD | R/W |
| Setting | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

Table 16. Addr 00H control register setting

■ **Input Selector for DAC**

**Control Register Setting:**

DACIN bit: Input selector for DAC1,2

| DACIN bit | Input Selector |
|---|---|
| 0 | ADC (default) |
| 1 | DOUTL/R |

Table 17a. Input Selector for DAC1 and DAC2

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Input Selector | 0 | 0 | 0 | DACIN | MOMIX | MDIF | AIN1 | AIN0 |
| R/W | | RD | RD | RD | R/W | R/W | R/W | R/W | R/W |
| Setting | | 0 | 0 | 0 | 1 | 0 | 0 | X | X |

Table 17b. Addr 04H control register setting

* When DACIN bit = "0", the digital ADC output is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-2 is ignored. The audio format of SDTO at loopback mode becomes mode 3 at mode 0, 1, 2, and 3, and mode 4 at mode 4, respectively. DACIN bit should be set "1" in TDM mode.

■ **Power management of DAC**

**Control Register Setting:**

PMDA3-1 bit: Power management of DAC 1-3 (0: Power-down, 1: Normal operation)
PMDA1 bit: Power management control of DAC1
PMDA2 bit: Power management control of DAC2
PMDA3 bit: Power management control of DAC3

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|

| 01H | Power Management 2 | 0 | 0 | 0 | 0 | 0 | PMDA3 | PMDA2 | PMDA1 |
|---|---|---|---|---|---|---|---|---|---|
| R/W | | RD | RD | RD | RD | RD | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Table 18. Addr 01H control register setting

Only the DAC bit being used should be powered on for best results.

## Control Software Manual

### ■ Set-up evaluation board and control software

1. Set up AKD4616-A evaluation board according to above instructions.
2. Connect PC with AKD4616-A evaluation board by USB cable (included in package).
3. Insert the CD-ROM labeled “AKD4616-A Evaluation Kit” into the CD-ROM drive.
4. Access the CD-ROM drive, double-click on “akd4616-a.exe” and set up the control program.
5. Evaluate according to the following.

### ■ Operation flow

Set up control program as above and open control program.
The following operation screen will be shown. (Default setting)

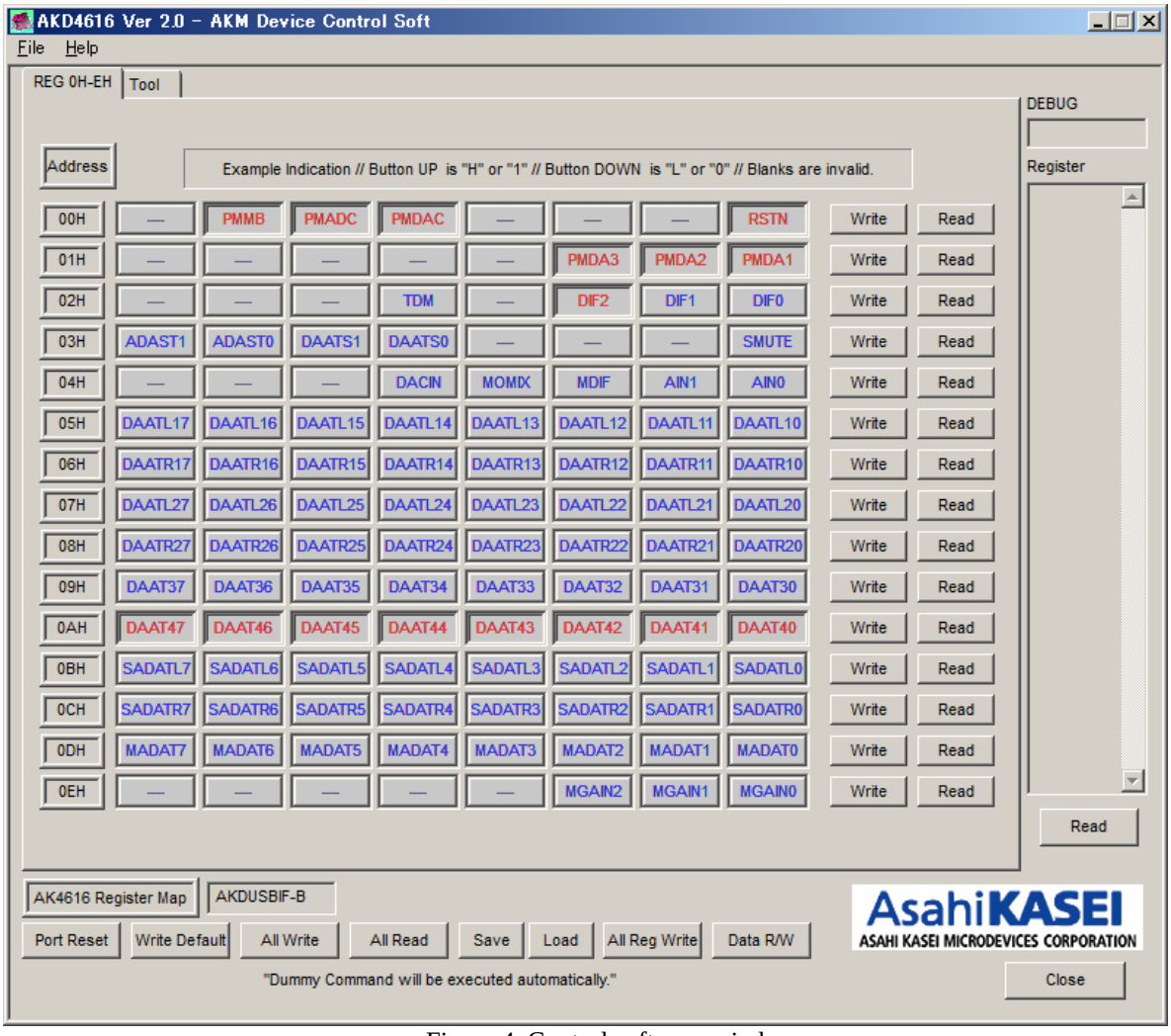



Figure 4. Control software window

Input registers accordingly into dialog box to evaluate AK4616.

## ■ Button Functions

1. [Port Reset] : Set up USB interface board (AKDUSBIF-B).
2. [Write Default] : Initialize all register setting.
3. [All Write] : Write all registers currently displayed.
4. [All Read] : Read all register setting.
5. [Save] : Save the current register setting to .akr file.
6. [Load] : Load register setting from saved .akr file.
7. [All Reg Write] : Opens “All Register Write” dialog box. (see Dialog boxes below)
8. [Data R/W] : Opens “Data Read/Write” dialog box . (see Dialog boxes below)
9. [Read] : Read and display current register setting in register window (on right side of main window). Different from [All Read] as it does not reflect to the register map.
10. [Close] : Close Control Software window.

## Dialog boxes

### 1. [All Register Write]: Dialog box to write register setting files

Clicking the [All Reg Write] button in the main window opens the dialog box below.
Multiple register setting files created by the [SAVE] button can be set and applied.

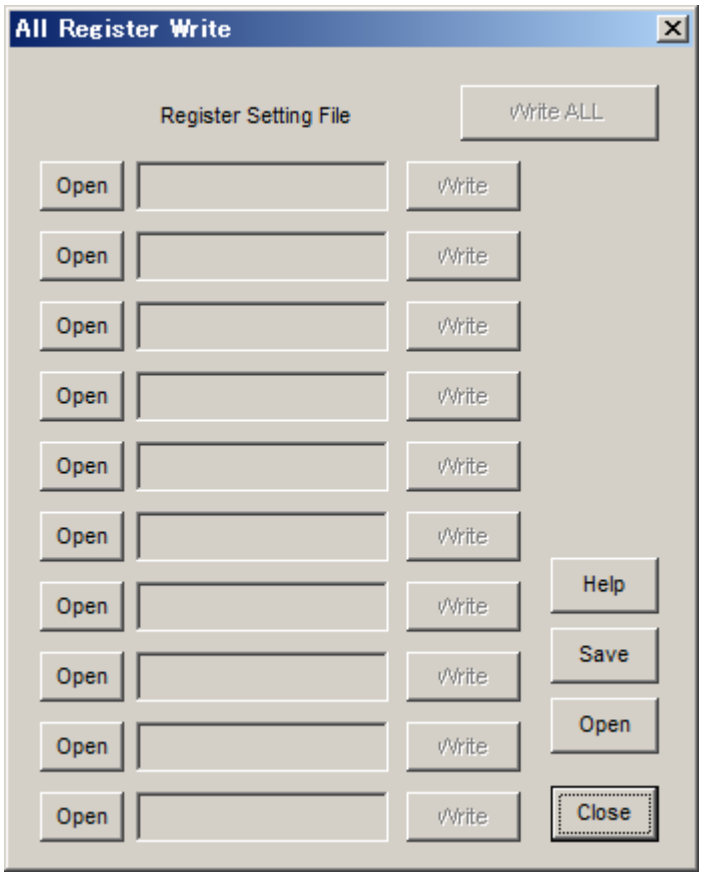



Figure 5. Window of [All Reg Write]

<Operation flow>
(1) Click [Open(left) Button.
(2) Select file (*.akr) and Click [Open] Button. Up to 10 files can be selected.
(3) Click [Write] to write each file. [Write ALL] writes all files selected.

**Button Functions:**
1. [Open (left)] : Select register setting file (*.akr).
2. [Write] : Write register setting file in textbox.
3. [Write ALL] : Write all register setting files selected. Write is executed in descending order.
4. [Help] : “Help” window pops up.
5. [Save] : Save the current register map setting (*.mar).
6. [Open (right)] : Load register map setting file (*.mar ).
7. [Close] : Close dialog box.

## 2. [Data Read/Write]: Dialog box to manually enter register setting

Click the [Data R/W] button in the main window to open the data read/write dialog box.
Data manually entered into Data box is written to the specified address.

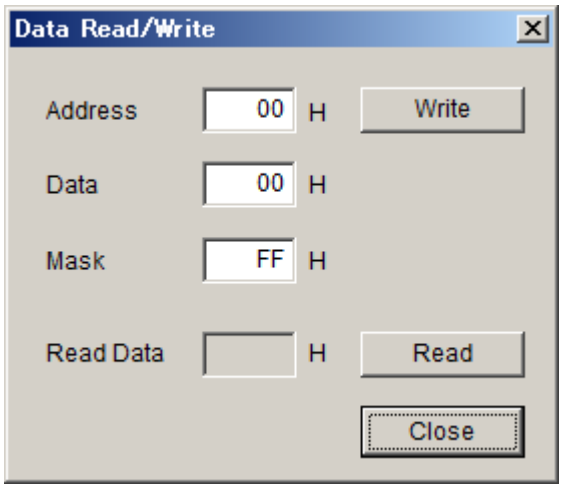



Figure 6. Window of [Data R/W]

**Textbox Functions:**
[Address] : Input register address in 2 hexadecimal digits.
[Data] : Input register data in 2 hexadecimal digits.
[Mask] : Input mask data in 2 hexadecimal digits. This value is AND-ed with input data.

**Button Functions:**
[Write] : Writes data generated from [Data] and [Mask] to register specified in [Address]
[Read] : Displays register data specified in [Address] in [Read Data] box in hexadedimal.
[Close] : Closes dialog box. To cancel a process close the dialog box without writing

※ Register map updated after [Write] and [Read] operation.

## Tab Functions

### 1. [REG]: Register Map

Register data is indicated on the register map. Each bit on the register map is a push-button switch. Button DOWN and red lettering indicates “1” and button UP with blue lettering indicates “0”. Buttons with “---“are undefined in the datasheet.

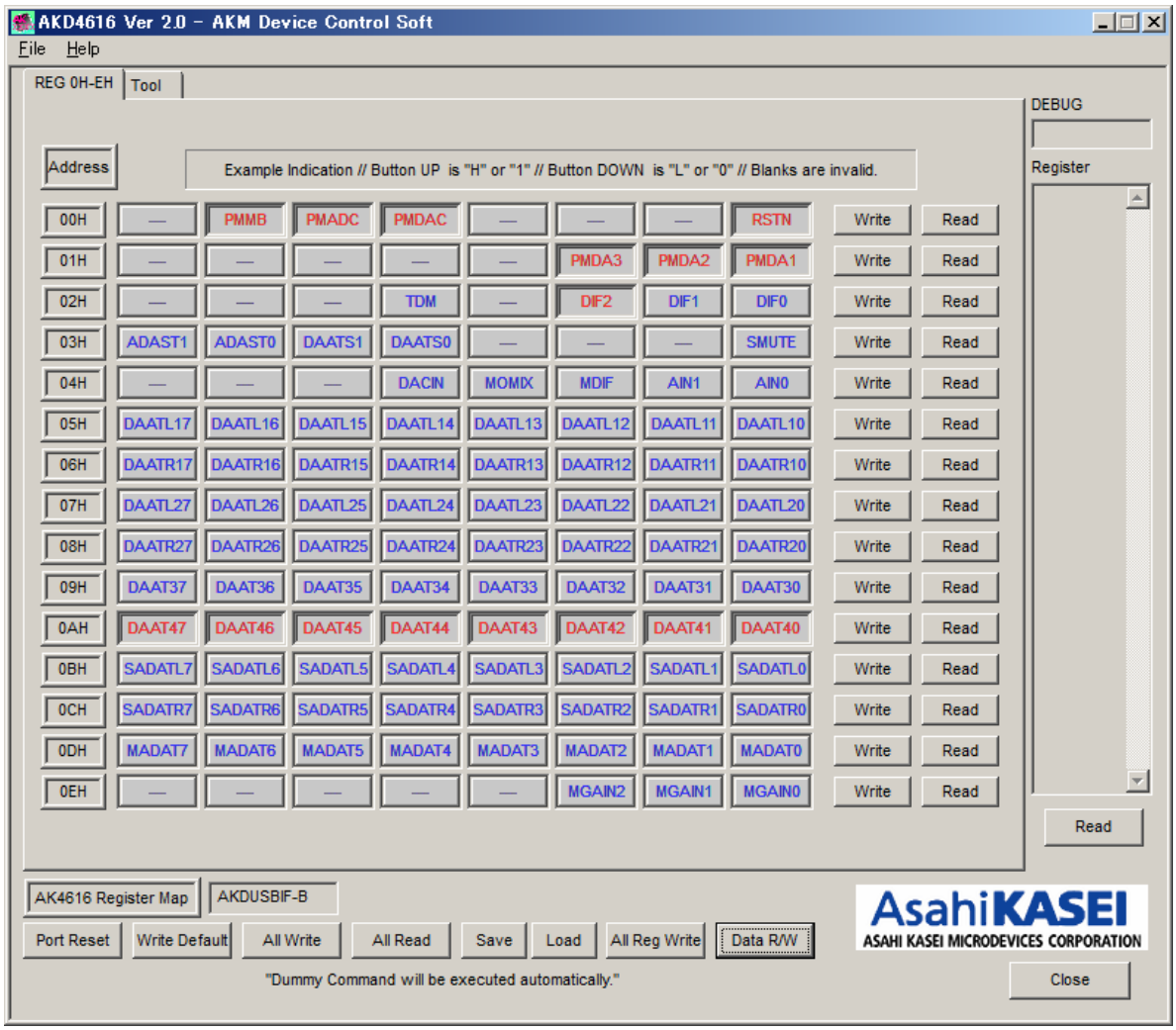



Figure 7. [REG] window

## 2. [Tool]: Testing Tools

This tab screen is for the evaluation testing tool.
Click button for each testing tool.

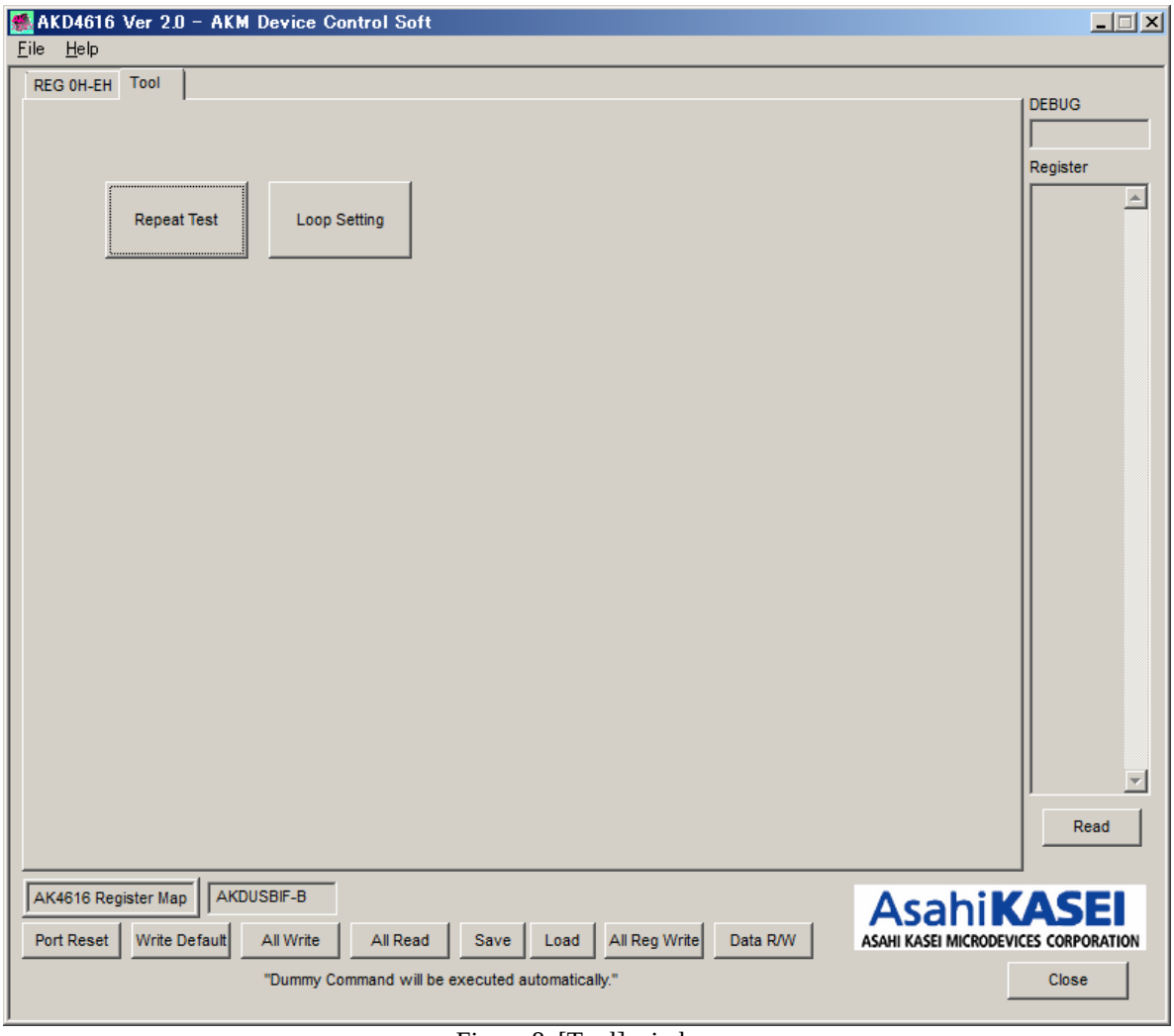



Figure 8. [Tool] window

## Measurement Results

### [Measurement condition]

- Measurement unit : Audio Precision, System two Cascade
- MCKI : 256fs (12.288MHz)
- BICK : 64fs
- fs : 48kHz
- Bit : 24bit
- Measurement Mode : ADC @ Master Mode / DAC @ Slave Mode
- Power Supply : VOP+(12V)=12V, GND
  A3V31=A3V32=3.3V (regulator), D3V=D3V3=3.3V (regulator),
  D1V8=1.8V (regulator)
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz @48kHz
- Temperature : Room

### [Measurement Results]

1. Stereo ADC

| | | Result | | Unit |
|---|---|---|---|---|
| | | Lch | Rch | |
| Stereo ADC : AIN1L/R => ADC => SDTO1 | | | | |
| S/(N+D) | fs = 48kHz (-1dBFS) | 88.6 | 88.7 | dB |
| DR | fs = 48kHz (-60dBFS, A-Weighted) | 98.5 | 98.5 | dB |
| S/N | fs = 48kHz (A-weighted) | 98.4 | 98.6 | dB |

2. Monaural ADC

| | | Result | | Unit |
|---|---|---|---|---|
| | | Single | Diff | |
| Mono ADC : MIC => Mono ADC => SDTO2 | | | | |
| S/(N+D) | fs = 48kHz (-1dBFS), MGAIN[2:0]=0h(0dB) | 87.4 | 87.6 | dB |
| | fs = 96kHz (-1dBFS ), MGAIN[2:0]=3h(+21dB) | 81.1 | 81.6 | |
| DR | fs = 48kHz (-60dBFS, A-Weighted), MGAIN[2:0]=0h(0dB) | 97.9 | 98.5 | dB |
| | fs = 48kHz (-60dBFS, A-Weighted), MGAIN[2:0]=3h(+21dB) | 85.8 | 85.2 | |
| S/N | fs = 48kHz (A-weighted), MGAIN[2:0]=0h(0dB) | 98.0 | 98.6 | dB |
| | fs = 48kHz (A-weighted), MGAIN[2:0]=3h(+21dB) | 85.8 | 85.2 | |

3. DAC1

| | | Result | | Unit |
|---|---|---|---|---|
| | | Lch | Rch | |
| DAC1 : SDTI1 => DAC1 => AOUT1 | | | | |
| S/(N+D) | fs = 48kHz (0dBFS) | 92.8 | 92.6 | dB |
| DR | fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL) | 104.9 | 104.9 | dB |
| S/N | fs = 48kHz (A-weighted, 20kHz SPCL) | 105.0 | 104.9 | dB |

4. DAC3

| | | Result | | Unit |
|---|---|---|---|---|
| | | AOUT3 | - | |
| DAC3 : SDT31 => Mono DAC => AOUT3 | | | | |
| S/(N+D) | fs = 48kHz (0dBFS) | 93.9 | - | dB |
| DR | fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL) | 107.2 | - | dB |
| S/N | fs = 48kHz (A-weighted, 20kHz SPCL) | 107.2 | - | dB |

## [Plot Data]

Stereo ADC (AIN1)
1. ADC1 (fs = 48kHz); AIN1(Diff) => ADC1 => SDTO1

AK4616 FFT Stereo ADC (AIN1L/R)
[fs=48kHz, fin=1kHz, -1dBFS]

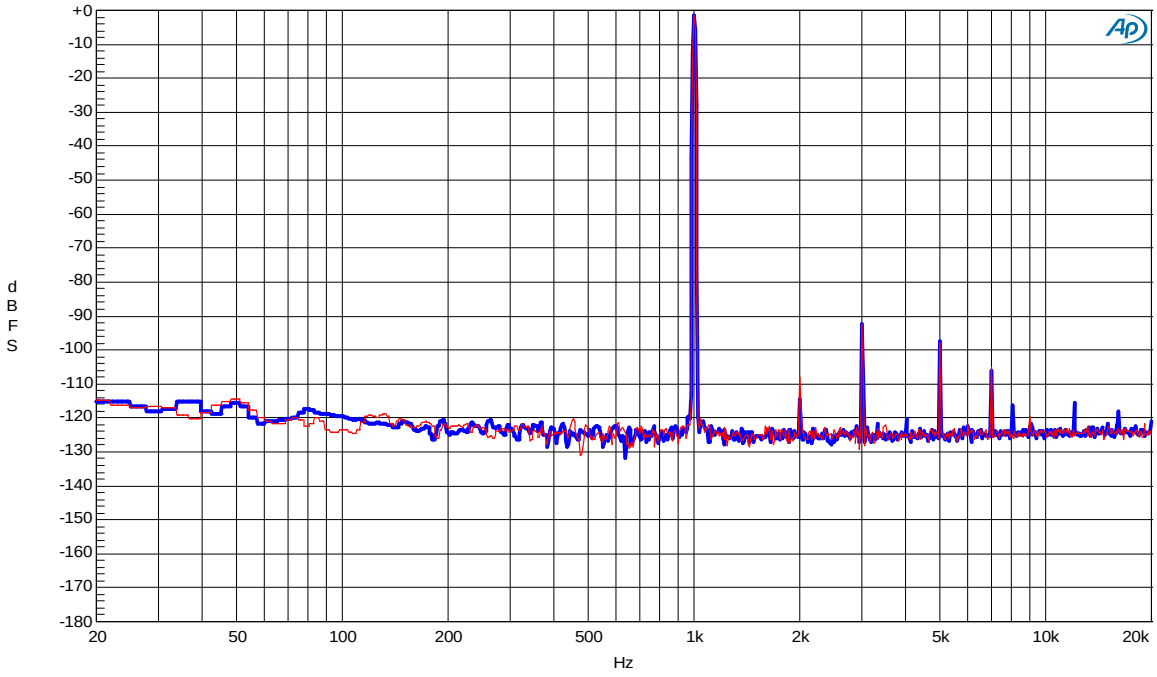



Figure 9. ADC1 – FFT (-1dBFS) [fs = 48kHz]

AK4616 FFT Stereo ADC (AIN1L/R)
[fs=48kHz, fin=1kHz, -60dBFS]

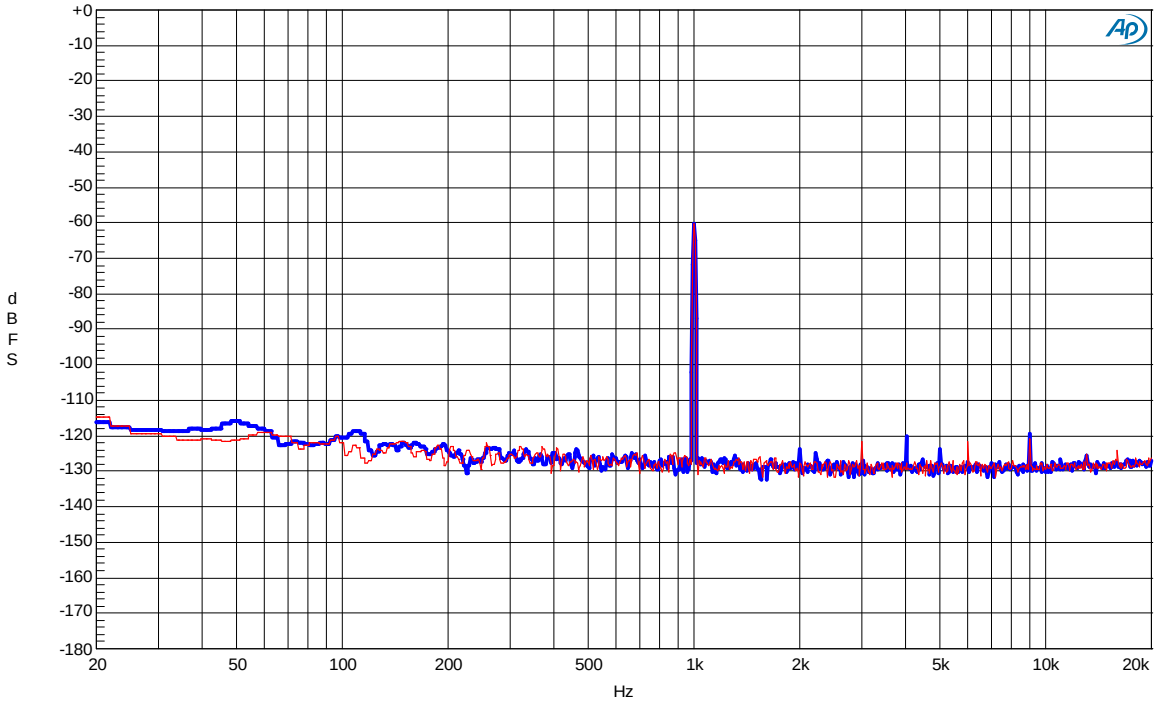



Figure 10. ADC1 – FFT (-60dBFS) [fs = 48kHz]

AK4616 FFT Stereo ADC (AIN1L/R)
[fs=48kHz, fin=1kHz, no signal]

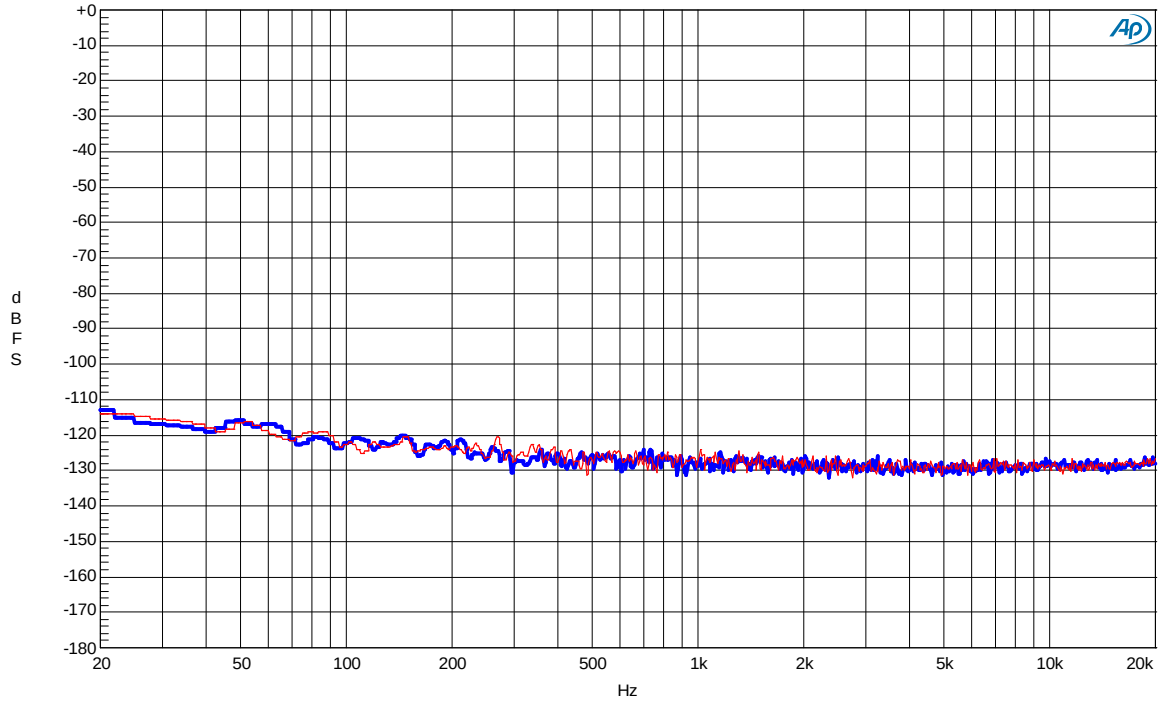



Figure 11. ADC1 – FFT (No Signal) [fs = 48kHz]

AK4616 THD+N vs Amplitude Stereo ADC (AIN1L/R)
[fs=48kHz, fin=1kHz]

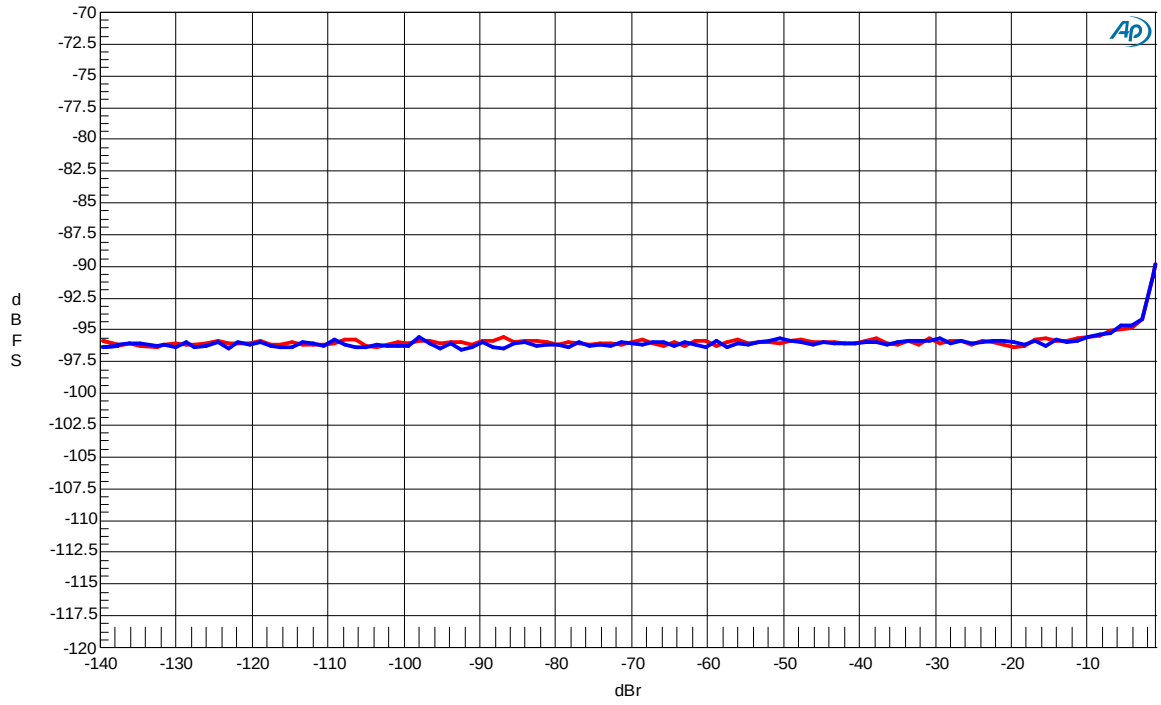



Figure 12. ADC1 – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4616 THD+N vs Input Frequency Stereo ADC (AIN1L/R)
[fs=48kHz, -1dBFS]

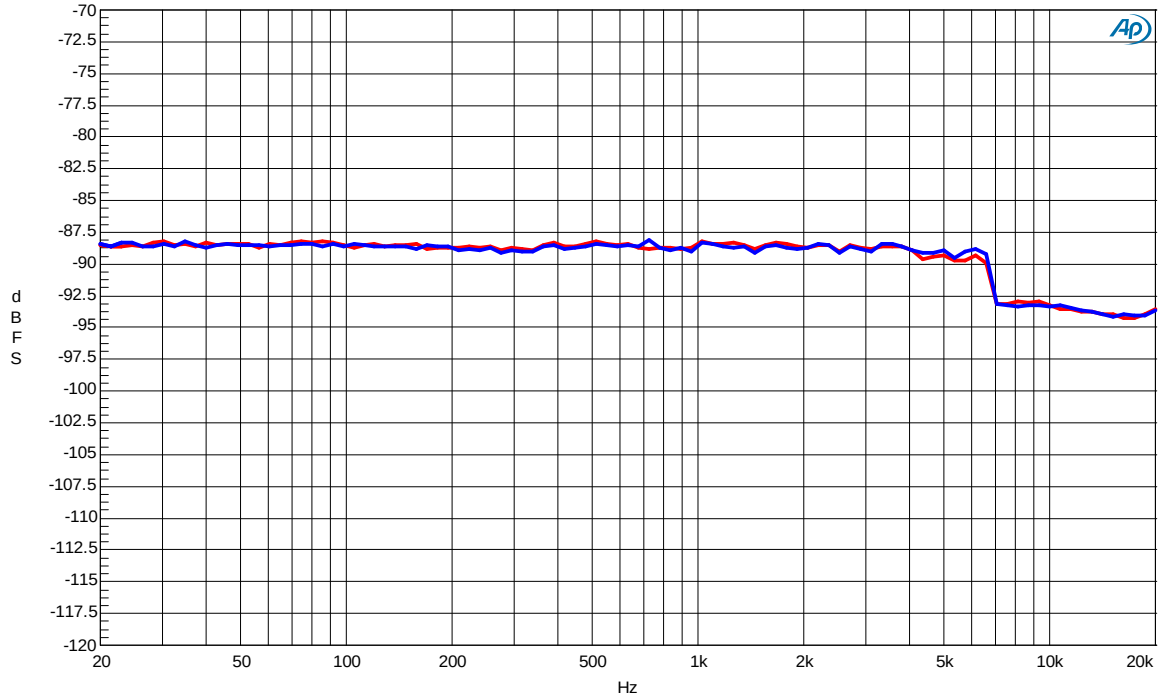



Figure 13. ADC1 – THD+N vs. Input Frequency [fs = 48kHz]

AK4616 Linearity Stereo ADC (AIN1L/R)
[fs=48kHz, fin=1kHz]

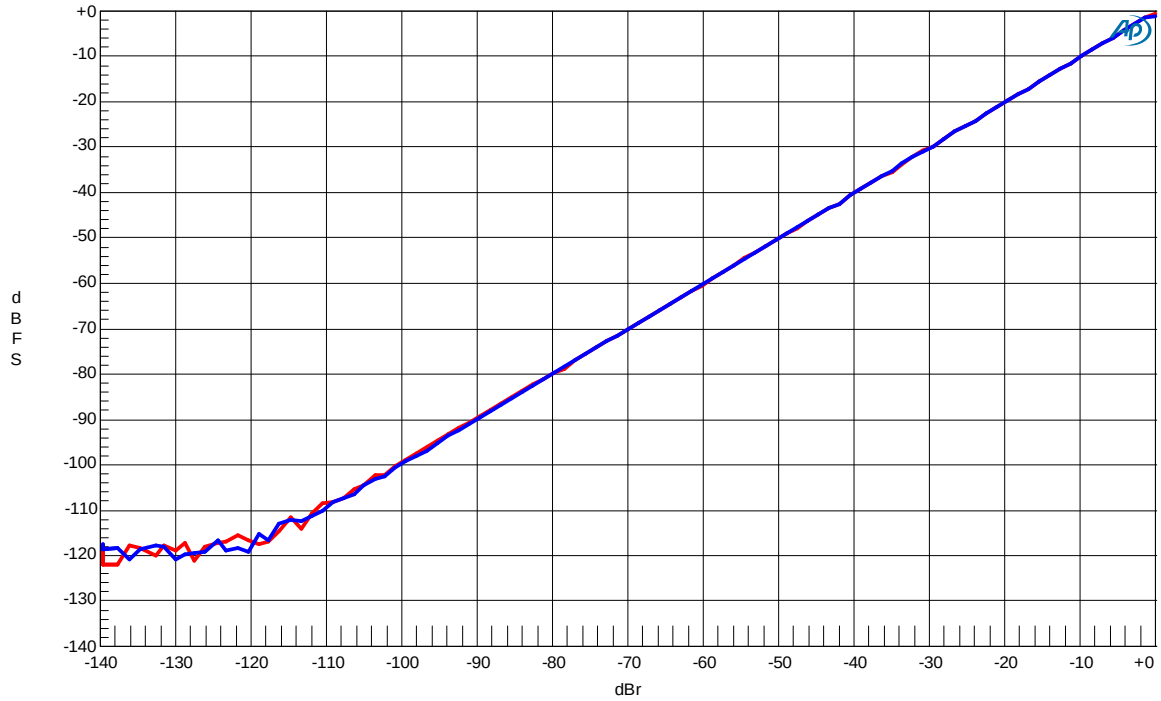



Figure 14. ADC1 – Linearity [fs = 48kHz]

AK4616 Frequency Response Stereo ADC (AIN1L/R)
[fs=48kHz, -1dBFS]

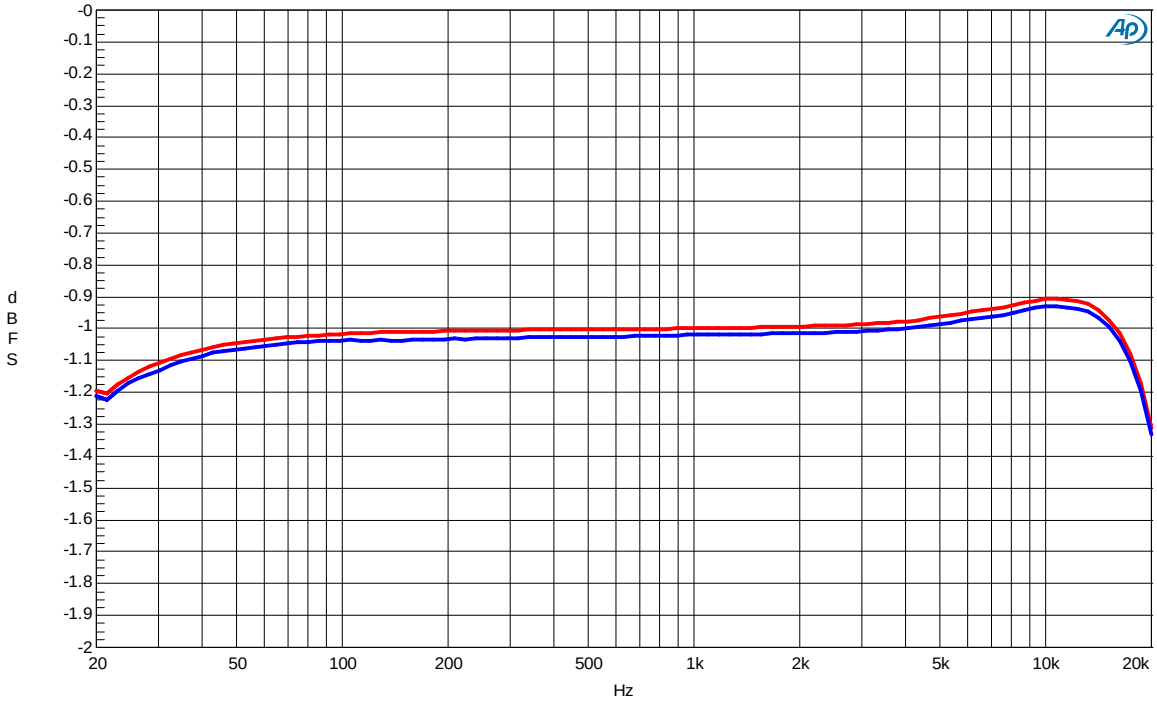



Figure 15. ADC1 – Frequency Response [fs = 48kHz]

AK4616 Crosstalk Stereo ADC (AIN1L/R)
[fs=48kHz, -1dBFS]

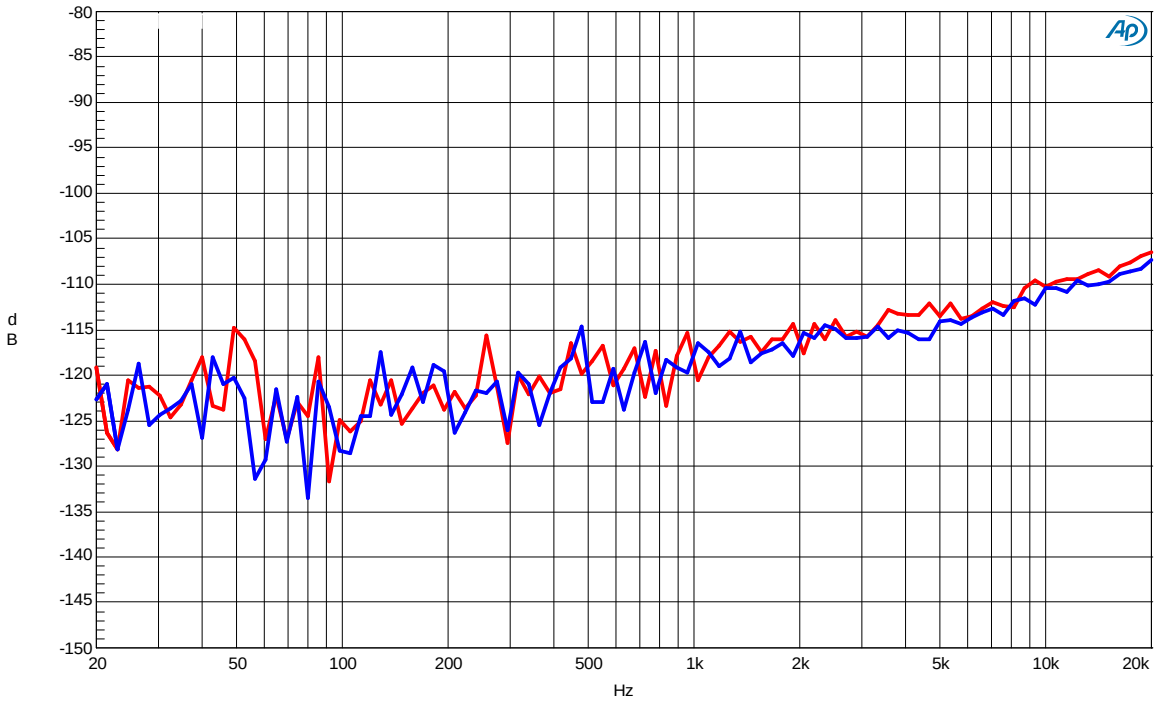



Figure 16. ADC1 – Crosstalk [fs = 48kHz]

2. ADC2 (fs = 48kHz); MIC (Single-end) => Mono ADC => SDTO2

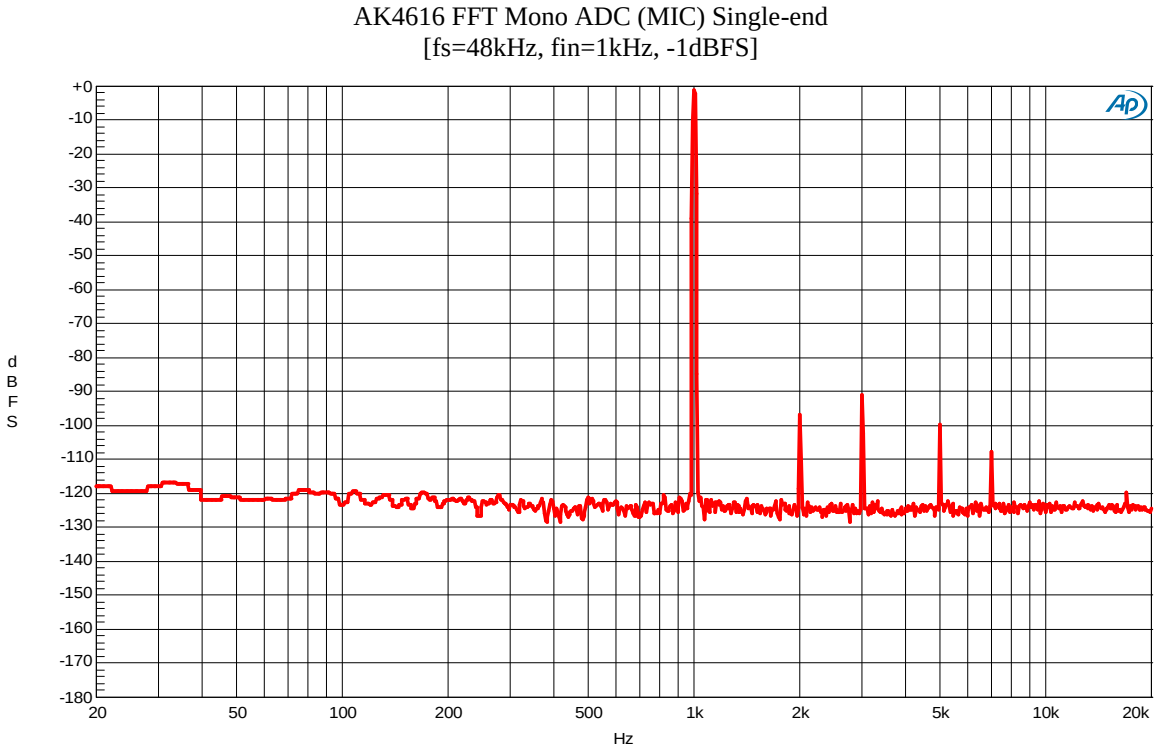



Figure 17. ADC2 – FFT (-1dBFS) [fs = 48kHz]

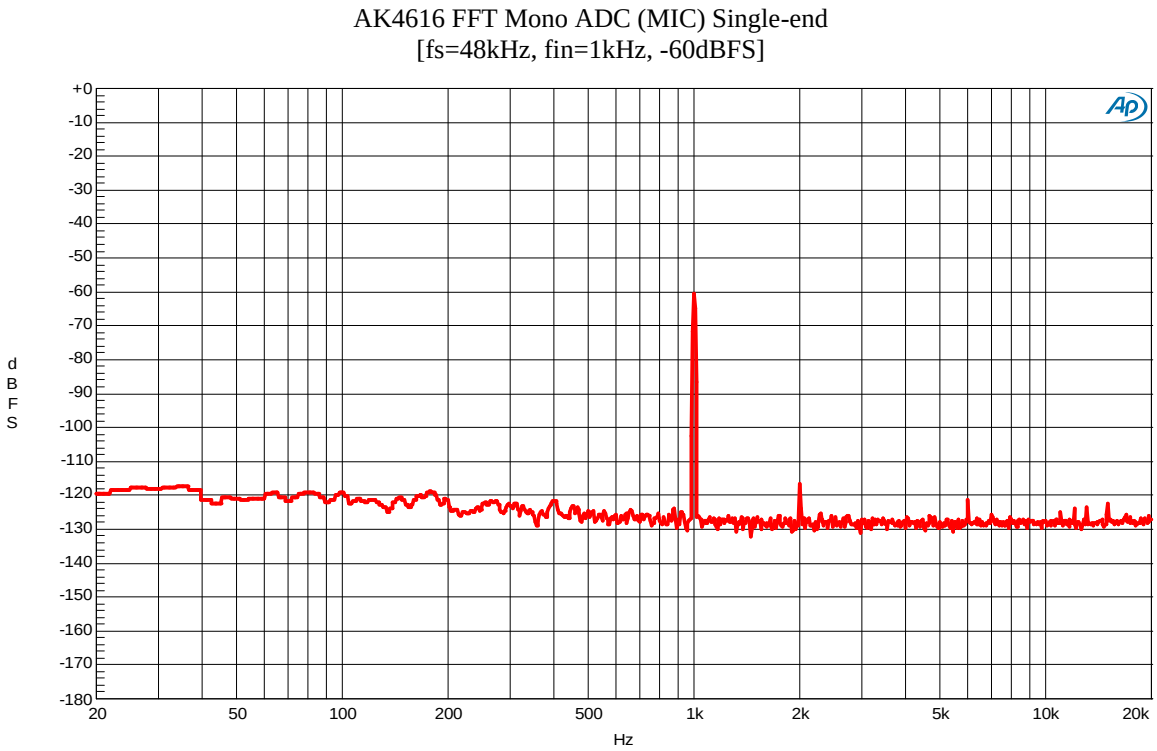



Figure 18. ADC2 – FFT (-60dBFS) [fs = 48kHz]

AK4616 FFT Mono ADC (MIC) Single-end
[fs=48kHz, fin=1kHz, no signal]

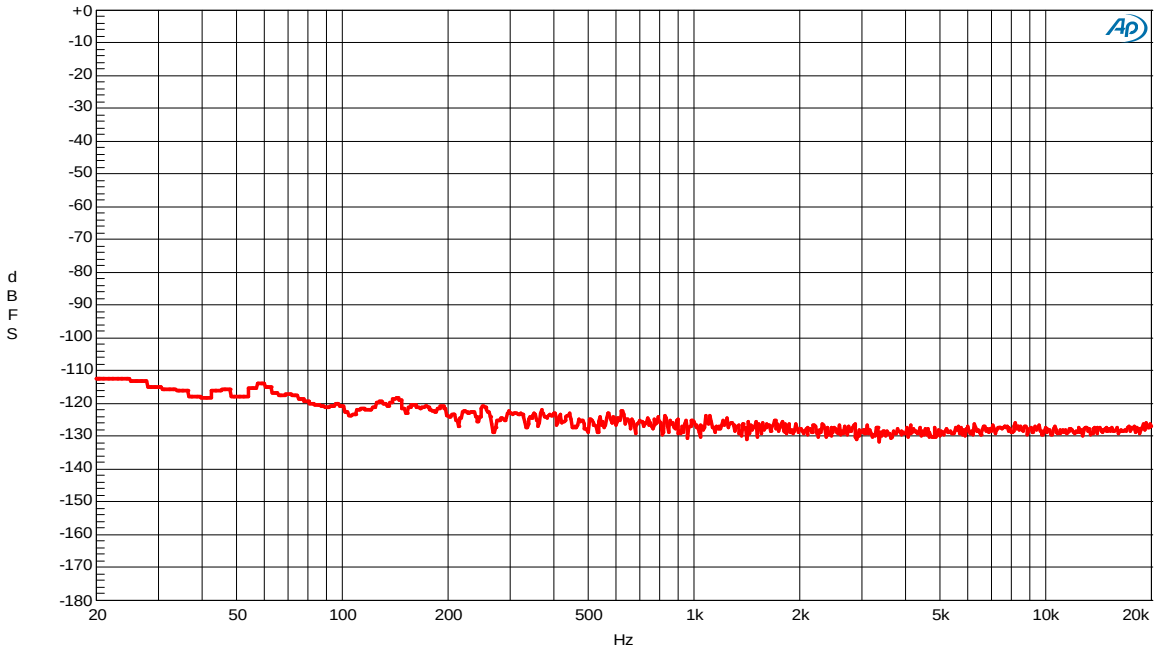



Figure 19. ADC2 – FFT (No Signal) [fs = 48kHz]

AK4616 THD+N vs Amplitude Mono ADC (MIC) Single-end
[fs=48kHz, fin=1kHz]

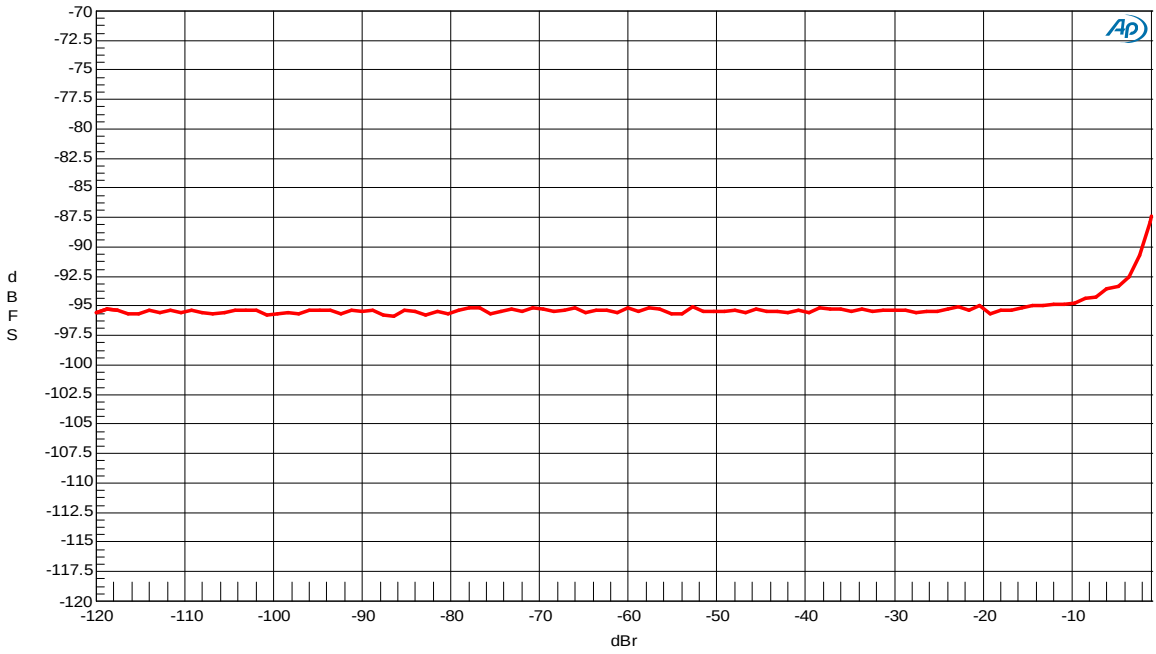



Figure 20. ADC2 – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4616 THD+N vs Input Frequency Mono ADC (MIC) Single-end
[fs=48kHz, -1dBFS] AMP Bypass

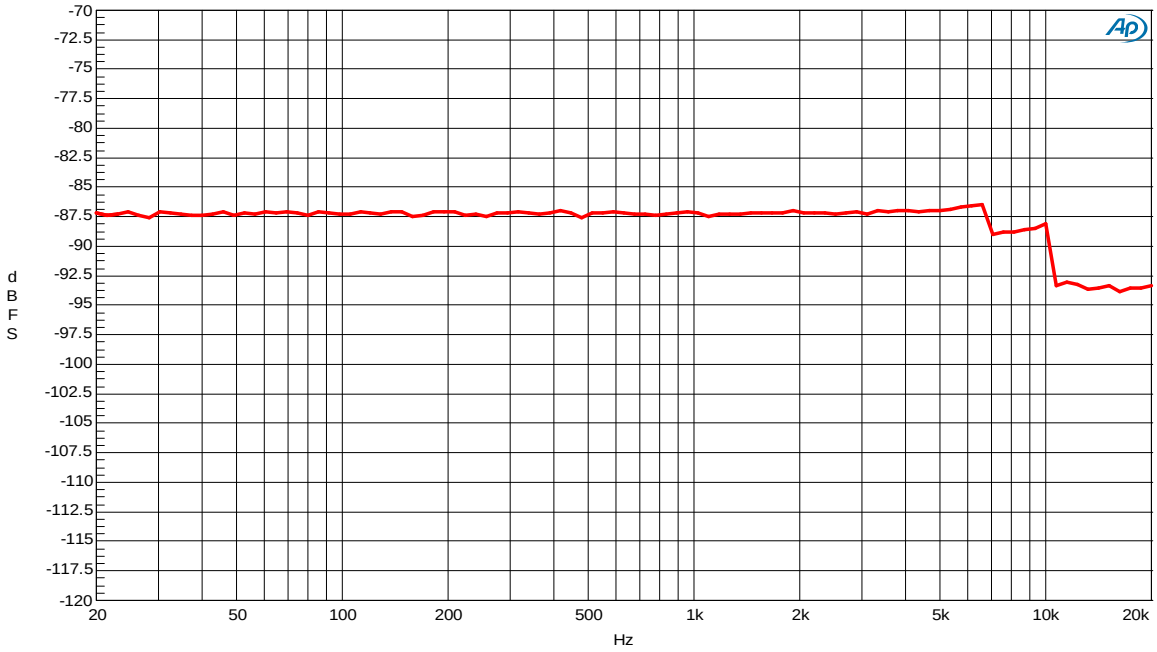



Figure 21. ADC2 – THD+N vs. Input Frequency [fs = 48kHz]

AK4616 Linearity Mono ADC (MIC) Single-end
[fs=48kHz, fin=1kHz]

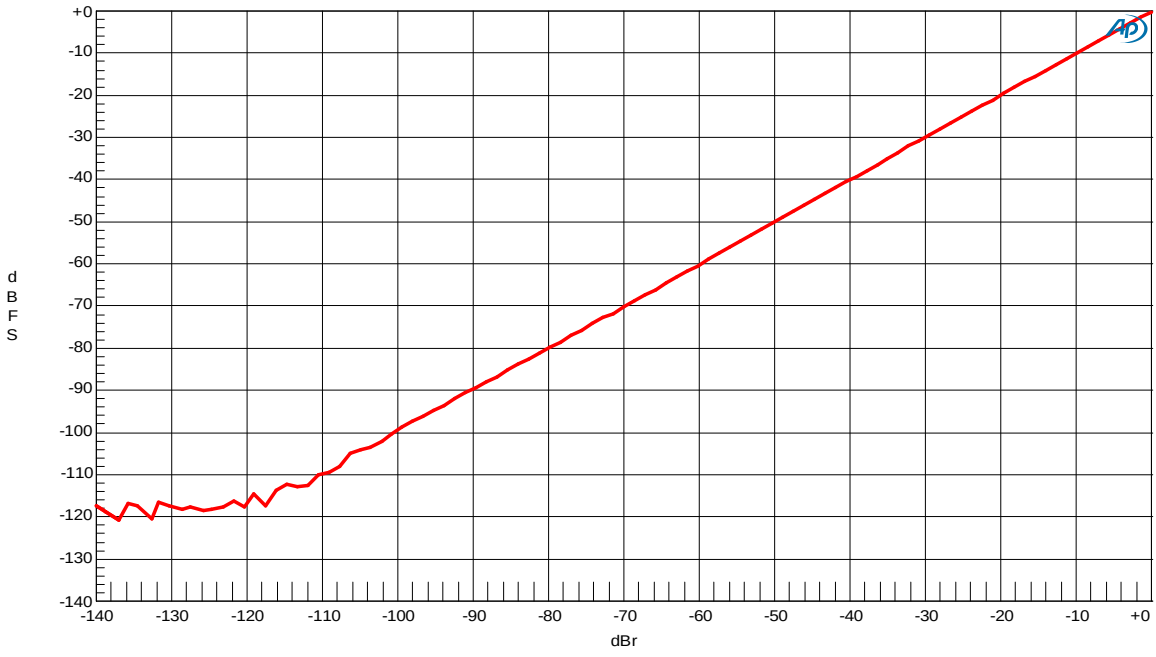



Figure 22. ADC2 – Linearity [fs = 48kHz]

AK4616 Frequency Response Mono ADC(MIC) Single-end
[fs=48kHz, -1dBFS] AMP Bypass

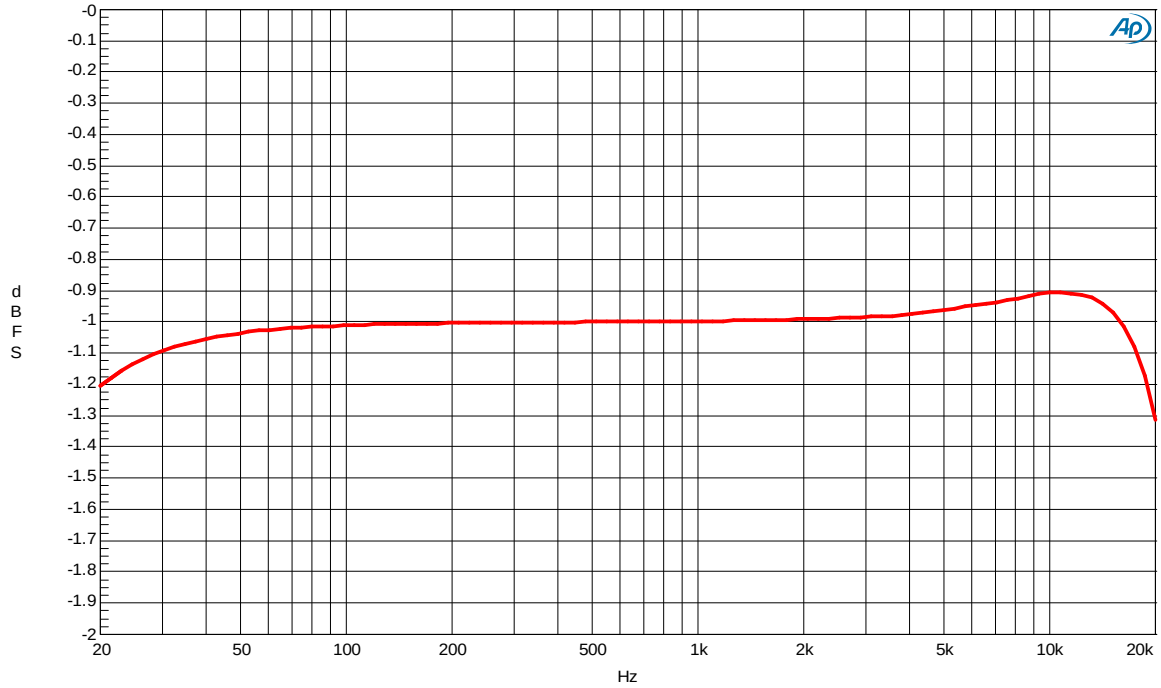



Figure 23. ADC2 – Frequency Response [fs = 48kHz]

3. Mono ADC (fs = 48kHz); MIC (Differential) => Mono ADC => SDTO2

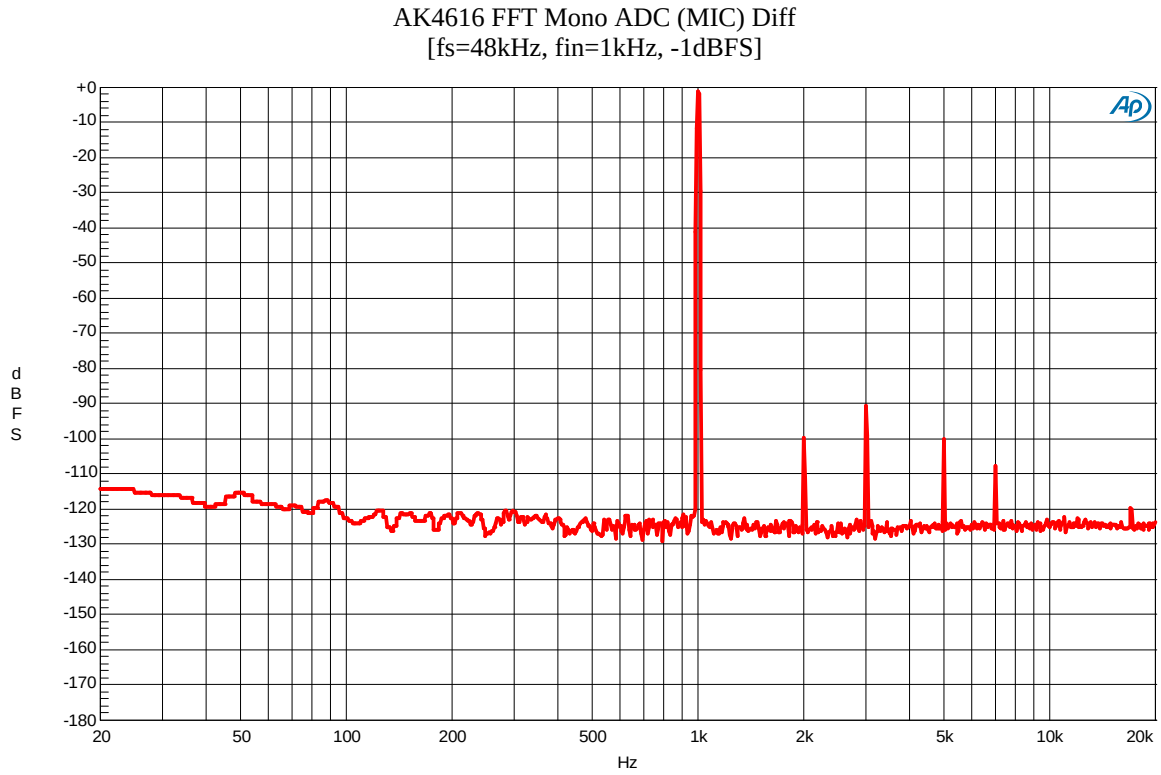



Figure 24. DAC1 – FFT (0BFS) [fs = 48kHz]

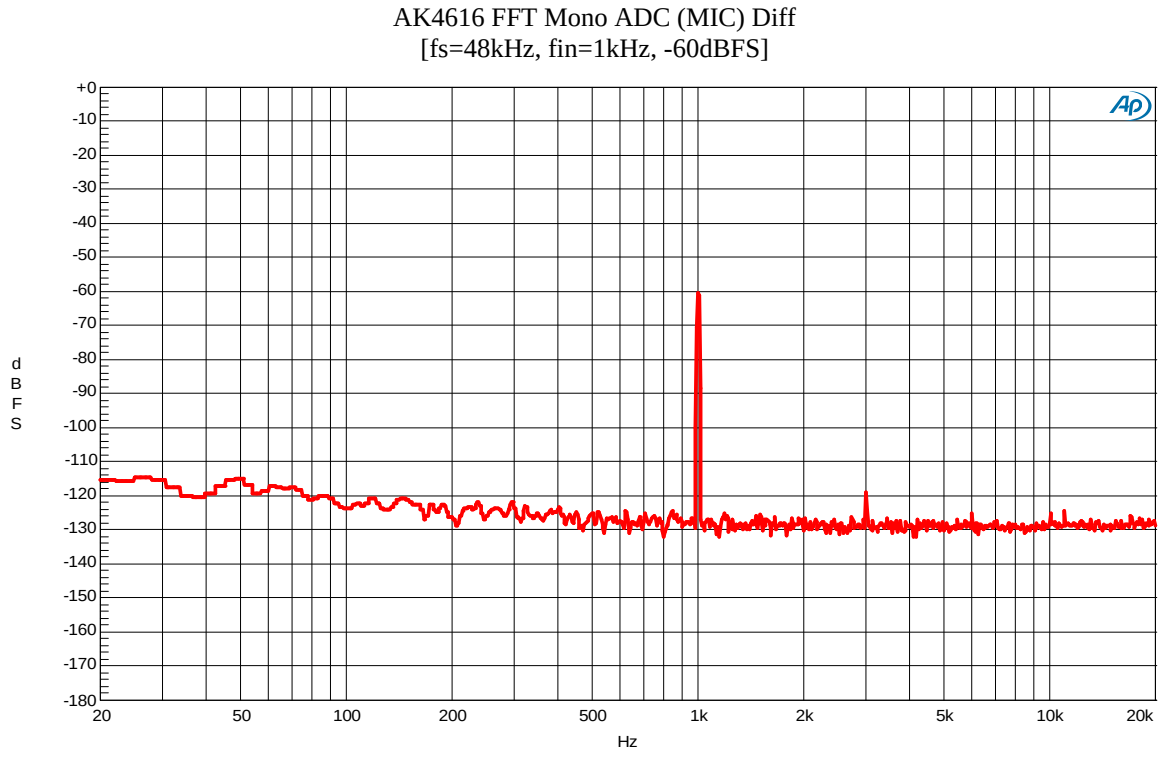



Figure 25. DAC1 – FFT (-60dBFS) [fs = 48kHz]

AK4616 FFT Mono ADC (MIC) Diff
[fs=48kHz, fin=1kHz, no signal]

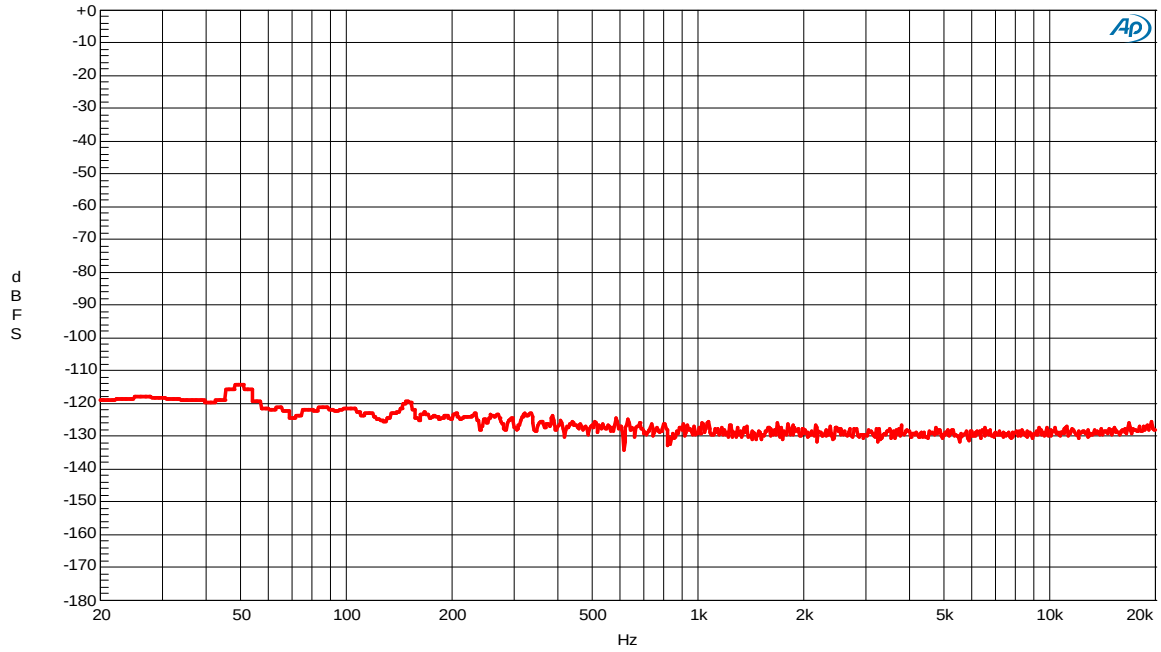



Figure 26. DAC1 – FFT (No Signal) [fs = 48kHz]

AK4616 THD+N vs Amplitude Mono ADC (MIC) Diff
[fs=48kHYz, fin=1kHz]

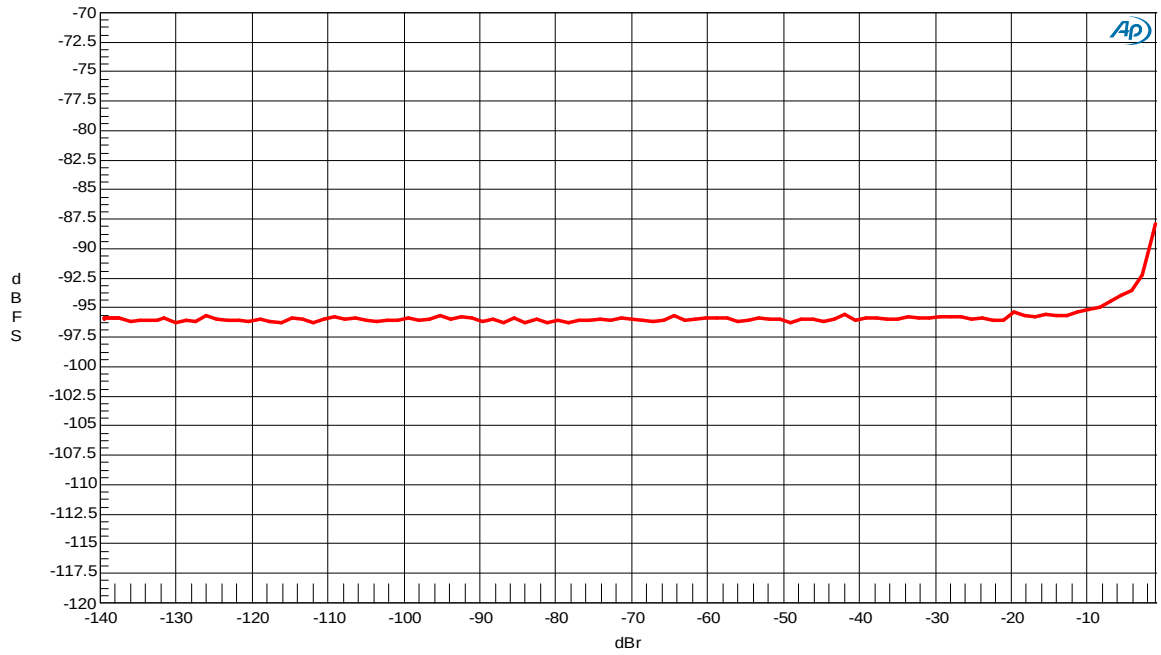



Figure 27. DAC1 – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4616 THD+N vs Input Frequency Mono ADC(MIC) Diff
[fs=48kHz, -1dBFS] AMP bypass

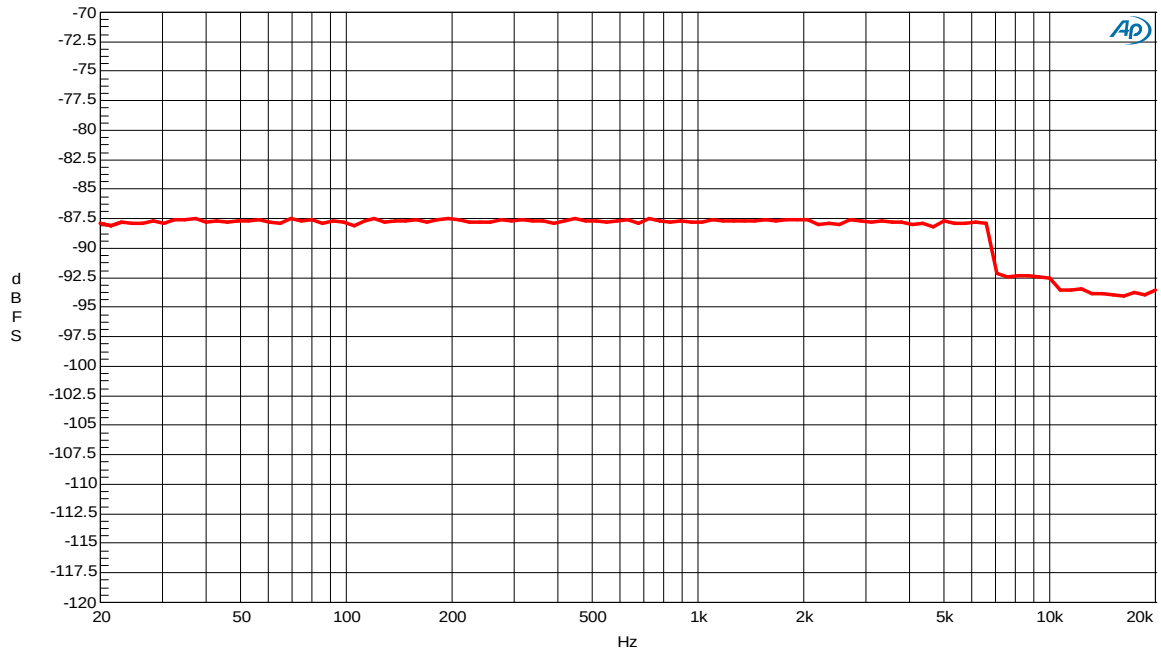



Figure 28. DAC1 – THD+N vs. Input Frequency [fs = 48kHz]

AK4616 Linearity Mono ADC (MIC) Diff
[fs=48kHYz, fin=1kHz]

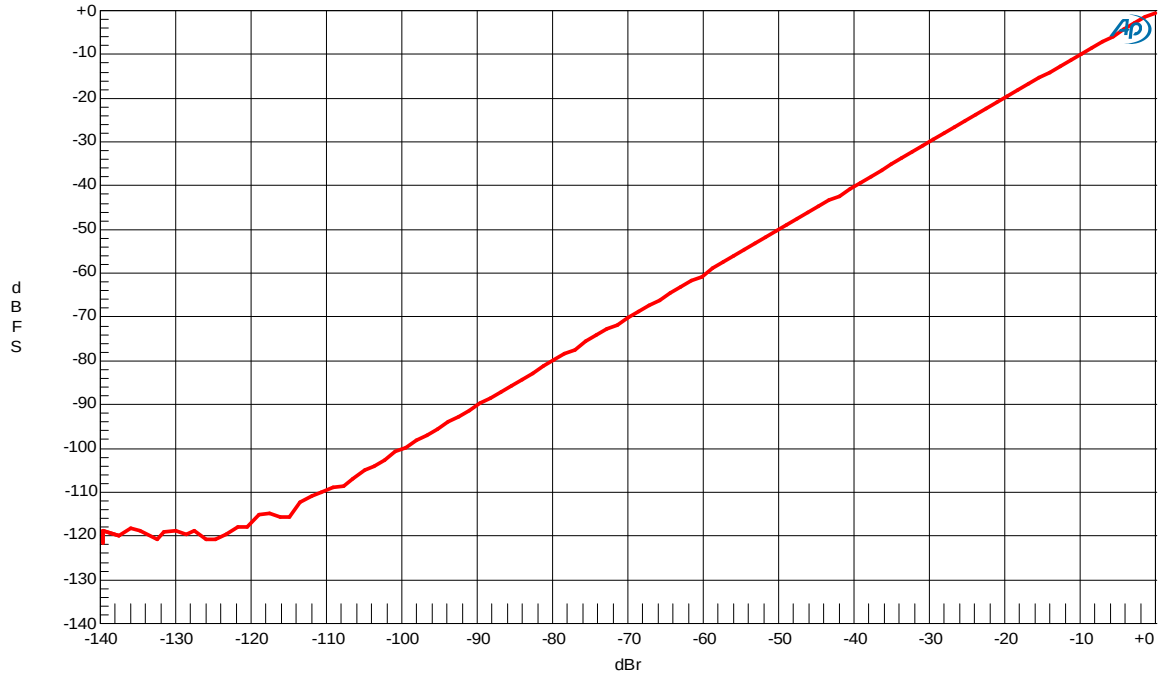



Figure 29. DAC1 – Linearity [fs = 48kHz]

AK4616 Frequency Response Mono ADC(MIC) Diff
[fs=48kHz, -1dBFS] AMP bypass

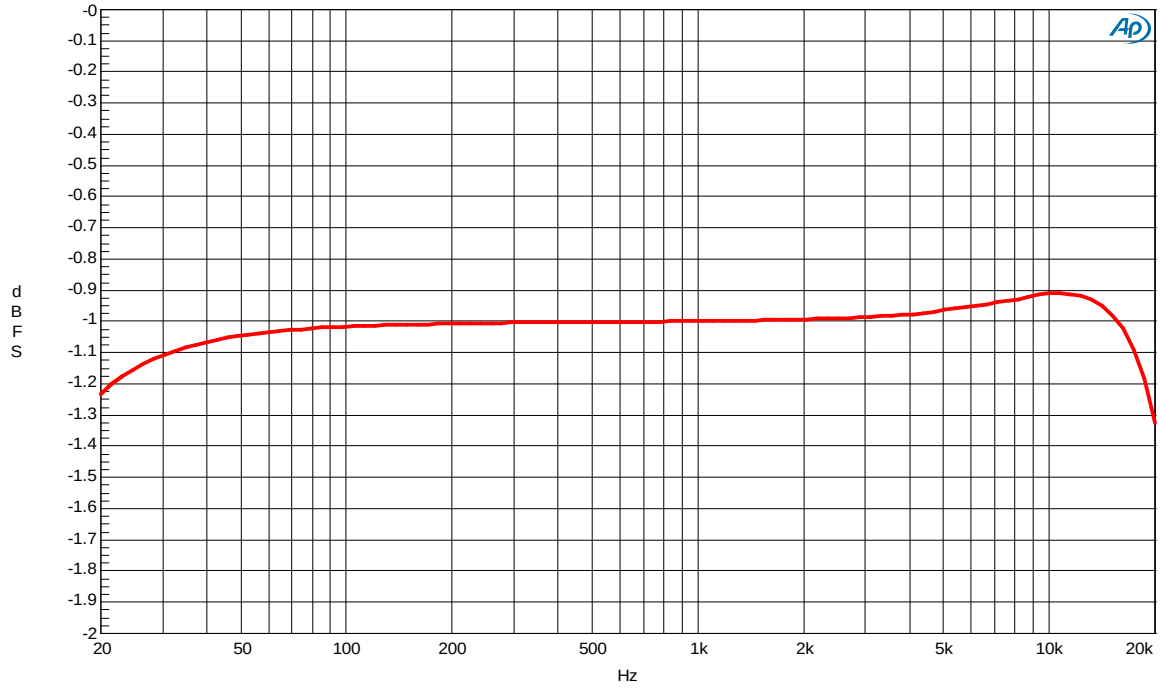



Figure 30. DAC1 – Frequency Response [fs = 48kHz]

4. DAC1 (fs = 48kHz); SDTI1 => DAC1 => AOUT1

AK4616 FFT Single-end DAC (AOUT1L/R)
[fs=48kHz, fin=1kHz, 0dBFS]

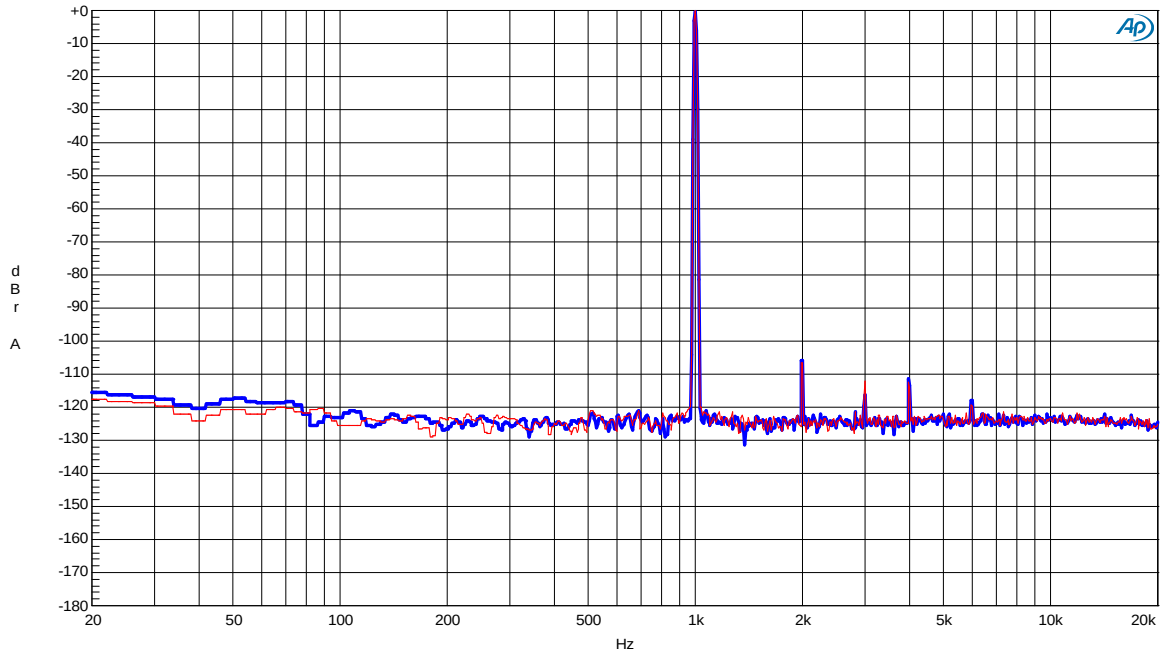



Figure 31. DAC2 – FFT (0BFS) [fs = 48kHz]

AK4616 FFT Single-end DAC (AOUT1L/R)
[fs=48kHz, fin=1kHz, -60dBFS]

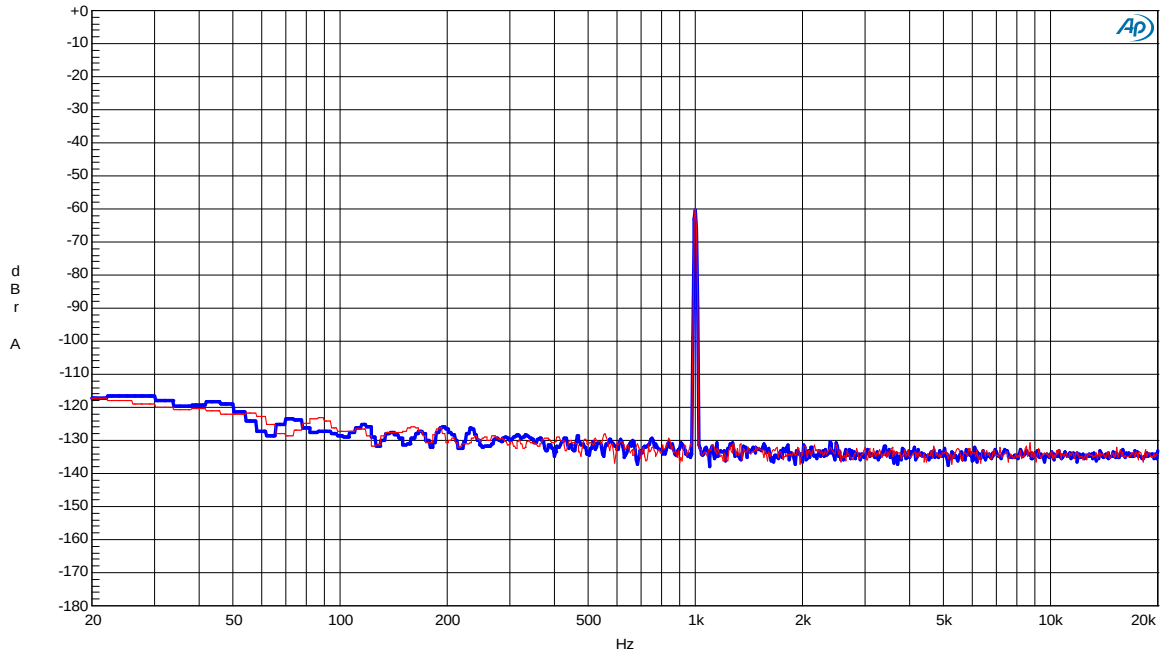



Figure 32. DAC2 – FFT (-60dBFS) [fs = 48kHz]

AK4616 FFT Single-end DAC (AOUT1L/R)
[fs=48kHz, fin=1kHz, no signal]

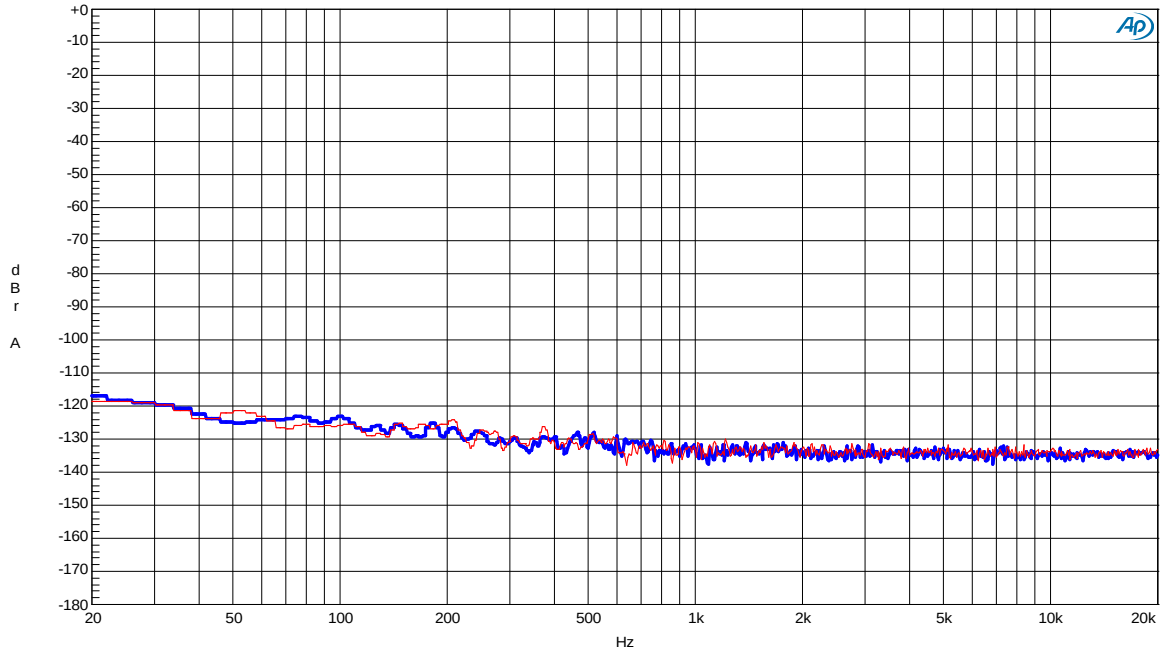



Figure 33. DAC2 – FFT (No Signal) [fs = 48kHz]

AK4616 THD+N vs Amplitude Single-end DAC (AOUT1L/R)
[fs=48kHz, fin=1kHz] 20kHz SPCL

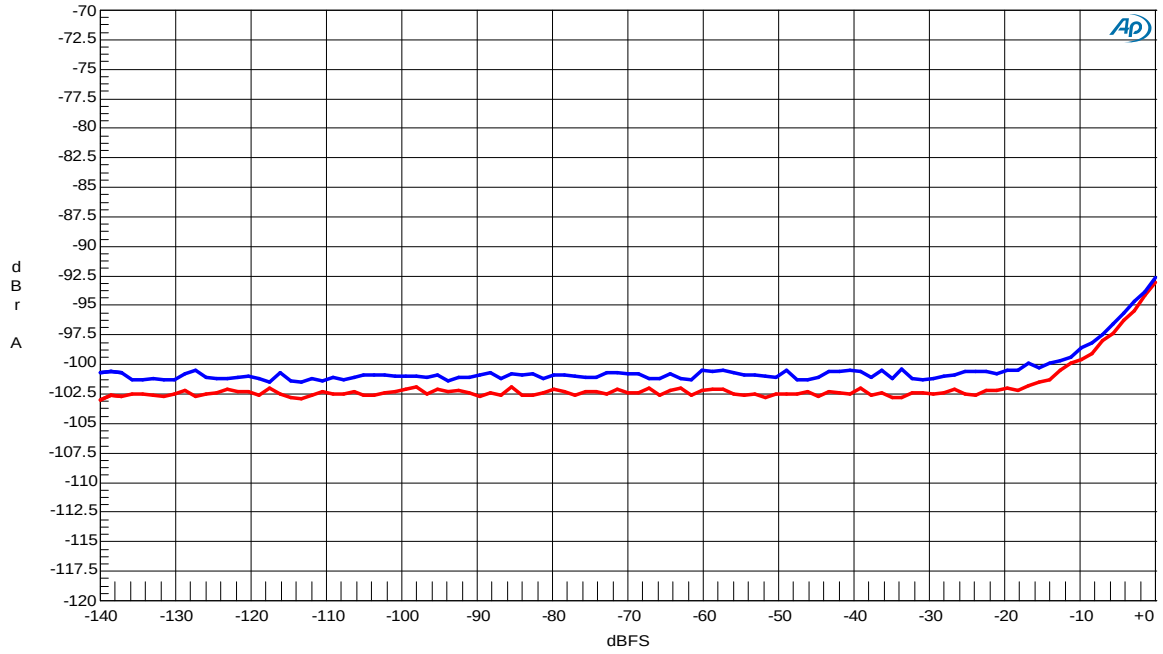



Figure 34. DAC2 – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4616 THD+N vs Input Frequency Single-end DAC (AOUT1L/R)
[fs=48kHz, 0dBFS] 20kHz SPCL

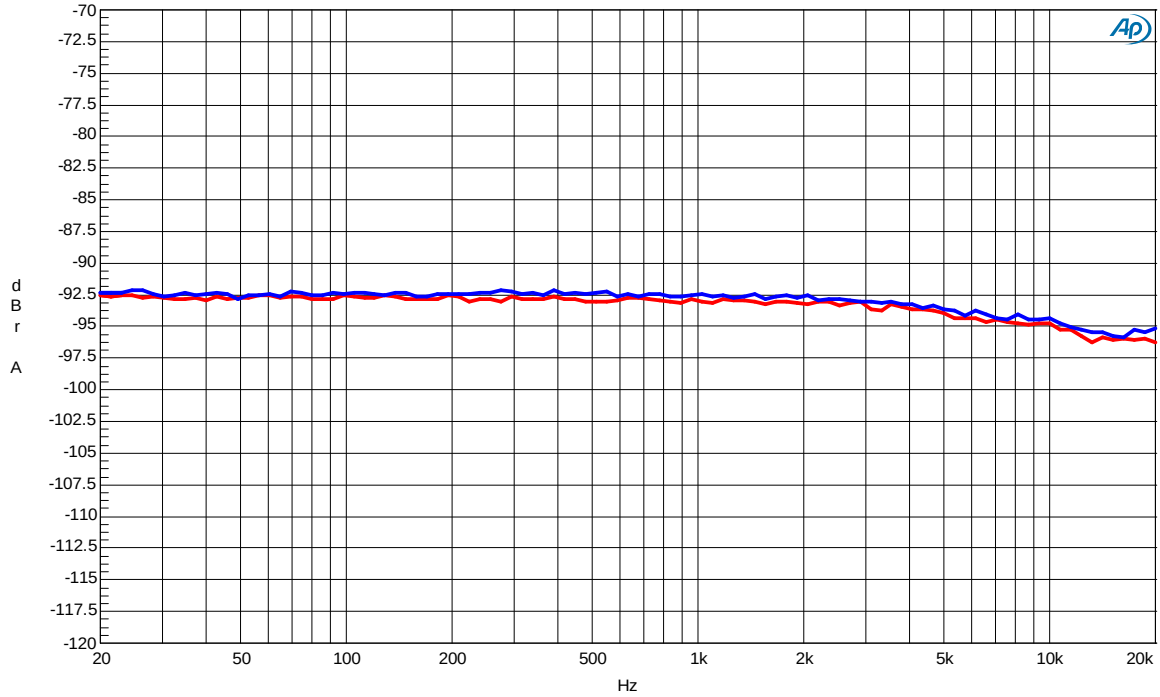



Figure 35. DAC2 – THD+N vs. Input Frequency [fs = 48kHz]

AK4616 Linearity Single-end DAC (AOUT1L/R)
[fs=48kHz,fin=1kHz]

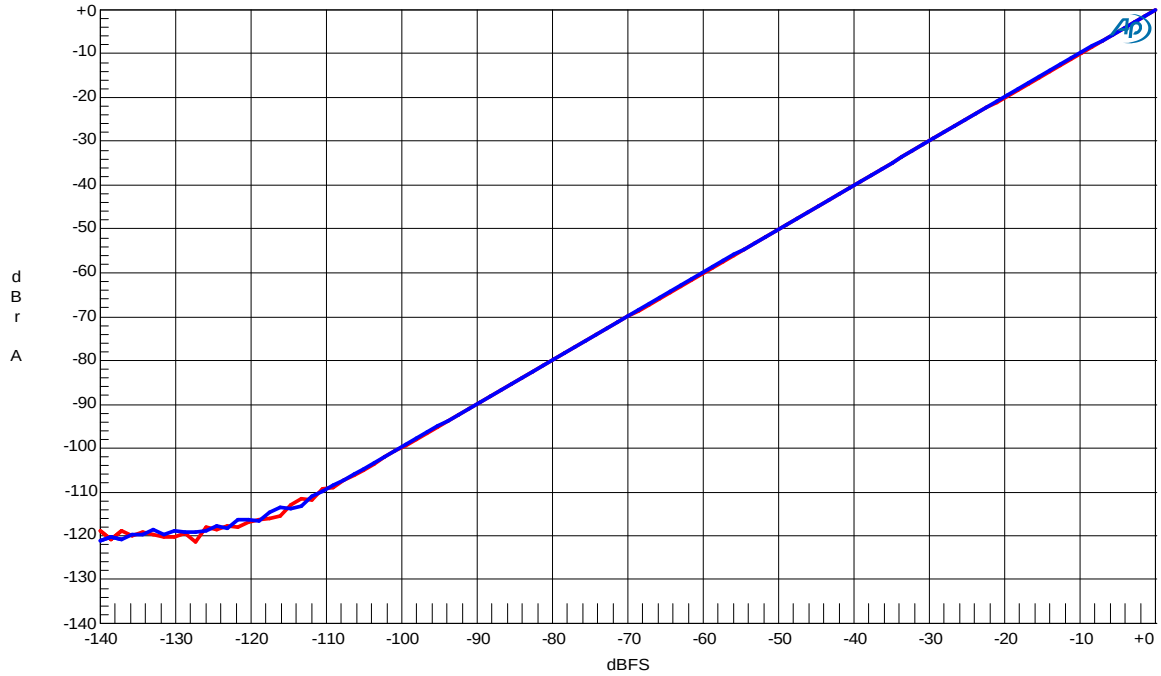



Figure 36. DAC2 – Linearity [fs = 48kHz]

AK4616 Frequency Response Single-end DAC (AOUT1L/R)
[fs=48kHz, 0dBFS]

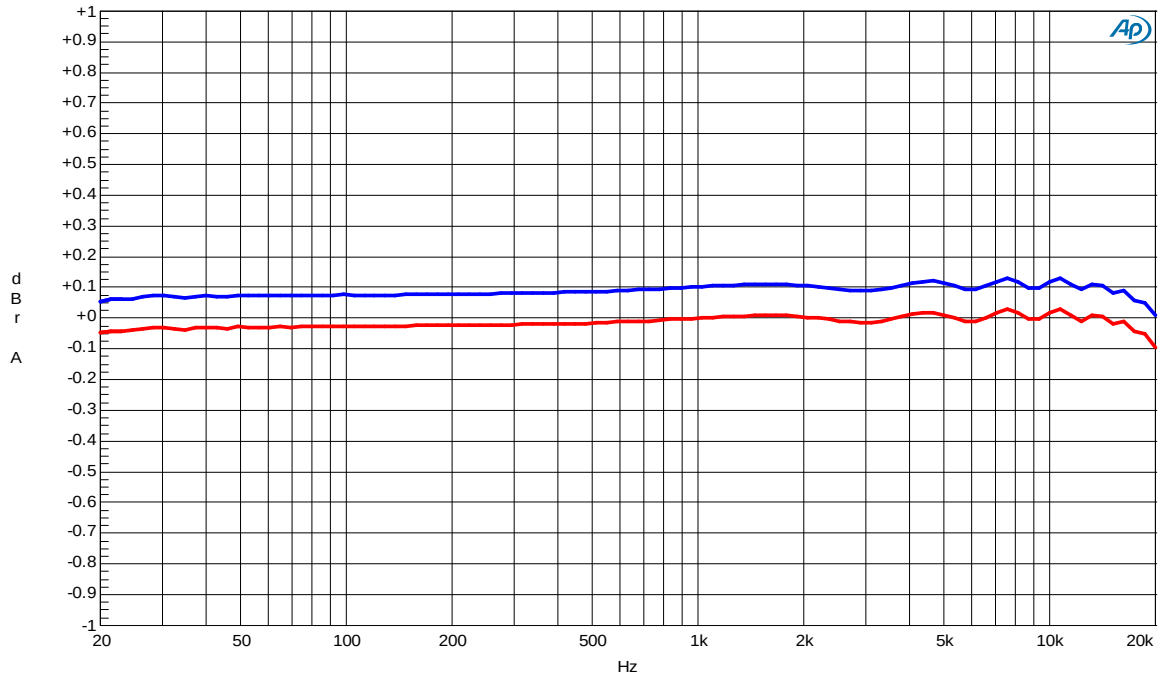



Figure 37. DAC2 – Frequency Response [fs = 48kHz]

AK4616 Crosstalk Single-end DAC (AOUT1L/R)
[fs=48kHz, 0dBFS]

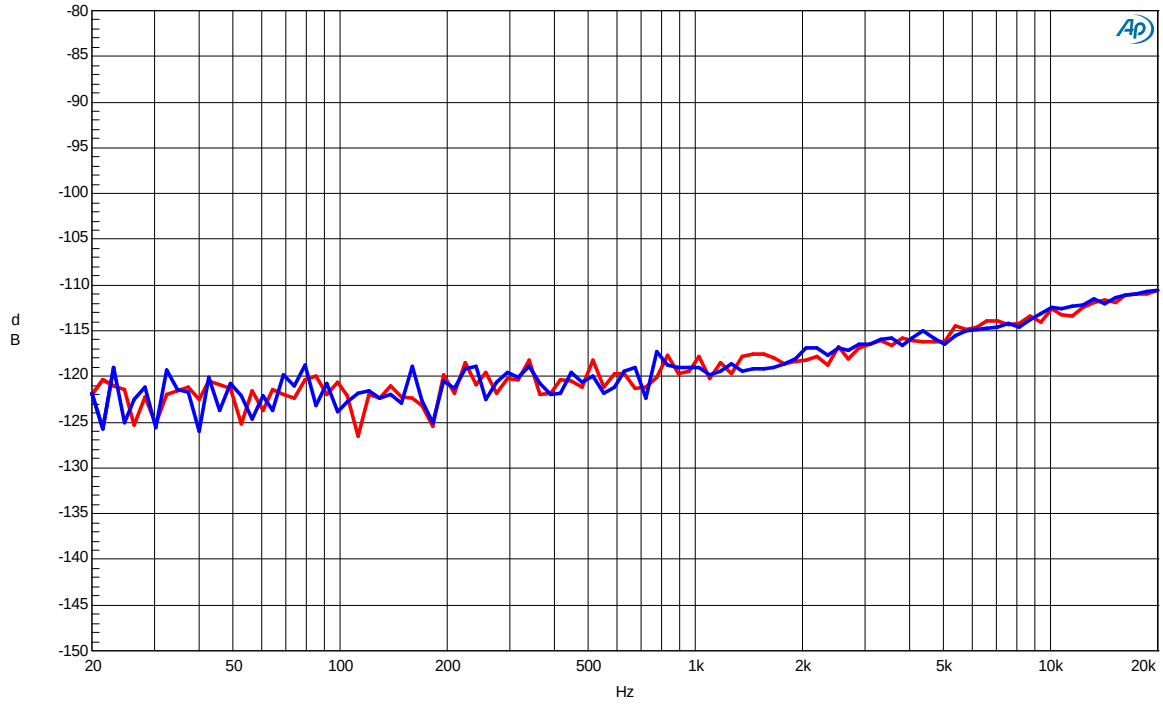



Figure 38. DAC2 – Crosstalk [fs = 48kHz]

5. Mono DAC (fs = 48kHz); SDTI3 => Mono DAC3 => AOUT3

AK4616 FFT Diff DAC (AOUT3)
[fs=48kHz, fin=1kHz, -60dBFS]

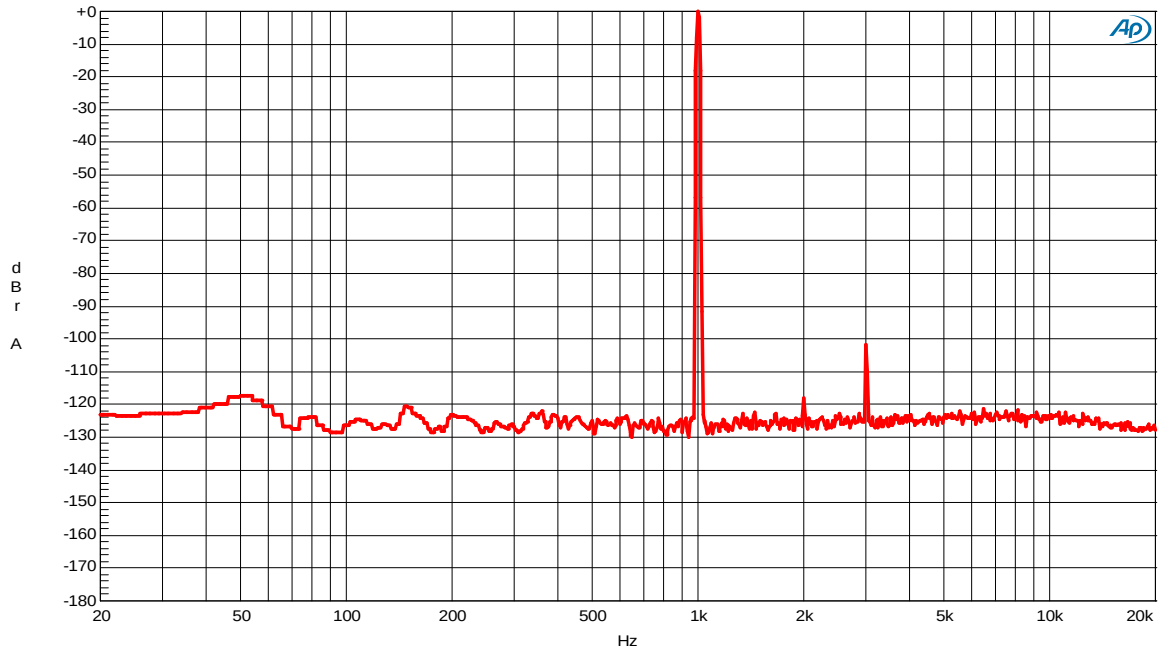



Figure 39. DAC3 – FFT (0BFS) [fs = 48kHz]

AK4616 FFT Diff DAC (AOUT3)
[fs=48kHz, fin=1kHz, -60dBFS]

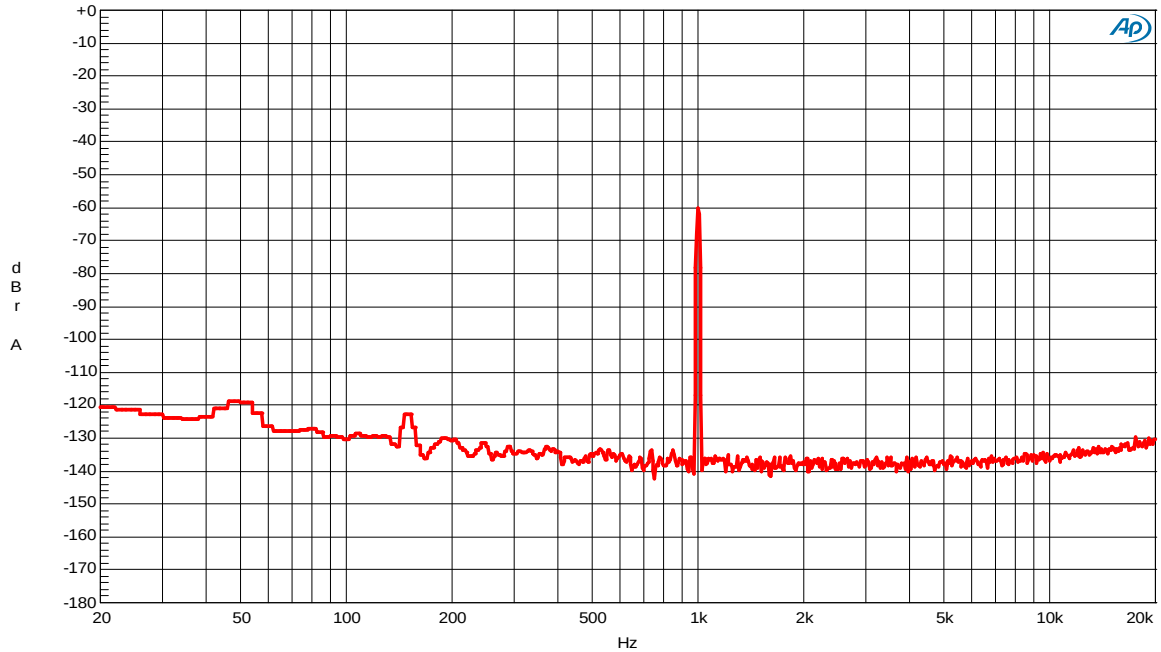



Figure 40. DAC3 – FFT (-60dBFS) [fs = 48kHz]

AK4616 FFT Diff DAC (AOUT3)
[fs=48kHz, fin=1kHz, no signal]

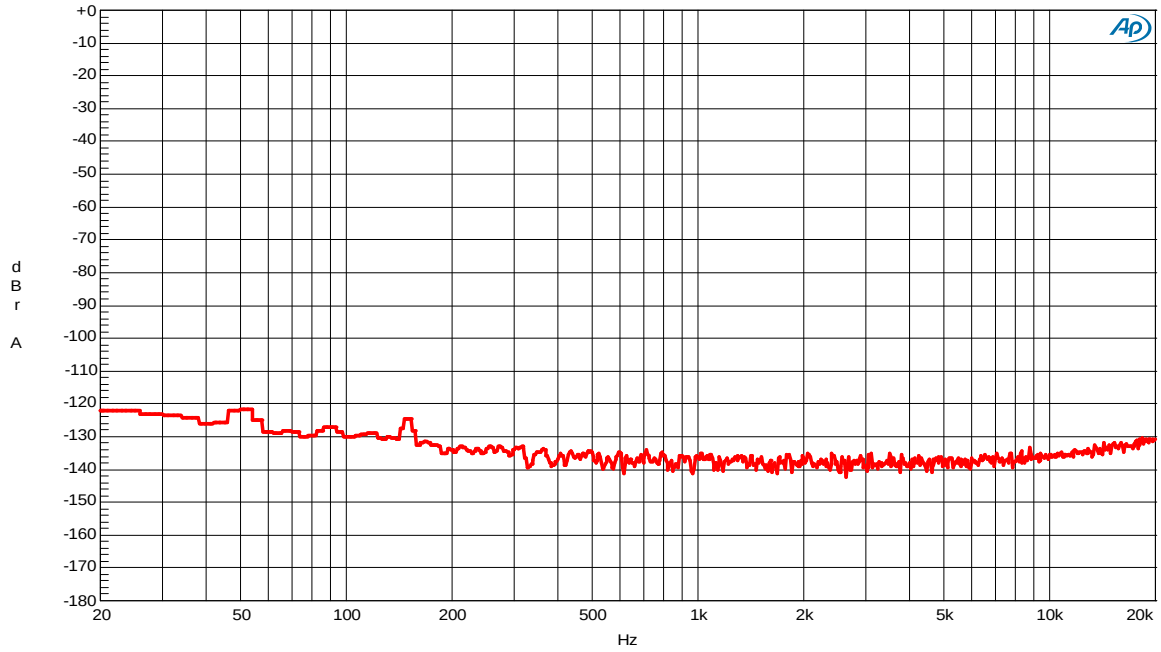



Figure 41. DAC3 – FFT (No Signal) [fs = 48kHz]

AK4616 THD+N vs Amplitude Diff DAC (AOUT3)
[fs=48kHz, fin=1kHz] 20kHz SPCL

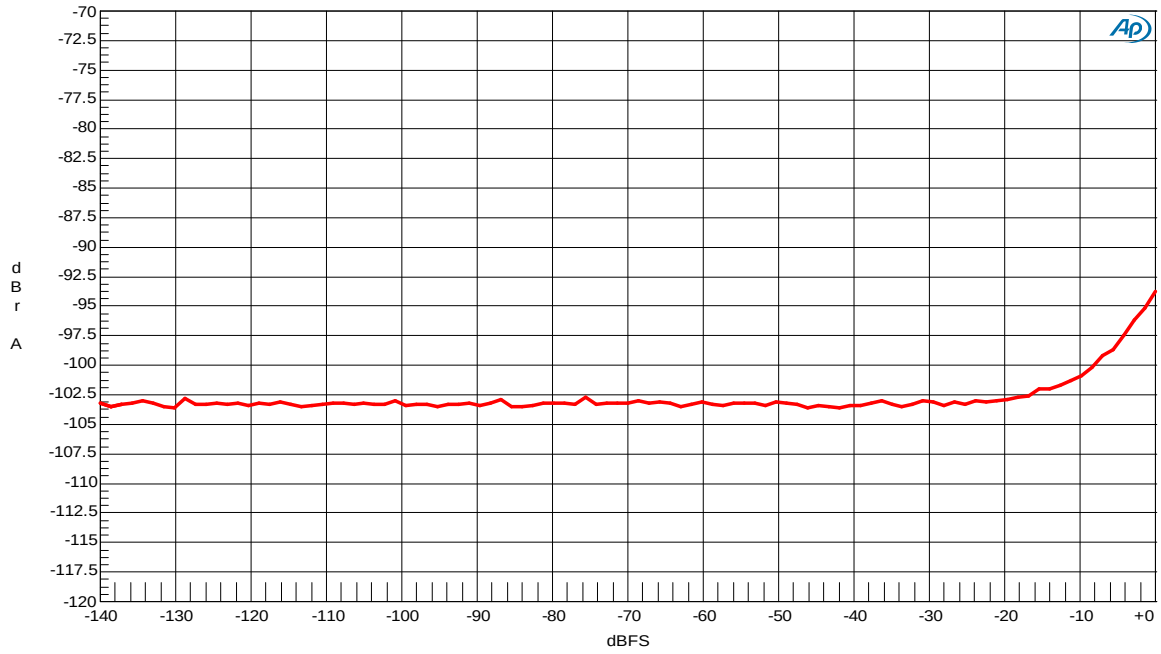



Figure 42. DAC3 – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4616THD+N vs Input Frequency Diff DAC (AOUT3)
[fs=48kHz, 0dBFS] 20kHz SPCL

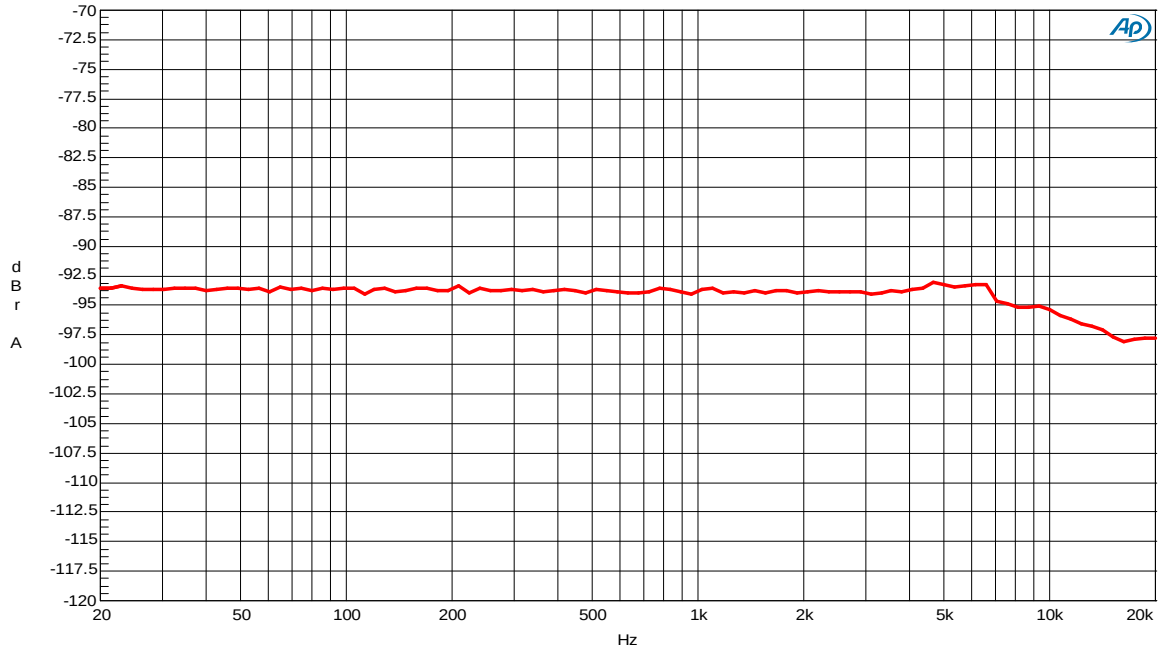



Figure 43. DAC3 – THD+N vs. Input Frequency [fs = 48kHz]

AK4616 Linearity Diff DAC (AOUT3)
[fs=48kHz, fin=1kHz]

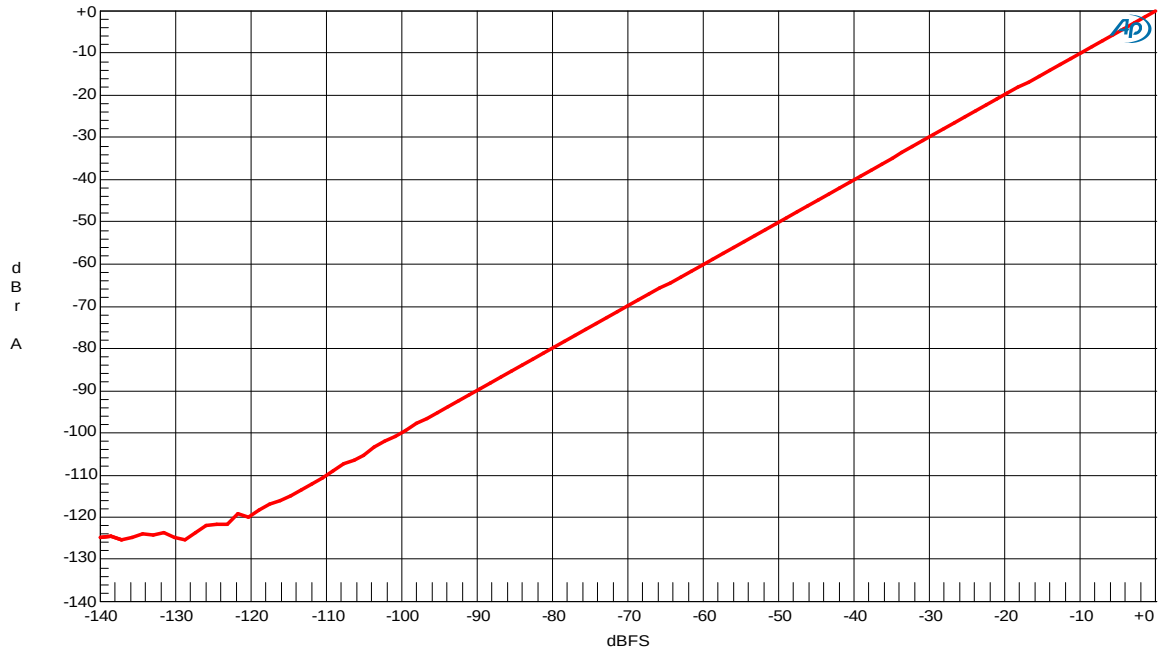



Figure 44. DAC3 – Linearity [fs = 48kHz]

AK4616 Frequency Response Diff DAC (AOUT3)
[fs=48kHz, 0dBFS] AMP Bypass

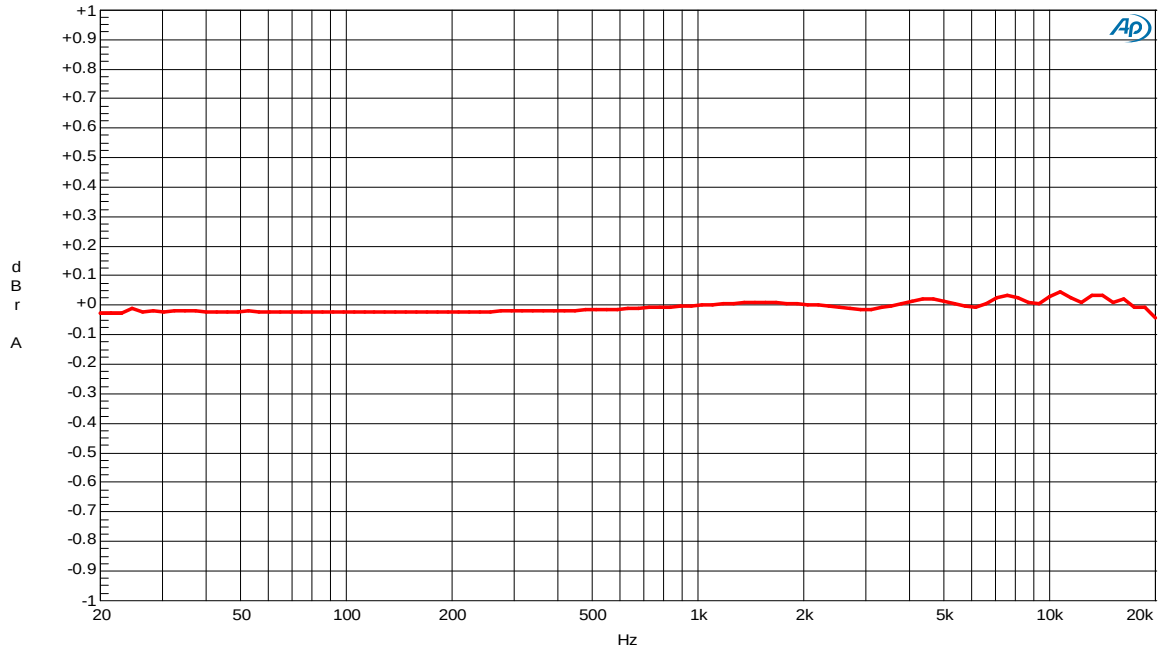
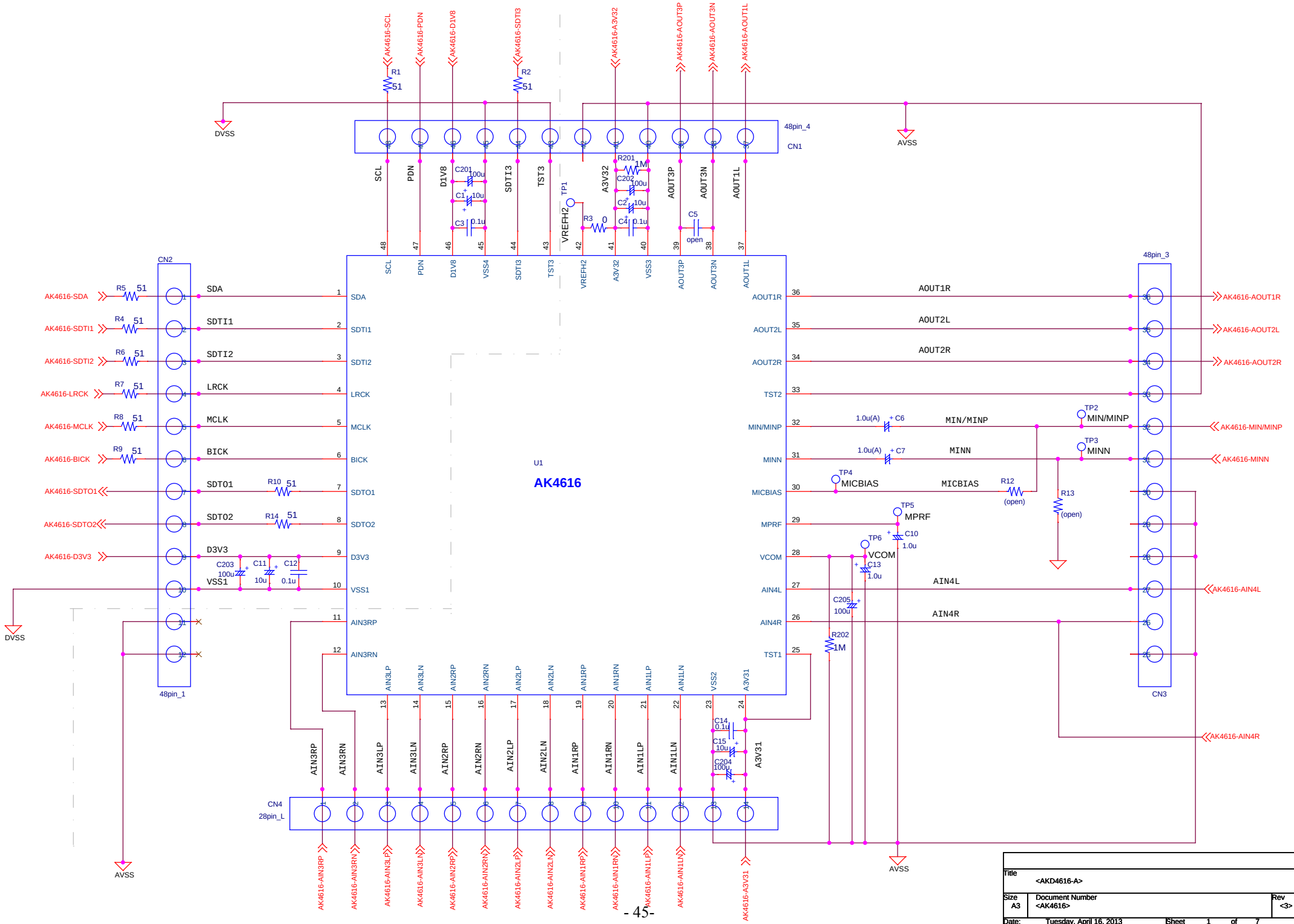



Figure 45. DAC3 – Frequency Response [fs = 48kHz]

## REVISION HISTORY

| Date (yy/mm/dd) | Manual Revision | Board Revision | Reason | Page | Contents |
|---|---|---|---|---|---|
| 12/02/11 | KM110800 | 0 | First edition | | |
| 12/07/12 | KM110801 | 2 | Board Revision | p6,13 | Remove JP6,7 |
| 13/04/16 | KM110802 | 3 | Board Revision | p45 | |
| 13/04/23 | KM110803 | 3 | Soft Revision | | Control Software Manual Revision |

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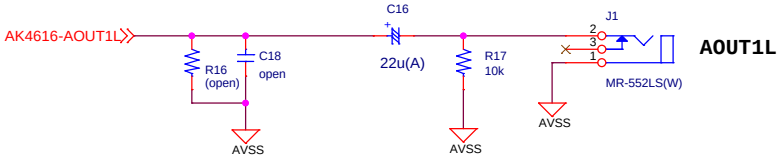
## AOUT1L

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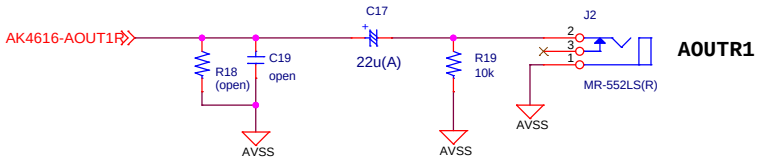


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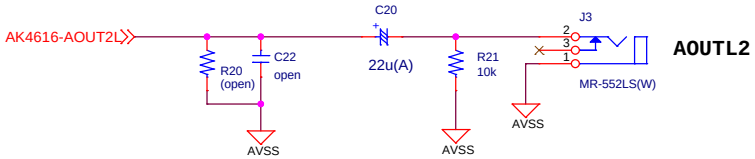


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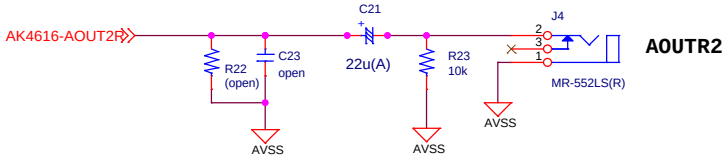
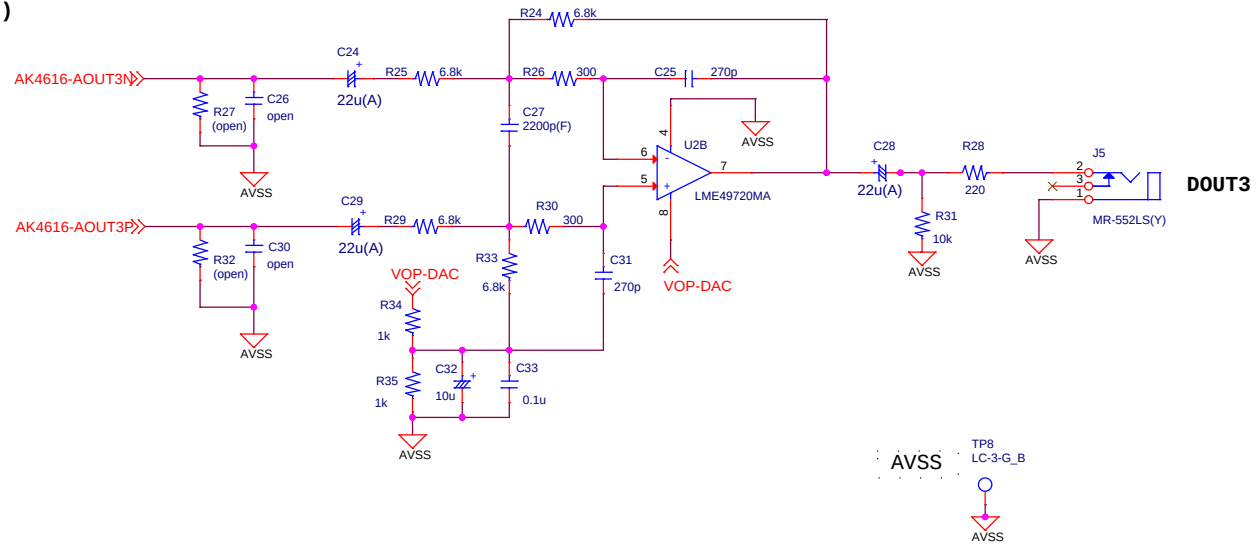



## AOUT3 (Monaural)







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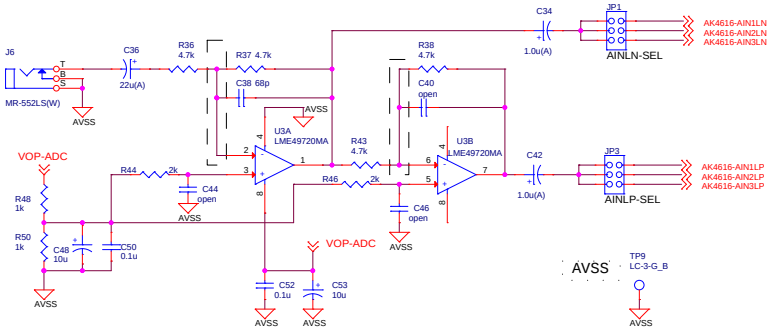
AREA: SHORTEST WIRING

**AINL**

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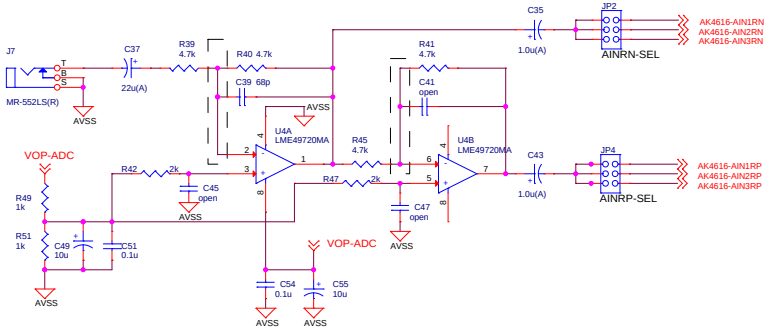


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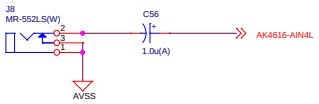


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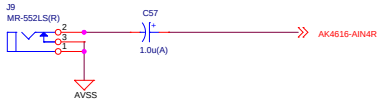


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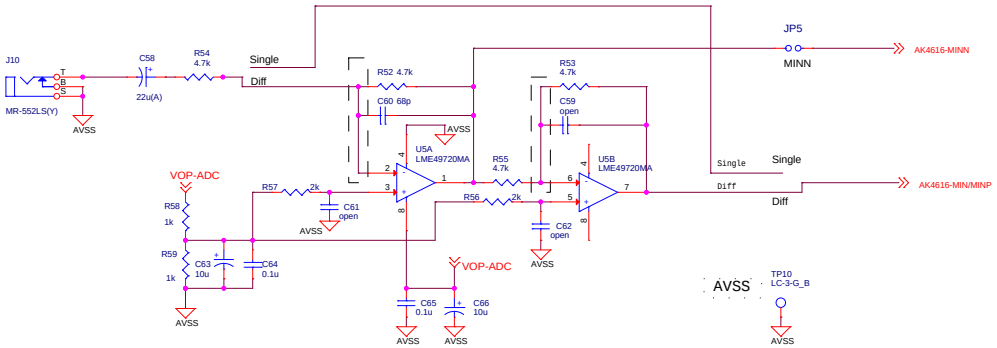




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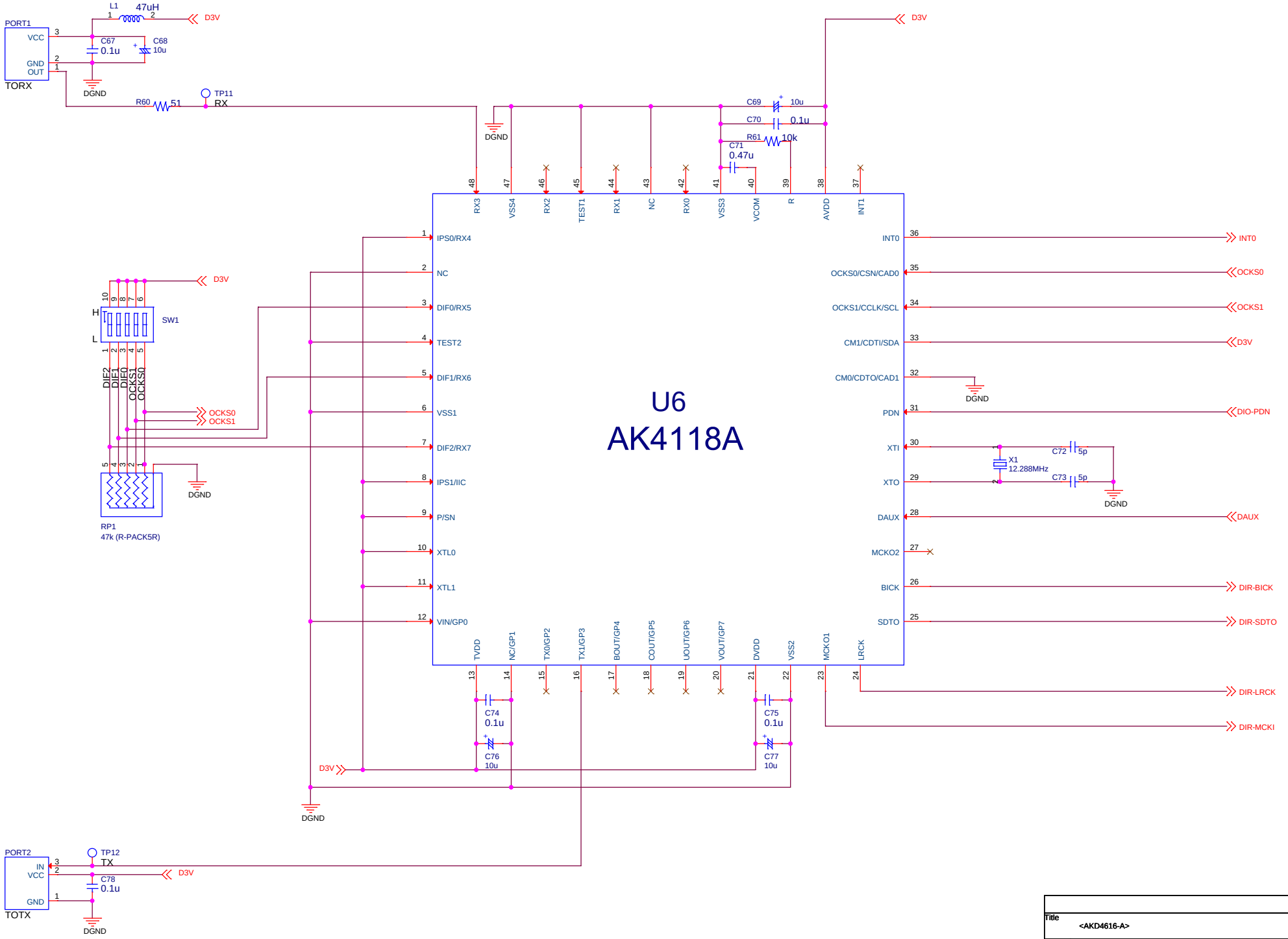


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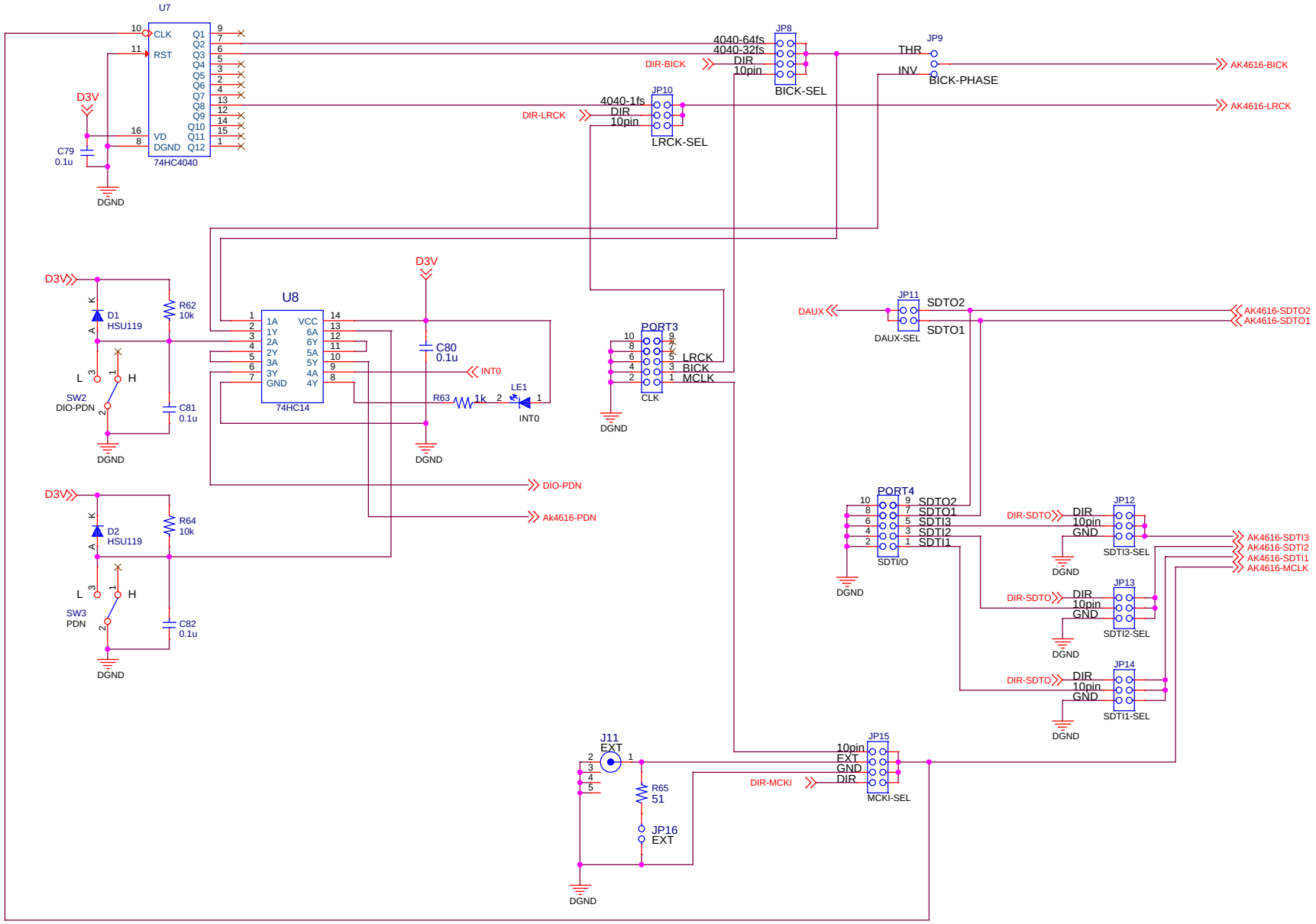




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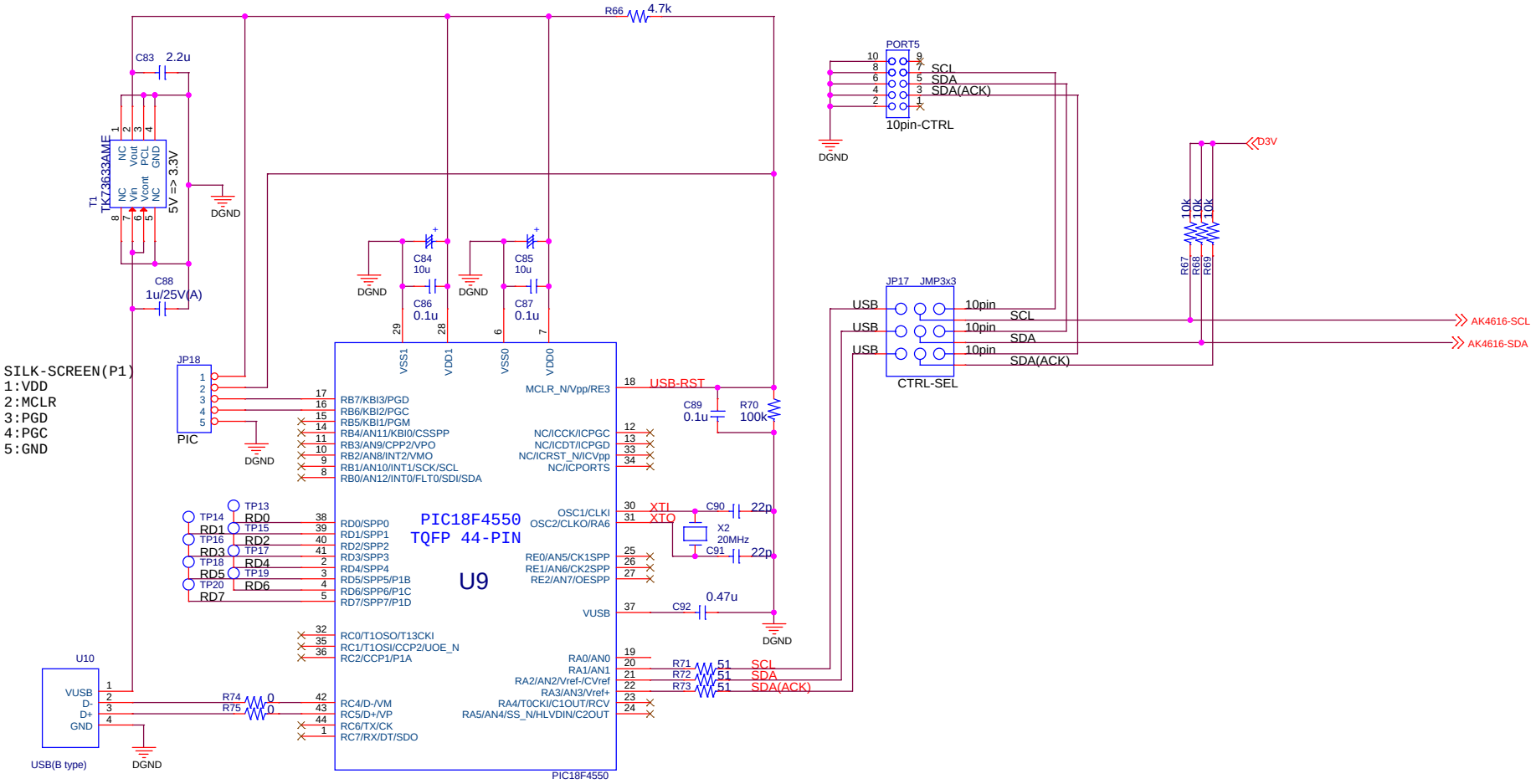




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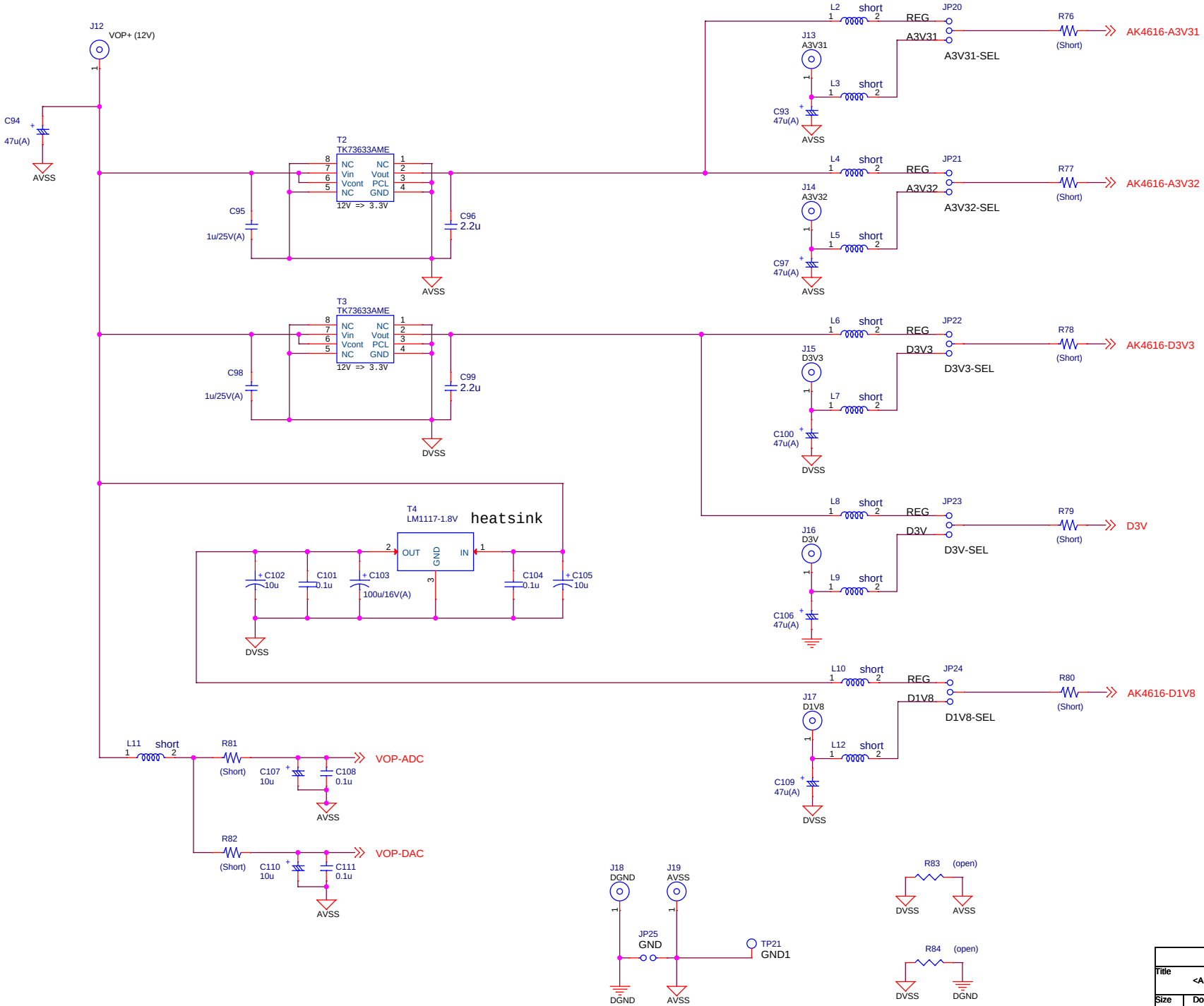


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