

**Data Sheet AS1360** 

## 1.5µA Low-Power, Positive Voltage Regulator

## 1 General Description

The AS1360 low-power, positive voltage regulator was designed to deliver up to 250mA while consuming only 1.5µA of quiescent current. The device is available in fixed output voltages of 1.8, 2.1, 2.5, 3.0, 3.3, and 5.0V.

The device features integrated short-circuit and overcurrent protection.

The wide input voltage range, low-dropout voltage, and high-accuracy output voltage makes the device perfectly suited for 2- and 3-cell battery-powered and portable applications.

The low dropout voltage (650mV) prolongs battery life and allows high current in small applications when operated with minimum input-to-output voltage differentials.

The device features very stable output voltage (using only 1µF tantalum or aluminum-electrolytic capacitors), strict output voltage regulation tolerances (±0.5%), and excellent line-regulation.

The AS1360 is available in a 3-pin SOT23 package.

## 2 Key Features

Low Quiescent Current: 1.5µA

Input Voltage Range: Up to 20V

Low Dropout Voltage

- 250mV @ 100mA

- 400mV @ 200mA

Fixed Output Voltages: 1.8, 2.1, 2.5, 3.0, 3.3, 5.0V

High Output Current: 250mA (Vout = 5.0V)

High-Accuracy Output Voltage: ±1.5%

Exceptional Line Regulation: 0.1%/V

Low Temperature Drift: ±100ppm/°C

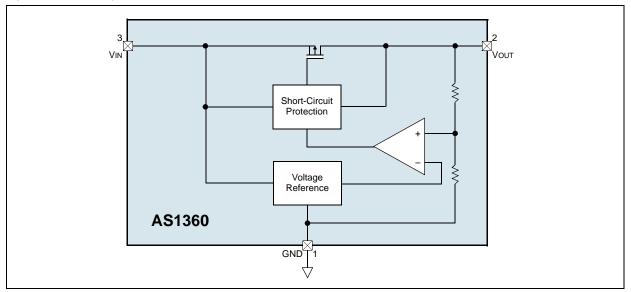
Integrated Short-Circuit and Overcurrent Protection

3-pin SOT23 Package

## 3 Applications

The device is ideal for mobile phones, PDAs, digital cameras, smart battery packs, battery-powered alarms, solar-powered instruments, intelligent instruments, CO2 and smoke detectors, CPU power supplies, and any battery-powered application.



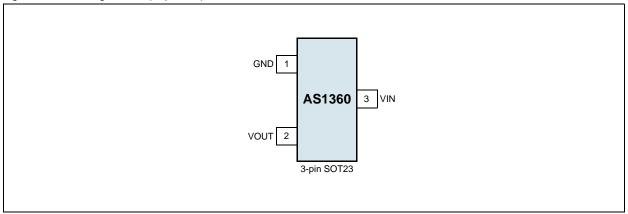




# 4 Pinout and Packaging

## **Pin Assignments**

Figure 2. Pin Assignments (Top View)



## **Pin Descriptions**

Table 1. Pin Descriptions

Pin Number	Pin Name	Description	
1	GND	<b>Ground</b> . This pin should be connected to the negative side of the output and the negative terminal of the input capacitor. No high-current flows out of this pin, only bias current (1.5μA, typ).	
		<b>Note:</b> Voltage drops between this pin and the negative side of the load should be minimized.	
2 VOUT		<b>Regulated Output Voltage</b> . This pin should be connected to the positive side of the load and the positive terminal of the output capacitor. Current flowing out of this pin is equivalent DC load current.	
		<b>Note:</b> The positive side of the output capacitor should be mounted as close as is practical to this pin.	
3	VIN	<b>Unregulated Input Voltage</b> . This pin should be connected to the positive terminal of the input capacitor.	
3		<b>Note:</b> The input capacitor should be mounted as close as is practical to this pin.	



# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Input Voltage		+30	V	
Continuous Output Current		PD/ (VIN - VOUT)	mA	
Peak Output Current		500	mA	
Output Voltage	- 0.3V	VIN + 0.3V or +7V	V	Minimum of the two values
Thermal Resistance @JA		230	°C/W	Typical FR4, 4-layer application
Operating Temperature Range	-40	+85	°C	
Storage Temperature Range	-40	+125	°C	
Electrostatic Discharge (ESD) Protection Level	1		kV	HBM - Norm: MIL 883 E methode 3015
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in compliance with IPC/JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".



## **6 Electrical Characteristics**

TAMB = +25°C (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Unit
VIN	Input Voltage				20	V
Vouт	Output Voltage	IOUT = 40mA <sup>1</sup> , IOUT = 15mA if VOUT = 1.8V	Vоитном - 1.5%	VOUTNOM ± 0.5%	VOUTNOM + 1.5%	٧
		VOUT = 5.0V (VIN = VOUTNOM + 1.0V)	250			mA
		Vout = 3.3V	150			
IOUT(MAX)	Maximum Output Current	Vout = 3.0V	150			
	Current	VOUT = 2.5V	125			
		Vout = 2.1V	115			
		Vout = 1.8V	110			
	Load Regulation <sup>2</sup>	$Vout = 5.0V$ , $1mA \le Iout \le 100mA$	-1.60	±0.8	+1.60	%
		Vout = 3.3V, $1mA \le Iout \le 80mA$	-2.72	±1.3	+2.72	
ΔVουτ/Vουτ		Vout = 3.0V, $1mA \le Iout \le 80mA$	-3.00	±1.5	+3.00	
Δνοσί/νοσί		Vout = 2.5V, $1mA \le Iout \le 60mA$	-3.60	±1.8	+3.60	
		Vout = 2.1V, $1mA \le Iout \le 40mA$	-2.60	±1.6	+2.60	
		Vout = 1.8V, $1mA \le Iout \le 30mA$	-1.60	±0.8	+1.60	
$\Delta V$ OUT x 100/ $\Delta V$ IN x $V$ OUT	Line Regulation	IOUT = $40$ mA, (VOUTNOM +1.0) $\leq$ VIN $\leq$ 10.0V		0.1	0.25	%/V
	Dropout Voltage	IOUT = 200mA, $VOUTNOM = 5.0V$		400	630	mV
		IOUT = 160mA, $VOUTNOM = 3.3V$		400	700	
VIN - VOUT		IOUT = 160mA, $VOUTNOM = 3.0V$		400	700	
		IOUT = 120mA, $VOUTNOM = 2.5V$		400	700	
		IOUT = 60mA, $VOUTNOM = 2.1V$		200	500	
		IOUT = 20mA, $VOUTNOM = 1.8V$		180	300	
IQ	Input Quiescent Current	VIN = VOUTNOM + 1.0V		1.5	3.0	μA
ТСVоит	Temperature Coefficient of Vout <sup>3</sup>	$\begin{array}{l} \text{IOUT} = 40\text{mA}, \\ \text{-}40^{\text{o}}\text{C} \leq \text{TAMB} \leq +85^{\text{o}}\text{C} \end{array}$		±100		ppm/ °C
tR	Output Rise Time	10% Voutnom to 90% Voutnom, Vin = 0V to Voutnom + 1V, RLOAD = $25\Omega$ resistive		150		μs

- 1. VOUTNOM is the nominal device output voltage.
- 2. Measured at a constant junction temperature using low duty cycle pulse testing.
- 3. TCVout = (VoH VoL) x 10<sup>6</sup>/(Voutnom x Temperature). Where:

Voh is the highest voltage measured over the device temperature range.

Vol is the lowest voltage over the device temperature range.



# 7 Typical Operating Characteristics

VOUT = 3.3V,  $ILOAD = 100\mu A$ , VIN = 4.3V,  $CIN 1\mu F$  (tantalum),  $COUT = 1\mu F$  (tantalum),  $TAMB = +25^{\circ}C$  (unless otherwise specified).

Figure 3. Supply Current vs. Input Voltage;

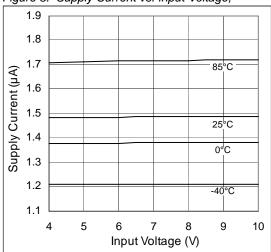


Figure 5. Supply Current vs. Temperature;

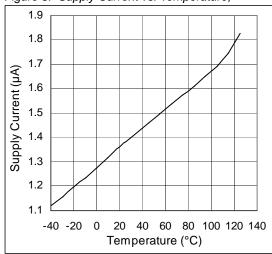


Figure 7. Output Voltage vs. Load Current,

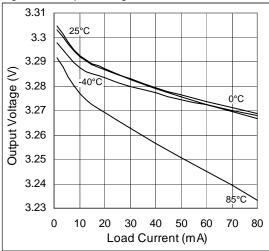


Figure 4. Supply Current vs. Load Current;

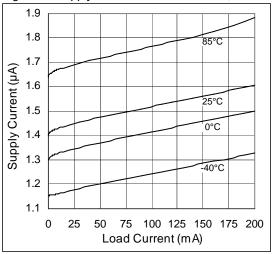


Figure 6. Output Voltage vs. Input Voltage;

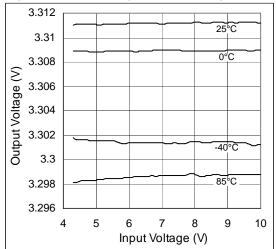


Figure 8. Dropout Voltage vs. Load Current;

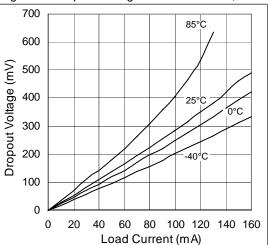


Figure 9. Load Regulation vs. Temperature,

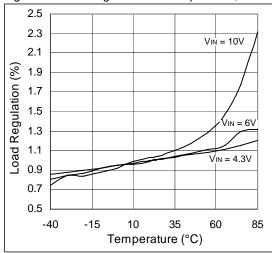


Figure 10. Line Regulation vs. Temperature;

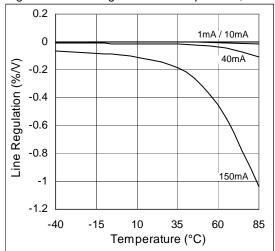


Figure 11. Startup Rise Time;

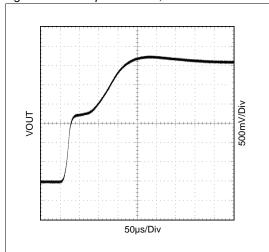
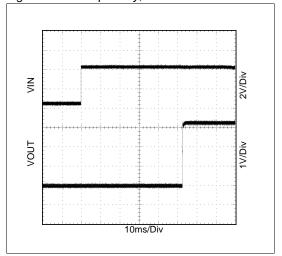


Figure 12. Startup Delay;



**Note:** All graphs where measured without additional heat sinks, with the SOT23 package mounted on a 4-layer PCB. Adding additional heat sinks will improve performance in high temperature environment.



## 8 Detailed Description

The AS1360 is a low-power, positive voltage regulator designed in such a way that the supply current is independent from the load current. The device regulates the output by comparing the output voltage to an internally generated reference voltage.

The device is available in fixed output voltages of 1.8, 2.5, 3.0, 3.3, and 5.0V. Fixed output voltages are generated using the internal resistor divider network (see Figure 1 on page 1).

### **Short Circuit/Overcurrent Protection**

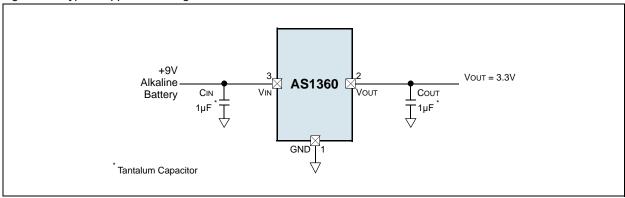
The AS1360 monitors current flow through the p-channel MOSFET. In short-circuit or overcurrent conditions, the integrated short-circuit protection circuitry will limit output current.

Note: Thermal Dissipation according to Absolute Maximum Ratings on page 3 must be considered.



# 9 Application Information

Figure 13. Typical Application Diagram



### **Power Dissipation**

Power dissipation (PD) of the AS1360 is the sum of the power dissipated by the p-channel MOSFET and the quiescent current required to bias the internal voltage reference and the internal power amplifier, and is calculated as:

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD$$
 (Bias) = VINIGND (EQ 2)

Total AS1360 power dissipation is calculated as:

$$PD(Total) = PD(P-Channel MOSFET) + PD(Bias)$$
 (EQ 3)

The internal quiescent bias current ( $2\mu A$ , typ) is such that the PD(Bias) term of (EQ 3) can be disregarded and the maximum power dissipation can be estimated using VIN(MAX) and VOUT(MIN) to obtain a maximum voltage differential between VIN and VOUT, and multiplying the maximum voltage differential by the maximum output current:

$$PD = (VIN(MAX)VOUT(MIN))IOUT(MAX)$$
 (EQ 4)

#### Where:

VIN = 3.3 to 4.1V VOUT = 3.0V  $\pm 2\%$ IOUT = 1 to 100mA TAMB(MAX) = 55°C

 $PMAX = (4.1V - (3.0V \times 0.98)) \times 100mA = 116.0mW$ 

### **Junction Temperature**

The AS1360 junction temperature (T<sub>J</sub>) can be determined by first calculating the thermal resistance from junction temperature-to-ambient temperature.

**Note:** Thermal resistance is estimated to be the junction temperature-to-air temperature RΦJA, and is approximately 230°C/W or 335°C/W (when mounted on 1 square inch of copper). RΦJA will vary depending on PCB layout, air-flow and application specific conditions.

The AS1360 junction temperature is determined by calculating the rise in TJ above TAMB, and then adding the increase of TAMB:

$$T_J = P_{D(MAX)} \times R_{\Phi JA} + T_{AMB}$$
 (EQ 5)

From (EQ 5), the value of T<sub>J</sub> can be calculated as:

 $T_J = 116.0 \text{mW} \times 230^{\circ}\text{C/W} + 55^{\circ}\text{C}$ 

Therefore:

 $T_J = 81.68^{\circ}C$ 



### **External Component Selection**

### **Input Capacitor**

In applications where input impedance is approximately  $10\Omega$ , a  $1\mu F$  capacitor is sufficient for CIN (see Figure 13 on page 8).

In cases where the AS1360 is operated from a battery, or when there is significant distance between the input source to the AS1360, larger values for CIN may be required for output stability.

Note: For values of Cout > 1µF, the value of Cin should be increased to prevent high source-impedance oscillations.

### **Output Capacitor**

In most applications for the AS1360, a 1 $\mu$ F capacitor (ESR > 0.1 $\Omega$ /< 5 $\Omega$ , fRES > 1MHz) is sufficient for Cout (see Figure 13 on page 8).

For improved power supply noise rejection and device transient response, larger values can be used for Cout.

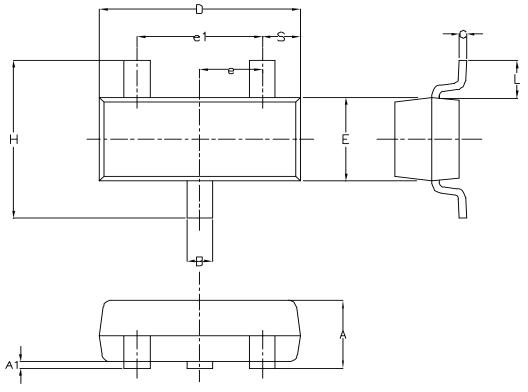
**Note:** For values of COUT >  $1\mu$ F, the input impedance must not be so large that it causes high-input impedance oscillations.



# 10 Package Drawings and Markings

The device is available in an 3-pin SOT23 package.

Figure 14. 3-pin SOT23 Package



#### Notes:

- 1. Lead coplanarity should be 0 to 0.10mm (.004") max.
- 2. Package surfacing:
  - a. Top: matte (charmilles #18-30).
  - b. All sides: matte (charmilles #18-30).
  - c. Bottom: smooth or matte (charmilles #18- 30).
- 3. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.25mm (.010") per side (D).
- 4. Details of pin #1 identifier are optional but must be located within the zone indicated.
- 5. Dimensions are in millimeters.

Symbol	Min	Max	
Α	0.89	1.12	
A1	0.013	0.100	
В	0.37	0.51	
О	0.085	0.18	
D	2.80	3.04	
Е	1.20	1.40	
е	0.89	1.03	
e1	1.78	2.05	
Н	2.10	2.64	
L	0.55ref		
Α	0.89	1.12	
S	0.45	0.60	



# 11 Ordering Information

The device is available as the standard products shown in Table 4.

Table 4. Ordering Information

Model	Marking	Description	Delivery Form	Package
AS1360-18-T	ASKD	HV low-quiescent current LDO, 1.8V	Tape and Reel	3-pin SOT23
AS1360-21-T	ASRO	HV low-quiescent current LDO, 2.1V	Tape and Reel	3-pin SOT23
AS1360-25-T	ASKE	HV low-quiescent current LDO, 2.5V	Tape and Reel	3-pin SOT23
AS1360-30-T	ASKF	HV low-quiescent current LDO, 3.0V	Tape and Reel	3-pin SOT23
AS1360-33-T	ASKG	HV low-quiescent current LDO, 3.3V	Tape and Reel	3-pin SOT23
AS1360-50-T	ASKH	HV low-quiescent current LDO, 5.0V	Tape and Reel	3-pin SOT23

All devices are RoHS compliant and free of halogene substances.



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