REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - ro	16-02-08	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 10-12-13	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, LINEAR, DUAL, HIGH SPEED BiFET OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/11603**
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AMSC N/A

5962-V036-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual, high speed bipolar field effect transistor (BiFET) operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11603	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD712-EP	Dual, high speed BiFET operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage ($\pm V_S$)	±18 V
Input voltage (V_{IN})	±18 V 2/
Output short circuit duration	Indefinite
Differential input voltage	$+V_S$ and $-V_S$
Power dissipation(P_D)	14.4 mW
Junction temperature range (T_J)	-65°C to +150°C
Storage temperature range (T_{STG})	-65°C to +125°C
Lead temperature range (soldering, 60 seconds)	+300°C
Thermal resistance, junction to ambient (θ_{JC})	43°C/W
Thermal resistance, junction to ambient (θ_{JA})	100°C/W

1.4 Recommended operating conditions. 3/

Supply voltage ($\pm V_S$)	±15 V
Operating temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ For supply voltages less than ±18 V, the absolute maximum voltage is equal to the supply voltage.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_S = ±15 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input offset voltage section 2/							
Initial offset voltage	V_{IO}		+25°C	01		3	mV
			-55°C to +125°C			4	
Initial offset voltage versus temperature	V_{IO} / T		+25°C	01		20	µV/°C
Initial offset voltage versus supply	V_{IO} / V_S		+25°C	01	76		dB
			-55°C to +125°C		76		
Long term offset stability			+25°C	01	15 typical		µV/ month
Input bias current 3/	I_{IB}	V_{CM} = 0 V	+25°C	01		75	pA
			+125°C			77	nA
		V_{CM} = ±10 V	+25°C			100	pA
Input offset current	I_{IO}	V_{CM} = 0 V	+25°C	01		25	pA
			+125°C			26	nA
Matching characteristics section							
Input offset voltage	V_{IO}		+25°C	01		3	mV
			-55°C to +125°C			4	
Input offset voltage drift			+25°C	01		20	µV/°C
Input bias current	I_{IB}		+25°C	01		25	pA
Crosstalk		At f = 1 kHz	+25°C	01	120 typical		dB
		At f = 100 kHz			90 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = ±15 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency response section							
Small signal bandwidth	SSBW		+25°C	01	3.0		MHz
Full power response	FPR		+25°C	01	200 typical		kHz
Slew rate	SR		+25°C	01	16		V/µs
Settling time to 0.01%	t_S		+25°C	01		1.2	µs
Total harmonic distortion	THD		+25°C	01	0.0003 typical		%
Input impedance section							
Differential input impedance		4/	+25°C	01	3×10^{12} || 5.5 typical		Ω||pF
Common mode input impedance		4/	+25°C	01	3×10^{12} || 5.5 typical		Ω||pF
Input voltage range section							
Differential input voltage range 5/	V_{DIN}		+25°C	01	±20 typical		V
Common mode voltage 6/	V_{CM}		+25°C	01	+14.5, -11.5 typical		V
			-55°C to +125°C		$-V_S$ + 4	$+V_S$ - 2	
Common mode rejection ratio	CMRR	V_{CM} = ±10 V	+25°C	01	76		dB
			-55°C to +125°C		76		
		V_{CM} = ±11 V	+25°C		70		
			-55°C to +125°C		70		
Input voltage noise section							
Input voltage noise		0.1 Hz to 10 Hz	+25°C	01	2 typical		µVp-p
		f = 10 Hz			45 typical		nV / √Hz
		f = 100 Hz			22 typical		
		f = 1 kHz			18 typical		
		f = 10 kHz			16 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 15$ V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input current noise	NI	f = 1 kHz	+25°C	01	0.01 typical		pA / $\sqrt{Hz}$
Open loop gain	AOL		+25°C	01	150		V/mV
			-55°C to +125°C		100		
Output characteristics							
Output voltage swing high	V_{OH}		+25°C	01		13.0	V
			-55°C to +125°C			12.0	
Output voltage swing low	V_{OL}		+25°C	01	-12.5		V
			-55°C to +125°C		-12.0		
Output current	I_{OUT}		+25°C	01	25 typical		mA
Power supply section							
Rated performance			+25°C	01	±15 typical		V
Operating range			+25°C	01	±4.5	±18	V
Quiescent current			+25°C	01		6.8	mA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

3/ Bias current specifications are guaranteed maximum at either input after five minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

4/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

5/ Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

6/ Typically exceeding -14.1 V negative common mode voltage on either input results in an output phase reversal.

Case X

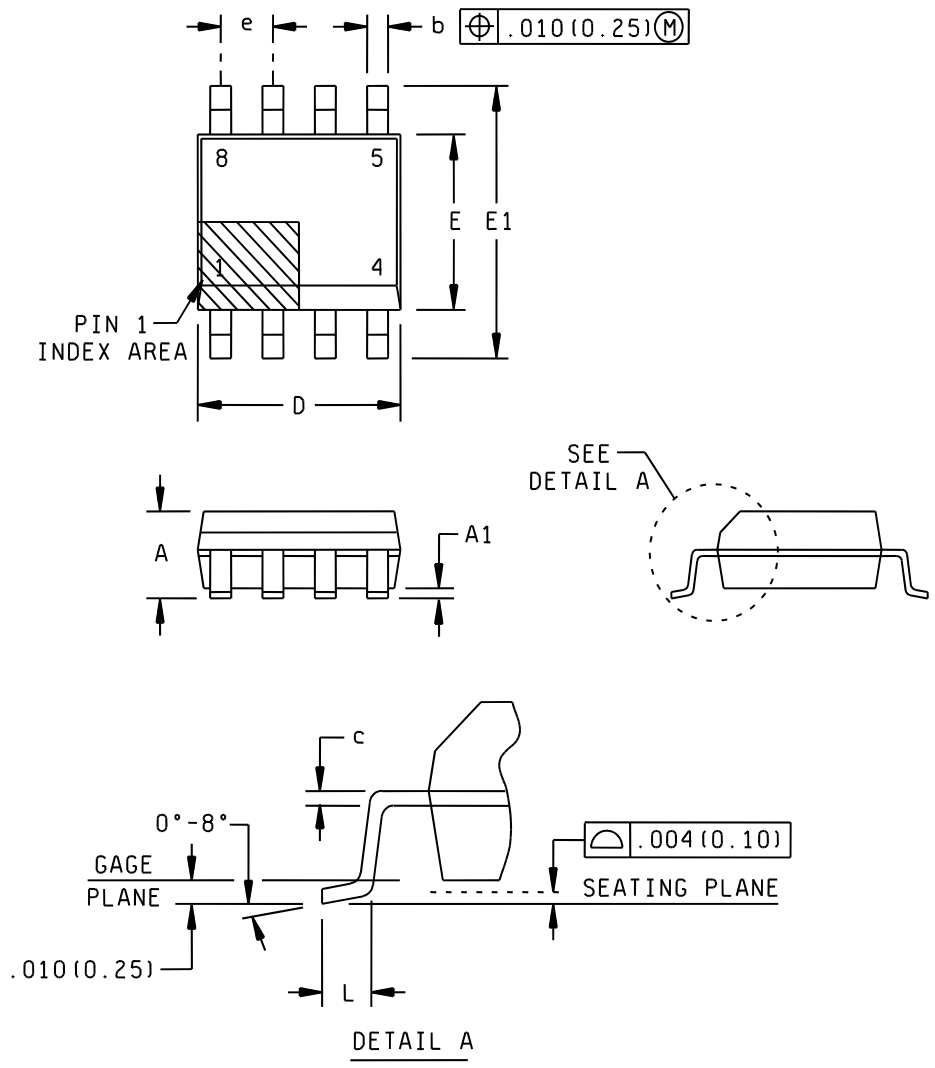

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/11603
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
b	0.0122	0.0201	0.31	0.51
c	0.0067	0.0098	0.17	0.25
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
E1	0.2284	0.2441	5.80	6.20
e	0.0500 BSC		1.27 BSC	
L	0.0157	0.0500	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only and are not appropriate for use in design.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inch (0.15 mm).
3. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outline – Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUTPUT 1
2	INVERTING INPUT 1
3	NONINVERTING INPUT 1
4	$-V_S$
5	NONINVERTING INPUT 2
6	INVERTING INPUT 2
7	OUTPUT 2
8	$+V_S$

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11603-01XE	24355	AD712TRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code
24355

Source of supply
Analog Devices
Route 1 Industrial Park
P.O. Box 9106
Norwood, MA 02062
Point of contact: Raheen Business Park
Limerick, Ireland