REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 12-10-09	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, LINEAR, LOW DISTORTION DIFFERENTIAL ADC DRIVER, MONOLITHIC SILICON
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12629**
	REV	**PAGE** 1 **OF** 12

AMSC N/A

5962-V007-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low distortion differential ADC driver microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12629	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD8138-EP	Low distortion differential ADC driver

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MO-187-AA	Mini Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage	±5.5 V
V_{OCM}	$\pm V_S$
Output voltage swing	See FIGURE 5 and 6
Internal power dissipation	550 mW
Operating temperature range:	-55°C to +105°C
Storage temperature range	-65°C to 150°C
Lead temperature, (Soldering, 10 sec)	300°C
Junction temperature	150°C

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	Unit
Case X	145	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Maximum power dissipation vs ambient temperature. The maximum power dissipation vs ambient temperature shall be as shown in figure 4.

3.5.5 Differential output voltage swing vs ambient temperature, $V_S = \pm 5$ V. The differential output voltage swing vs ambient temperature, $V_S = \pm 5$ V shall be as shown in figure 5.

3.5.6 Differential output voltage swing vs ambient temperature, $V_S = 5$ V. The differential output voltage swing vs ambient temperature, $V_S = 5$ V shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
$\pm D_{IN}$ TO $\pm$OUT SPECIFICATIONS 2/						
Dynamic performance						
-3 dB small signal bandwidth		V_{OUT} = 0.5 V p-p, C_F = 0 pF	290	320		MHz
		T_{MIN} to T_{MAX} 3/	256			
		V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		
Bandwidth for 0.1 dB Flatness		V_{OUT} = 0.5 V p-p, C_F = 0 pF		30		
Large signal bandwidth		V_{OUT} = 2 V p-p, C_F = 0 pF		265		
Slew rate		V_{OUT} = 2 V p-p, C_F = 0 pF		1150		V/µs
Settling time		0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive recovery time		V_{IN} = 5 V to 0 V step, G = +2		4		
Noise/Harmonic performance						
Second Harmonic		V_{OUT} = 0.5 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		-94		dBc
		V_{OUT} = 0.5 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		-87		
		V_{OUT} = 0.5 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		-62		
Third Harmonic		V_{OUT} = 0.5 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		-114		
		V_{OUT} = 0.5 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		-85		
		V_{OUT} = 0.5 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		-57		
IMD		20 MHz		-77		
IP3		20 MHz		37		dBm
Voltage noise (RTI)		f = 100 kHz to 40 MHz		5		nv/√Hz
Input current noise		f = 100 kHz to 40 MHz		2		pA/√Hz
Input characteristics						
Offset voltage		$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	-2.5	±1	+2.5	mV
		T_{MIN} to T_{MAX} 3/	-4.8		+4.8	
Input bias current				3.5	7	µA
		T_{MIN} to T_{MAX} variation		-0.01		µA/°C
Input resistance		Differential		6		MΩ
		Common mode		3		
Input capacitance				1		pF
Input common mode voltage				-4.7 to +3.4		V
CMRR		$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V,		-77	-70	dB
		T_{MIN} to T_{MAX} 3/			-69	
Output characteristics						
Output voltage swing 4/		Maximum ΔV_{OUT}; single ended output		7.75		V p-p
Output balance error		$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V,		-66		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OCM} TO ±OUT SPECIFICATIONS 2/						
Dynamic performance						
-3dB bandwidth				250		MHz
Slew rate				330		V/µs
Noise						
Input voltage noise (RTI)		f = 0.1 MHz to 100 MHz		17		nv/√Hz
DC performance						
Input voltage range				±3.8		V
Input resistance				200		kΩ
Input offset voltage		$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	-3.5	±1	+3.5	mV
		T_{MIN} to T_{MAX} 3/	-10.2		+10.2	
Input bias current				0.5		µA
V_{OCM} CMRR		$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V,		-75		dB
Gain		$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V; T_{MIN} to T_{MAX} 3/	0.9955	1	1.0045	V/V
Power supply						
Operating range			±1.4		±5.5	V
Quiescent current			18	20	23	mA
		T_{MIN} to T_{MAX} 3/	13.2			mA
Power supply rejection ratio		$\Delta V_{OUT, dm}/\Delta V_S$, ΔV_S = ±1 V; T_{MIN} to T_{MAX} 3/		-90	-70	dB
Operating temperature range			-55		+105	°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
±D_{IN} TO ±OUT SPECIFICATIONS 5/						
Dynamic performance						
-3 dB small signal bandwidth		V_{OUT} = 0.5 V p-p, C_F = 0 pF	280	310		MHz
		T_{MIN} to T_{MAX} 3/	242			
		V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		
Bandwidth for 0.1 dB flatness		V_{OUT} = 0.5 V p-p, C_F = 0 pF		29		
Large signal bandwidth		V_{OUT} = 2 V p-p, C_F = 0 pF		265		
Slew rate		V_{OUT} = 2 V p-p, C_F = 0 pF		950		V/µs
Settling time		0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive recovery time		V_{IN} = 5 V to 0 V step, G = +2		4		
Noise/Harmonic performance						
Second Harmonic		V_{OUT} = 0.5 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		-90		dBc
		V_{OUT} = 0.5 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		-79		
		V_{OUT} = 0.5 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		-60		
Third Harmonic		V_{OUT} = 0.5 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		-100		
		V_{OUT} = 0.5 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		-82		
		V_{OUT} = 0.5 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		-53		
IMD		20 MHz		-74		
IP3		20 MHz		35		dBm
Voltage noise (RTI)		f = 100 kHz to 40 MHz		5		nv/√Hz
Input current noise		f = 100 kHz to 40 MHz		2		pA/√Hz
Input characteristics						
Offset voltage		$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V	-2.5	±1	+2.5	mV
		T_{MIN} to T_{MAX} 3/	-5.1		+5.1	
Input bias current				3.5	7	µA
		T_{MIN} to T_{MAX} variation		-0.01		µA/°C
Input resistance		Differential		6		MΩ
		Common mode		3		
Input capacitance				1		pF
Input common mode voltage				-0.3 to +3.2		V
CMRR		$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = 1 V,		-77	-70	dB
		T_{MIN} to T_{MAX} 3/			-69.5	
Output characteristics						
Output voltage swing 4/		Maximum ΔV_{OUT}; single ended output		2.9		V p-p
Output balance error		$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V,		-65		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OCM} TO ±OUT SPECIFICATIONS 5/						
Dynamic performance						
-3dB bandwidth				220		MHz
Slew rate				250		V/µs
Noise						
Input voltage noise (RTI)		f = 0.1 MHz to 100 MHz		17		nv/√Hz
DC performance						
Input voltage range				1.0 to 3.8		V
Input resistance				100		kΩ
Input offset voltage		$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	-5	±1	+5	mV
		T_{MIN} to T_{MAX} 3/	-9.7		+9.7	
Input bias current				0.5		µA
V_{OCM} CMRR		$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 ±1 V,		-70		dB
Gain		$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 ±1 V; T_{MIN} to T_{MAX} 3/	0.9968	1	1.0032	V/V
Power supply						
Operating range			2.7		11	V
Quiescent current			15	20	21	mA
		T_{MIN} to T_{MAX} 3/	10.6			mA
Power supply rejection ratio		$\Delta V_{OUT, dm}/\Delta V_S$, ΔV_S = ±1 V;		-90	-70	dB
		T_{MIN} to T_{MAX} 3/			-57	
Operating temperature range			-55		+105	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

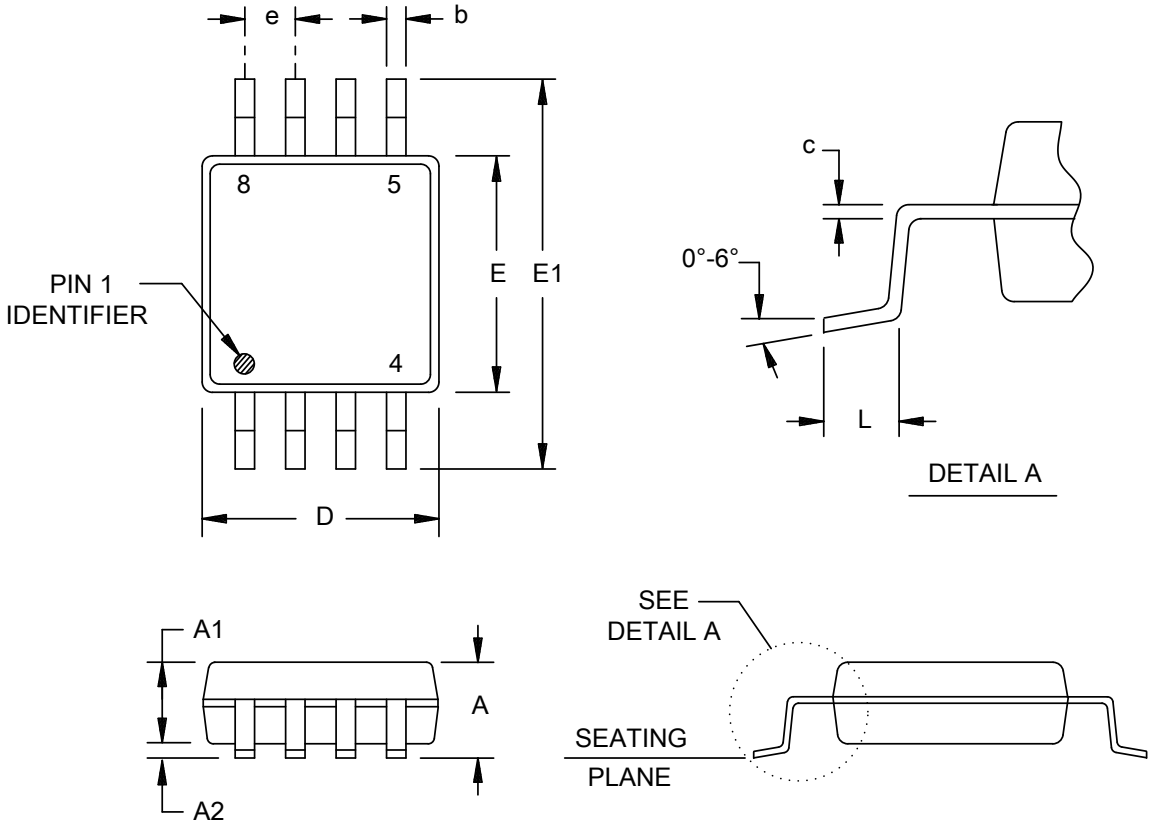
2/ At 25°C, V_S = ±5 V, V_{OCM} = 0 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. All specifications refer to single ended input and differential outputs, unless otherwise noted.

3/ Specified to ±6 sigma over the -40°C to +105°C operating temperature range.

4/ Output swing capabilities vary over operating temperature. See FIGURE 5 for more information.

5/ At 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. All specifications refer to single ended input and differential outputs, unless otherwise noted.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.10	D/E	2.80	3.20
A1	0.75	0.95	E1	4.65	5.15
A2	0.05	0.15	e	0.65 BSC	
b	0.25	0.40	L	0.40	0.80
c	0.09	0.23			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-187-AA.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	-IN	8	+IN
2	V_{OCM}	7	NC
3	V+	6	V-
4	+OUT	5	-OUT

FIGURE 2. Terminal connections.

Terminal		Description
Number	Mnemonic	
1	-IN	Negative input summing node.
2	V_{OCM}	Voltage applied to this pin sets the common mode output voltage with a ratio of 1:1. For example, 1 Vdc on V_{OCM} sets the dc bias level on +OUT and –OUT to 1 V.
3	V+	Positive supply voltage.
4	+OUT	Positive output. Note that the voltage at $-D_{IN}$ is inverted at +OUT.
5	-OUT	Negative output. Note that the voltage at $+D_{IN}$ is inverted at -OUT.
6	V-	Negative supply voltage.
7	NC	No connect.
8	+IN	Positive input summing node.

FIGURE 3. Terminal function.

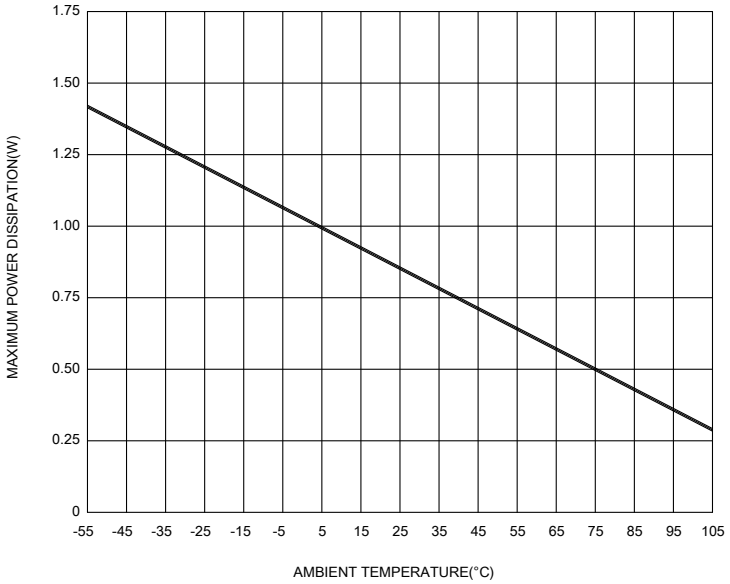


FIGURE 4. Maximum power dissipation vs ambient temperature.

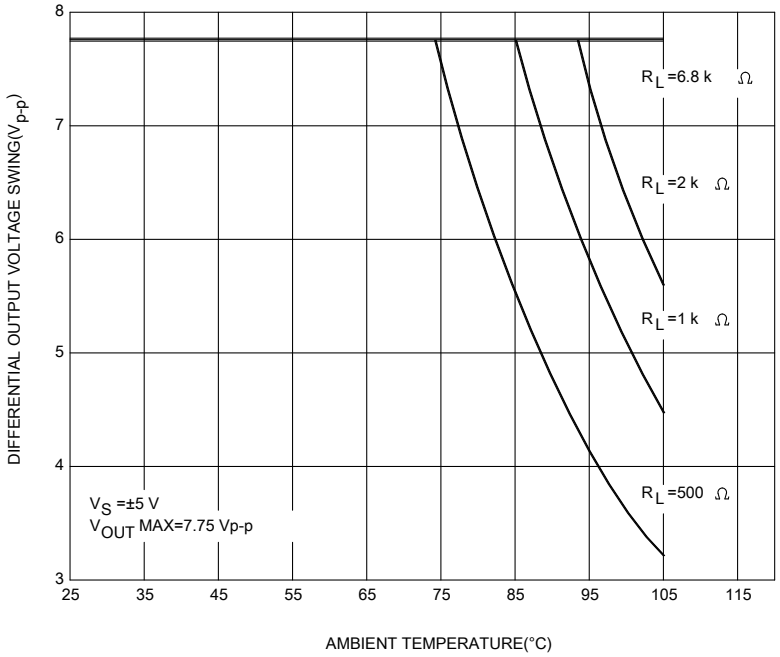


FIGURE 5. Differential output voltage swing vs ambient temperature, V_S = ±5 V.

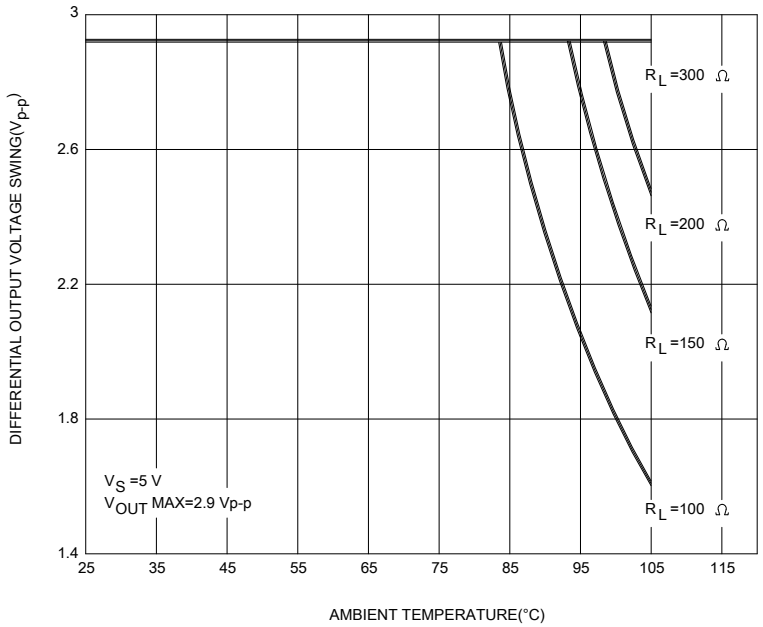


FIGURE 6. Differential output voltage swing vs ambient temperature, V_S = 5 V.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12629-01XE	24355	AD8138SRMZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106