## FEATURES

Gain set with 2 external resistors
Gain range: $\mathbf{1}$ to 1000
Input voltage goes below ground
Very wide power supply range
Single supply: 2.7V to 36V
Dual supply: $+/-2.7 \mathrm{~V}$ to $+/-18 \mathrm{~V}$
Bandwidth (G=100): $\mathbf{2 . 5}$ kHz
Input noise: $50 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$
Max supply current: $\mathbf{9 0} \boldsymbol{\mu \mathrm { A }}$
Max offset voltage: $\mathbf{2 0 0} \mathbf{u V}$
Max differential input voltage: 1V
Min CMRR: 100 dB
MSOP-8 package

## APPLICATIONS

## Bridge amplifiers

Pressure Measurement
Medical instrumentation
Portable data acquisition
Multichannel systems

PIN CONFIGURATION


Figure 1.

Table 1. Instrumentation Amplifiers by Category ${ }^{1}$

| General | Zero | Military | Low | Digital |
| :--- | :--- | :--- | :--- | :--- |
| Purpose | Drift | Grade | Power | Gain |
| AD8221/2 | AD8231 | AD620 | AD8420 | AD8250 |
| AD8220/4 | AD8290 | AD621 | AD8235/6 | AD8251 |
| AD8228 | AD8293 | AD524 | AD627 | AD8253 |
| AD8295 | AD8553 | AD526 | AD8226/7 | AD8231 |
|  | AD8556 | AD624 | AD623 |  |
|  | AD8557 |  | AD8223 |  |

${ }^{1}$ See www.analog.com for the latest instrumentation amplifiers.

The AD8420 can operate off both single or dual supplies. It works well for a portable system with a limited single supply voltage and equally well for a system using large dual supplies.

Gain is set using the ratio of two resistors. A reference pin allows the user to offset the output voltage. This feature is useful when the output signal needs to be centered around a specific voltage, such as mid-supply.

The AD8420 is available in an 8 pin MSOP package. Performance is specified over the full temperature range of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. Part is operational from $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$

## Rev. PrD

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## SPECIFICATIONS

$+\mathrm{V}_{\mathrm{S}}=+5 \mathrm{~V},-\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}+}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{G}=1$ to $1000, \mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$, specifications referred to input, unless otherwise noted

Table 2.

| Parameter | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMMON-MODE REJECTION RATIO (CMRR) CMRR DC to 60 Hz CMRR at 1 kHz | $\mathrm{V}_{\text {CM }}=0 \mathrm{~V}$ to 2.7 V | 100 |  |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| NOISE <br> Voltage Noise Spectral Density Peak to Peak <br> Current Noise Spectral Density Peak to Peak | $\begin{aligned} & \mathrm{f}=1 \mathrm{kHz}, V_{\text {DIFF }} \leq 100 \mathrm{mV} \\ & \mathrm{f}=0.1 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz}, V_{\text {DIFF }} \leq 100 \mathrm{mV} \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{f}=0.1 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz} \end{aligned}$ |  | $\begin{aligned} & 50 \\ & 1.5 \end{aligned}$ |  | $n \mathrm{~V} / \sqrt{ } \mathrm{Hz}$ <br> $\mu \mathrm{V}$ p-p <br> fA/ $\sqrt{\mathrm{Hz}}$ <br> pA p-p |
| VOLTAGE OFFSET <br> Offset <br> Average Temperature Coefficient Offset RTI vs. Supply (PSR) | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | $\begin{aligned} & 200 \\ & 1 \end{aligned}$ | $\mu \mathrm{V}$ <br> $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> dB |
| INPUTS <br> Input Bias Current ${ }^{1}$ <br> Average Temperature Coefficient Input Offset Current <br> Average Temperature Coefficient Input Impedance <br> Differential <br> Common Mode <br> Differential Input Operating Voltage Input Operating Voltage (+IN, -IN, or REF) | Valid for REF \& FB pair, as well as +IN \& -IN $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\begin{aligned} & -1 \\ & -V_{S}-0.15 \\ & -V_{S}-0.05 \\ & -V_{S}-0.2 \end{aligned}$ | 25 <br> 1 <br> 130\||2 <br> 1000\||2 | 40 <br> 1 <br> $+V_{s}-2.2$ <br> $+V_{s}-1.8$ <br> $+V_{s}-2.7$ | $n A$ $n A$ $n A$ $p A /{ }^{\circ} \mathrm{C}$ $n A$ $n A$ $n A$ $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ $\mathrm{M} \Omega \\| \mathrm{lpF}$ $\mathrm{M} \Omega \\| \mathrm{pF}$ V V V V |
| DYNAMIC RESPONSE <br> Small Signal -3 dB Bandwidth $\begin{aligned} & G=1 \\ & G=10 \\ & G=100 \\ & G=1000 \end{aligned}$ <br> Settling Time 0.01\% $\begin{aligned} G & =10 \\ G & =100 \\ G & =1000 \end{aligned}$ <br> Slew Rate | 4 V step |  | 250 <br> 25 <br> 2.5 <br> 0.25 <br> Bandwid |  | kHz <br> kHz <br> kHz <br> kHz <br> $\mu \mathrm{s}$ <br> $\mu \mathrm{s}$ <br> $\mu \mathrm{s}$ <br> $\mathrm{V} / \mu \mathrm{s}$ |


${ }^{1}$ The input stage uses pnp transistors, so input bias current always flows out of the part.
${ }^{2}$ For G $>1$, errors from external resistors R1 and R2 should be added to these specifications, including error from FB pin bias current.
${ }^{3}$ Minimum supply voltage indicated for $\mathrm{V}_{+ \text {IN }}, \mathrm{V}_{-\mathrm{IN}}, \mathrm{V}_{\text {REF }}=0 \mathrm{~V}$.
${ }^{4}$ See Typical Performance Curves for operation between $85^{\circ} \mathrm{C}$ and $125^{\circ} \mathrm{C}$
$+\mathrm{V}_{\mathrm{S}}=+15 \mathrm{~V},-\mathrm{V}_{\mathrm{S}}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{G}=1$ to $1000, \mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$, specifications referred to input, unless otherwise noted
Table 3.


${ }^{1}$ The input stage uses pnp transistors, so input bias current always flows out of the part.
${ }^{2}$ For G>1, errors from external resistors R1 and R2 should be added to these specifications, including error from FB pin bias current
${ }^{3}$ Minimum positive supply voltage indicated for $\mathrm{V}_{+\mid \mathrm{IN},} \mathrm{V}_{-\mathrm{IN},} \mathrm{V}_{\text {REF }}=0 \mathrm{~V}$. With $\mathrm{V}_{+ \text {IN }}, \mathrm{V}_{-\mathrm{IN},}, \mathrm{V}_{\text {REF }}=-\mathrm{VS}$, minimum supply is $\pm 1.35 \mathrm{~V}$.
${ }^{4}$ See Typical Performance Curves for operation between $85^{\circ} \mathrm{C}$ and $125^{\circ} \mathrm{C}$

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter | Rating |
| :--- | :--- |
| Supply Voltage | $\pm 18 \mathrm{~V}$ |
| Output Short-Circuit Current | Indefinite |
| Maximum Voltage at -IN or +IN | $-\mathrm{Vs}+40 \mathrm{~V}$ |
| Minimum Voltage at -IN or +IN | $+\mathrm{Vs}-40 \mathrm{~V}$ |
| Maximum Voltage at REF | $+\mathrm{Vs}+0.2 \mathrm{~V}$ |
| Minimum Voltage at REF | $-\mathrm{Vs}-0.2 \mathrm{~V}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| ESD |  |
| $\quad$Human Body Model <br> Charge Device Model <br> Machine Model |  |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{\mathrm{JA}}$ is specified for a device in free air.
Table 5.

| Package | $\boldsymbol{\theta}_{\mathrm{JA}}$ | Unit |
| :--- | :--- | :--- |
| 8-Lead MSOP, 4-Layer JEDEC Board | 135 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

ESD CAUTION

|  | ESD (electrostatic discharge) sensitive device. <br> Charged devices and circuit boards can discharge <br> without detection. Although this product features <br> patented or proprietary protection circuitry, damage <br> may occur on devices subjected to high energy ESD. <br> Therefore, proper ESD precautions should be taken to <br> avoid performance degradation or loss of functionality. |
| :--- | :--- |

## Preliminary Technical Data

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
| :--- | :--- | :--- |
| 1 | NC | This pin not connected internally. For best CMRR vs. frequency and leakage performance, connect this pin to <br> negative supply. <br> 2 |
| 3 | + Positive Input. |  |
| 4 | - IN | Negative Input |
| 5 | $-V_{S}$ | Negative Supply. |
| 6 | $+V_{S}$ | Positive Supply. |
| 7 | REF | Reference. |
| 8 | VB | Feedback. |

## THEORY OF OPERATION



Figure 3. Simplified Schematic

## ARCHITECTURE

The AD8420 consists of three amplifiers: two matched transconductance amplifiers that convert voltage to current and one integrator amplifier that converts current to voltage.
The AD8420 works as follows: assume a differential voltage is applied across inputs +IN and -IN. This input voltage is converted into a current by Amplifier A1. This will create a difference in current between A1 and A2, which is fed into A3. A3's output voltage will change until A2 sinks all the current A1 is generating. Because the gain of A1 and A2 are matched, this means the differential input voltage across A1 will appear across the inputs of A2. Gain is set by the ratio of R2 to R1.
Because the AD8420 converts the input differential signals to a current, there are no internal headroom issues as with traditional instrumentation amplifier architectures. This is particularly important when amplifying a signal with a common mode voltage near one of the supply rails.
To improve robustness and ease of use, the AD8420 includes overvoltage protection on its inputs. This protection scheme allows input voltages well beyond the supply rails (as well as wide differential input voltages) without damaging the part.

## SETTING THE GAIN

The transfer function of the AD8420 is

$$
V_{\text {OUT }}=G\left(V_{\text {IN }+}-V_{\text {IN- }}\right)+V_{\text {REF }}
$$

where:
$G=1+\frac{\mathrm{R} 2}{\mathrm{R} 1}$

Table 7. Suggested Resistors for Various Gains - 1\% Resistors

| R1 $(\mathbf{k}$ ) | R2 $(\mathbf{k} \Omega)$ | Gain |
| :--- | :--- | :--- |
| none | short | 1.00 |
| 49.9 | 49.9 | 2.00 |
| 20 | 80.6 | 5.03 |
| 10 | 90.9 | 10.09 |
| 5 | 95.3 | 20.06 |
| 2 | 97.6 | 49.8 |
| 1 | 100 | 101 |
| 1 | 200 | 201 |
| 1 | 499 | 500 |
| 1 | 1000 | 1001 |

While the ratio of R2 to R1 sets the gain, the absolute value of the resistors is up to the designer. Larger values reduce power consumption and output loading; smaller values limit FB input bias current error.

A method that allows large value feedback resistors while limiting FB bias current error is to place a resistor of value $\mathrm{R} 1|\mid \mathrm{R} 2$ in series with the REF terminal as shown in Figure 4. At higher gains, this resistor can simply be the same value as R1.


Figure 4. Cancelling Out Error from FB Input Bias Current

## INPUT VOLTAGE RANGE

Unlike traditional instrumentation amplifier architectures, the allowed input range of the AD8420 is simplicity itself. For the AD8420's transfer function to be valid, the input voltage should follow two rules:

1) Keep differential input voltage within $\pm 1 \mathrm{~V}$.
2) Keep voltage on +IN , -IN, and REF pins in specified input voltage range

No hexagonal figures. No complicated formulas.

## INPUT PROTECTION

The AD8420 has very robust inputs and typically does not need additional input protection. Input voltages can be up to 40 V from the opposite supply rail. For example, with a +5 V positive supply and a -8 V negative supply, the part can safely withstand voltages from -35 V to 32 V . The part can handle large differential input voltages, even when the part is in high gain, without damage.
The rest of the AD8420 terminals should be kept within the supplies. All terminals of the AD8426 are protected against ESD.
For applications that require protection beyond the AD8420's limits, place diodes at the AD8420 inputs to limit voltage and resistors in series with the inputs to limit the current into these diodes. To keep input bias current at minimum, low leakage diode clamps such as the BAV199 should be used. The AD8420 also combines well with TVS diodes such as the PTVSxS1UR.

## DRIVING THE REFERENCE PIN

Traditional instrumentation amplifier architectures require the reference pin to be driven with a low impedance source. In traditional architectures, impedance at the reference pin degrades both CMRR and gain accuracy. With the AD8420 architecture, resistance at the reference pin has no effect on CMRR.


Figure 5. Calculating Gain with Reference Resistance
Resistance at the reference pin does affect the AD8420's gain, but if this resistance is constant, the gain setting resistors can be adjusted to compensate. For example, the AD8420 can be driven with a voltage divider as shown in Figure 6.


Figure 6. Using Resistor Divider to Set Reference Voltage

## OUTLINE DIMENSIONS



## ORDERING GUIDE

| Model $^{1}$ | Temperature Range | Package Description | Package | Branding |
| :--- | :--- | :--- | :--- | :--- |
| AD8420ARMZ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Standard grade, tube | MSOP | Y3Y |
| AD8420ARMZ-R7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Standard grade, 7 inch Tape and Reel | MSOP | Y3Y |
| AD8420ARMZ-RL | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Standard grade, 13 inch Tape and Reel | MSOP | Y3Y |
| AD8420BRMZ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | High performance grade, tube | MSOP | Y3Z |
| AD8420BRMZ-R7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | High performance grade, 7 inch Tape and Reel | MSOP | Y3Z |
| AD8420BRMZ-RL | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | High performance grade, 13 inch Tape and Reel | MSOP | Y3Z |

[^0]
[^0]:    ${ }^{1} Z=$ RoHS Compliant Part.

