Quad-Channel Digital Isolators, 5 kV

ADuM2400/ADuM2401/ADuM2402

FEATURES

Low power operation
- **5 V operation**
  - **1.0 mA per channel max @ 0 Mbps to 2 Mbps**
  - **3.5 mA per channel max @ 10 Mbps**
  - **31 mA per channel max @ 90 Mbps**
- **3 V operation**
  - **0.7 mA per channel max @ 0 Mbps to 2 Mbps**
  - **2.1 mA per channel max @ 10 Mbps**
  - **20 mA per channel max @ 90 Mbps**

Bidirectional communication

3 V/5 V level translation

High temperature operation: 105°C

High data rate: dc to 90 Mbps (NRZ)

Precise timing characteristics
- **2 ns max pulse-width distortion**
- **2 ns max channel-to-channel matching**

High common-mode transient immunity: > 25 kV/μs

Output enable function

Wide body SOIC 16-lead package

Safety and regulatory approvals (pending)
- **UL recognition: 5000 V rms for 1 minute per UL 1577**
- **CSA component acceptance notice #5A:**
  - **IEC 60950-1: 600 V rms (reinforced)**
  - **IEC 60601-1: 250 V rms (reinforced)**
- **VDE certificate of conformity**
  - **DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01**
  - **DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000**
  - **V_{IORM} = 848 V peak**

APPLICATIONS

General-purpose, high voltage, multichannel isolation

Medical equipment

Motor drives

Power supplies

GENERAL DESCRIPTION

The ADuM240x are 4-channel digital isolators based on Analog Devices' *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discretes is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices run at one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM240x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see Ordering Guide). The ADuM240x models operate with the supply voltage of either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM240x provide low pulse-width distortion (<2 ns for CRWZ grade) and tight channel-to-channel matching (<2 ns for CRWZ grade). Unlike other optocoupler alternatives, the ADuM240x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

FUNCTIONAL BLOCK DIAGRAMS

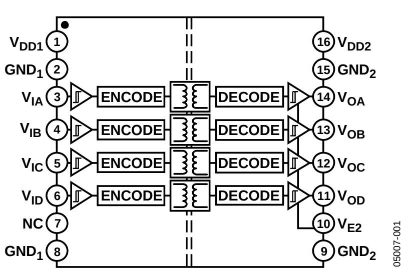

Figure 1. ADuM2400 Functional Block Diagram

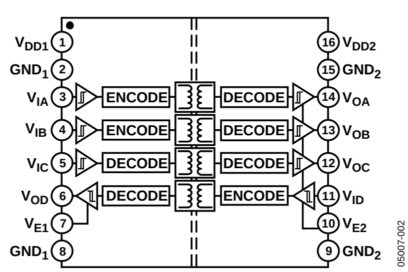

Figure 2. ADuM2401 Functional Block Diagram

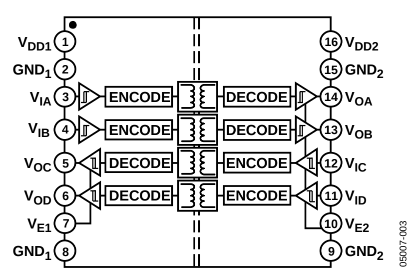

Figure 3. ADuM2402 Functional Block Diagram

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REVISION HISTORY

9/05—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

5 V OPERATION[1]

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All min/max specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.53	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.21	mA	
ADuM2400, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		8.6	10.6	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		76	100	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		21	25	mA	45 MHz logic signal freq.
ADuM2401, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		7.1	9.0	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		4.1	5.0	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		62	82	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		35	43	mA	45 MHz logic signal freq.
ADuM2402, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (90)}$, $I_{DD2 (90)}$		49	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	0.01	10	µA	0 ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	2.0			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.8		
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}/ V_{DD2} − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1}/ V_{DD2} − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
ADuM240xARWZ						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50	65	100	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels
ADuM240xBRWZ						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	32	50	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM240xCRWZ						
Minimum Pulse Width[3]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	18	27	32	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			10	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI (D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDO (D)}$		0.15		mA/Mbps	

[1] All voltages are relative to their respective ground.
[2] Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 14 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM2400/ADuM2401/ADuM2402 channel configurations.
[3] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[4] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[5] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[6] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[7] Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate than can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

3 V OPERATION[1]

2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V. All min/max specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.31	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.14	mA	
ADuM2400, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.4	2.0	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		42	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		11	15	mA	45 MHz logic signal freq.
ADuM2401, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.2	3.0	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		34	52	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		19	27	mA	45 MHz logic signal freq.
ADuM2402, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		3.0	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (90)}$, $I_{DD2 (90)}$		27	39	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	0.01	10	µA	0 ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 ≤ V_{E1},V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4		
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}/V_{DD2} − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1}/V_{DD2} − 0.4	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
ADuM240xARWZ						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50	75	100	ns	C_L = 15pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			40	ns	C_L = 15pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15pF, CMOS signal levels
ADuM240xBRWZ						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	38	50	ns	C_L = 15pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			3	ns	C_L = 15pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			22	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			3	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15pF, CMOS signal levels
ADuM240xCRWZ						
Minimum Pulse Width[3]	PW		8.3	11.1	ns	C_L = 15pF, CMOS signal levels
Maximum Data Rate[4]		90	120		Mbps	C_L = 15pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	34	45	ns	C_L = 15pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L = 15pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			16	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			2	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			5	ns	C_L = 15pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	C_L = 15pF, CMOS signal levels
Common Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI (D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] All voltages are relative to their respective ground.
[2] Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 14 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM2400/ADuM2401/ADuM2402 channel configurations.
[3] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[4] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[5] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[6] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[7] Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8V_{DD2}$. CM_L is the maximum common-mode voltage slew rate than can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

MIXED 5 V/3 V OR 3 V/5 V OPERATION[1]

5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All min/max specifications apply over the entire recommended operation range, unless otherwise noted.

All typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V; or V_{DD1} = 5 V, V_{DD2} = 3.0 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM2400, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.5	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			8.6	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			1.4	2.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			76	100	mA	45 MHz logic signal freq.
3 V/5 V Operation			42	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			11	15	mA	45 MHz logic signal freq.
3 V/5 V Operation			21	25	mA	45 MHz logic signal freq.
ADuM2401, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.8	2.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			7.1	9.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			2.2	3.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.1	5.0	mA	5 MHz logic signal freq.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1\ (90)}$					
5 V/3 V Operation			62	82	mA	45 MHz logic signal freq.
3 V/5 V Operation			34	52	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2\ (90)}$					
5 V/3 V Operation			19	27	mA	45 MHz logic signal freq.
3 V/5 V Operation			35	43	mA	45 MHz logic signal freq.
ADuM2402, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1\ (Q)}$					
5 V/3 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2\ (Q)}$					
5 V/3 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRWZ and CRWZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1\ (10)}$					
5 V/3 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2\ (10)}$					
5 V/3 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1\ (90)}$					
5 V/3 V Operation			49	62	mA	45 MHz logic signal freq.
3 V/5 V Operation			27	39	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2\ (90)}$					
5 V/3 V Operation			27	39	mA	45 MHz logic signal freq.
3 V/5 V Operation			49	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	0.01	10	µA	$0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID} \le V_{DD1}$ or V_{DD2}, $0 \le V_{E1}, V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	$V_{DD1}/V_{DD2} - 0.1$	V_{DD1}/V_{DD2}		V	$I_{Ox} = -20\ \mu A$, $V_{Ix} = V_{IxH}$
		$V_{DD1}/V_{DD2} - 0.4$	$V_{DD1}/V_{DD2} - 0.2$		V	$I_{Ox} = -4\ mA$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	$I_{Ox} = 20\ \mu A$, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400\ \mu A$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4\ mA$, $V_{Ix} = V_{IxL}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
ADuM240xARWZ						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50	70	100	ns	C_L = 15pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			40	ns	C_L = 15pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15pF, CMOS signal levels
ADuM240xBRWZ						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15pF,CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	15	35	50	ns	C_L = 15pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			3	ns	C_L = 15pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			22	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			3	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15pF, CMOS signal levels
ADuM240xCRWZ						
Minimum Pulse Width[3]	PW		8.3	11.1	ns	C_L = 15pF, CMOS signal levels
Maximum Data Rate[4]		90	120		Mbps	C_L = 15pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	30	40	ns	C_L = 15pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L = 15pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			14	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			2	ns	C_L = 15pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			5	ns	C_L = 15pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_f					C_L = 15pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI (D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDI (D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

[1] All voltages are relative to their respective ground.
[2] Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 14 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM2400/ADuM2401/ADuM2402 channel configurations.
[3] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[4] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[5] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[6] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[7] Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8V_{DD2}$. CM_L is the maximum common-mode voltage slew rate than can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{jci}		33		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{jco}		28		°C/W	

[1] Device considered a 2-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION (PENDING)

Table 5.

UL[1]	CSA	VDE[2]
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01[2]
5000 V rms isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1,600 V rms (848 V peak) maximum working voltage	Basic insulation, 848 V peak
	Approved per IEC 60601-1	Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000
	Reinforced insulation, 250 V rms maximum working voltage	Reinforced insulation, 560 V peak

[1] In accordance with UL1577, each ADuM240x is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN EN 60747-5-2, each ADuM240x is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration.
Minimum External Air Gap (Clearance)	L(I01)	7.46 min	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.10 min	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS (PENDING)

Table 7.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110			
For Rated Mains Voltage ≤ 300 V rms		I-IV	
For Rated Mains Voltage ≤ 450 V rms		I-II	
For Rated Mains Voltage ≤ 600 V rms		I-II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b1	V_{PR}	1590	V peak
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m = 1$ sec, Partial Discharge < 5 pC			
Input to Output Test Voltage, Method a	V_{PR}		
After Environmental Tests Subgroup 1			
$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, Partial Discharge < 5p C		1357	V peak
After Input and/or Safety Test Subgroup 2/3			
$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, Partial Discharge < 5p C		1018	V peak
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	V_{TR}	6000	V peak
Safety-Limiting Values (Maximum value allowed in the event of a failure, also see Figure 4)			
Case Temperature	T_S	150	°C
Side 1 Current	I_{S1}	265	mA
Side 2 Current	I_{S2}	335	mA
Insulation Resistance at T_S, $V_{IO} = 500$ V	R_S	$>10^9$	Ω

These isolators are suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

"*" marking on packages denotes DIN EN 60747-5-2 approval for 846 V peak working voltage.

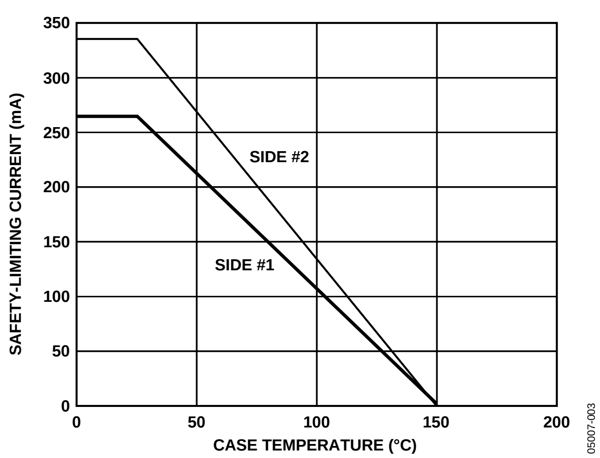

Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	–65	150	°C
Ambient Operating Temperature	T_A	–40	105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	–0.5	7.0	V
Input Voltage[1, 2]	V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}	–0.5	V_{DDI} + 0.5	V
Output Voltage[1, 2]	V_{OA}, V_{OB}, V_{OC}, V_{OD}	–0.5	V_{DDO} + 0.5	V
Average Output Current, Per Pin[3]				
Side 1	I_{O1}	–18	18	mA
Side 2	I_{O2}	–22	22	mA
Common-Mode Transients[4]		–100	+100	kV/μs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 4 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Ambient temperature = 25°C, unless otherwise noted.

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V_{PK}	50-year minimum lifetime
AC Voltage, Unipolar Waveform	848	V_{PK}	Maximum CSA/VDE approved working voltage
DC Voltage	848	V	Maximum CSA/VDE approved working voltage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 11. Truth Table (Positive Logic)

V_{IX} Input[1]	V_{EX} Input	V_{DDI} State[1]	V_{DDO} State[1]	V_{OX} Output[1]	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs returns to input state within 1 μs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs returns to input state within 1 μs of V_{DDO} power restoration if V_{EX} state is H or NC. Outputs returns to high impedance state within 8 ns of V_{DDO} power restoration if V_{EX} state is L.

[1] V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, or D). V_{EX} refers to the output enable signal on the same side as the V_{OX} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND PIN FUNCTION DESCRIPTIONS

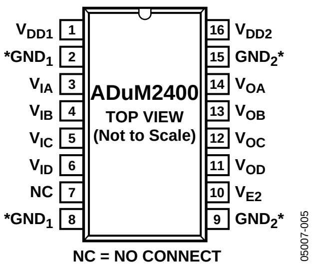

Figure 5. ADuM2400 Pin Configuration

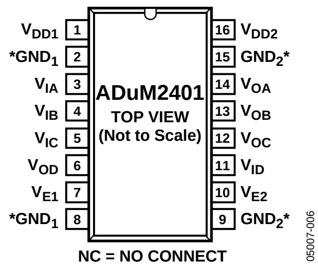

Figure 6. ADuM2401 Pin Configuration

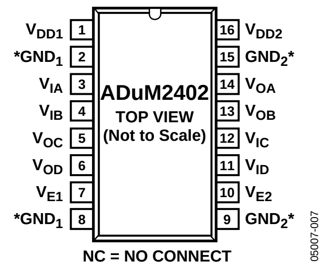

Figure 7. ADuM2402 Pin Configuration

* Pin 2 and Pin 8 are internally connected. Connecting both to GND_1 is recommended. Pin 9 and Pin 15 are internally connected. Connecting both to GND_2 is recommended. Output enable Pin 10 on the ADuM2400 may be left disconnected if outputs are always enabled. Output enable Pin 7 and Pin 10 on the ADuM2401/ADuM2402 may be left disconnected if outputs are always enabled. In noisy environments, connecting Pin 7 (for ADuM2401 and ADuM2402) and Pin 10 (for all models) to an external logic high or low is recommended.

Table 12. ADuM2400 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	NC	No Connect.
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled when V_{E2} is low.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

Table 13. ADuM2401 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output enable 1. Active high logic input. V_{OD} output is enabled when V_{E1} is high or disconnected. V_{OD} is disabled when V_{E1} is low.
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.

Table 14. ADuM2402 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. V_{OC} and V_{OD} outputs are enabled when V_{E1} is high or disconnected. V_{OC} and V_{OD} outputs are disabled when V_{E1} is low.
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. V_{OA} and V_{OB} outputs are disabled when V_{E2} is low.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

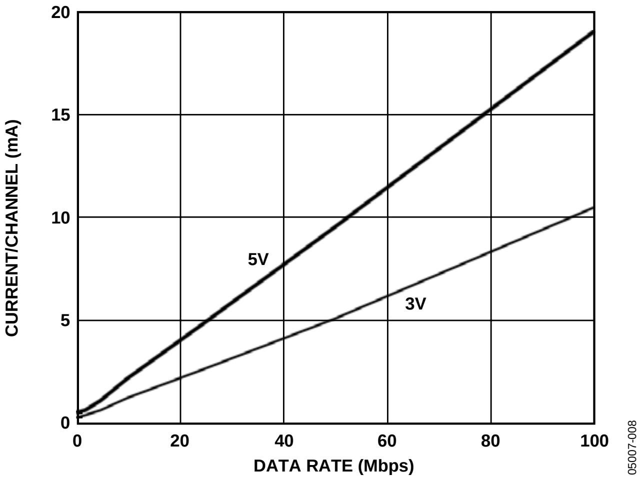

Figure 8. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

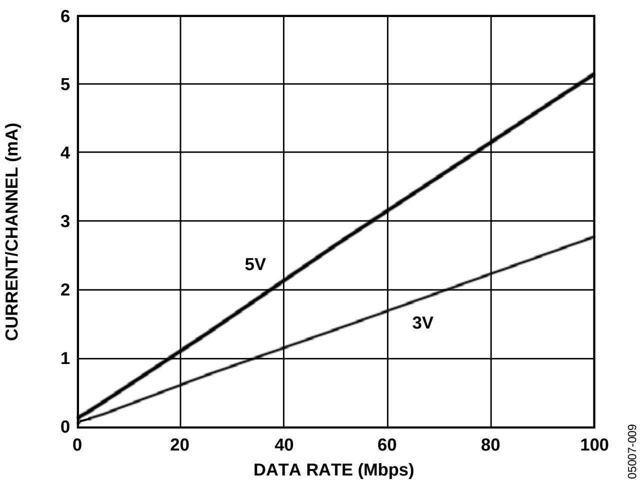

Figure 9. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

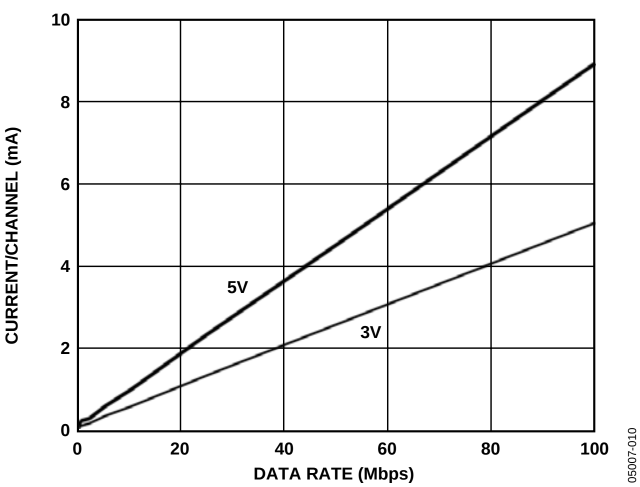

Figure 10. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

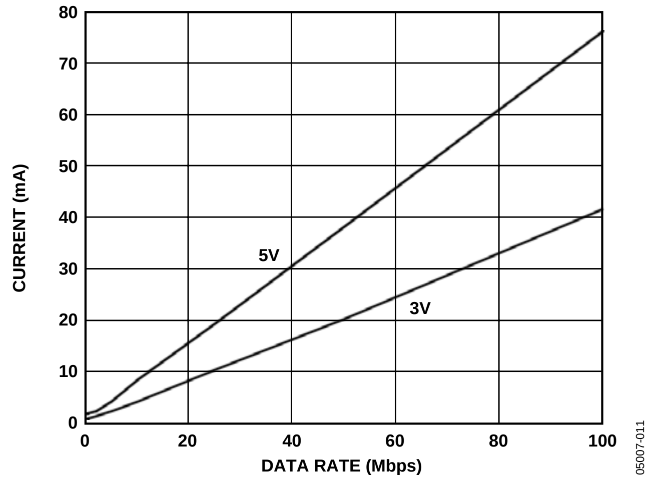

Figure 11. Typical ADuM2400 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

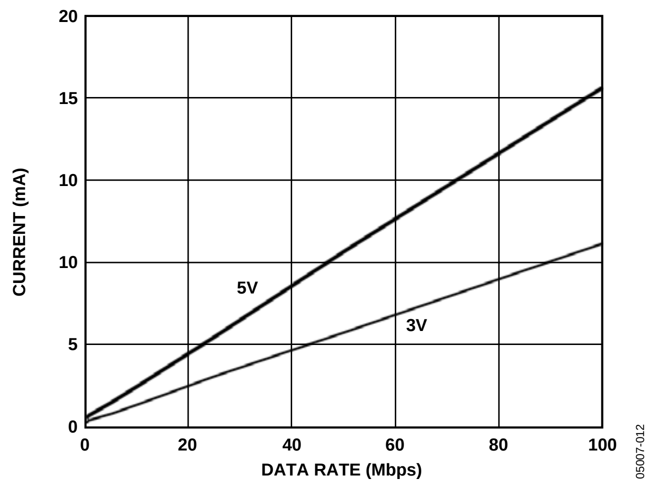

Figure 12. Typical ADuM2400 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

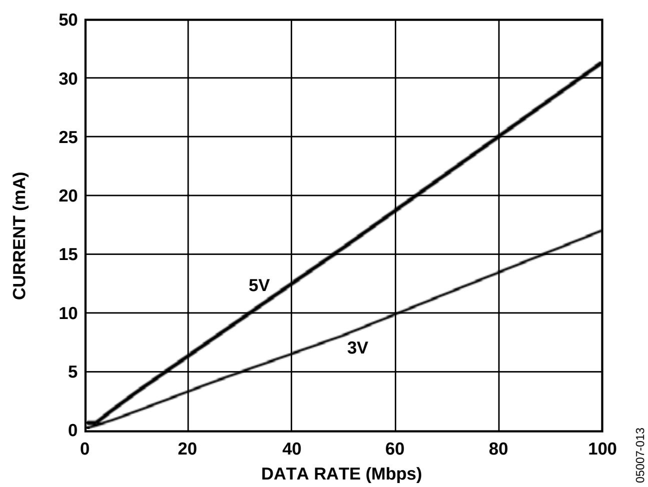

Figure 13. Typical ADuM2401 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

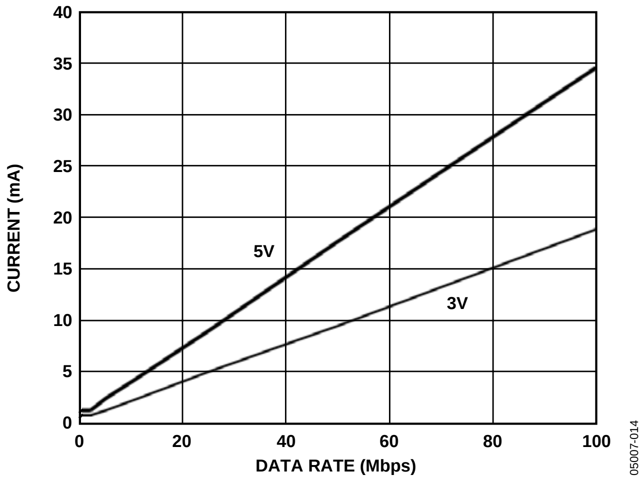

Figure 14. Typical ADuM2401 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

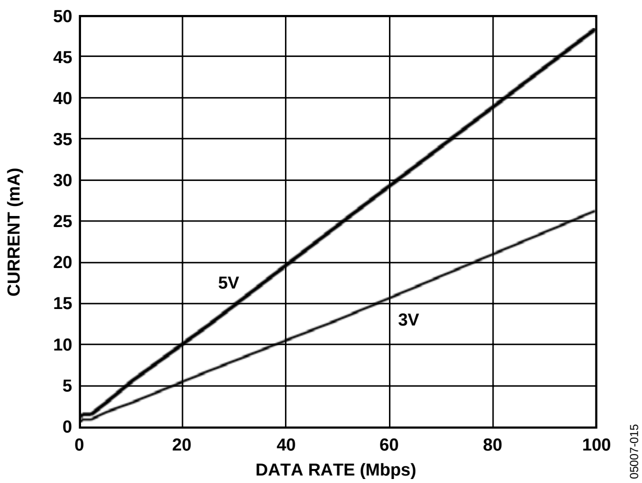

Figure 15. Typical ADuM2402 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

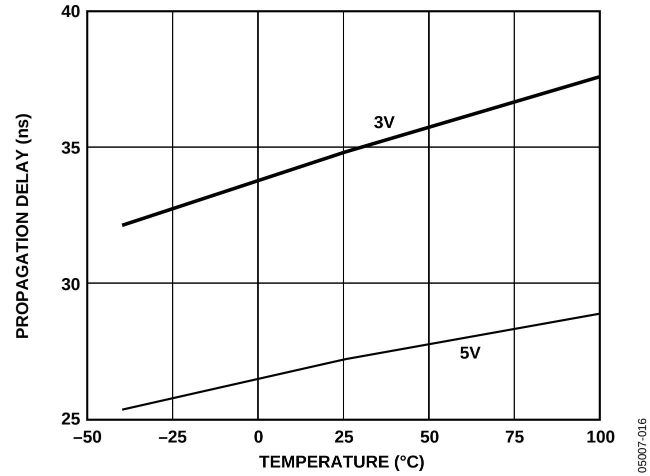

Figure 16. Propagation Delay vs. Temperature, C Grade

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM240x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side are connected close to the package.

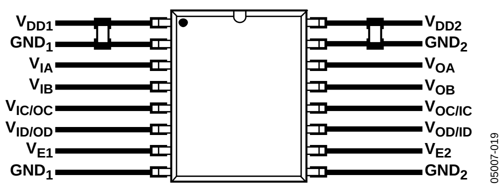

Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to logic high.

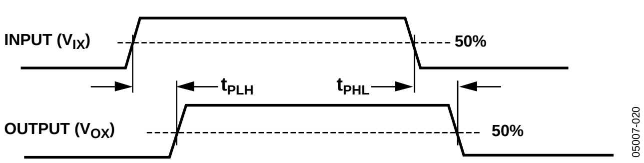

Figure 18. Propagation Delay Parameters

Pulse-width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs among channels within a single ADuM240x component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM240x components operated under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 2 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be without power or nonfunctional; in which case, the isolator output is forced to a default state (see Table 11) by the watchdog timer circuit.

The limitation on the ADuM240x's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is large enough to either falsely set or reset the decoder. The analysis below defines the conditions under which this may occur. The 3 V operating condition of the ADuM240x is examined as it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\prod r_n^2;\ n = 1, 2, \ldots, N$$

where:

β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n[th] turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM240x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

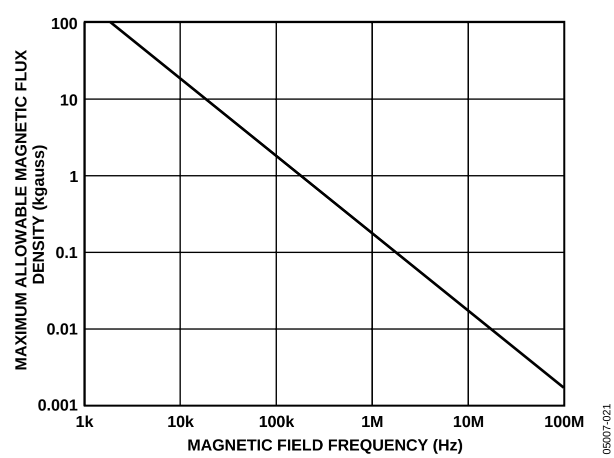

Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from > 1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM240x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM240x is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM240x to affect the component's operation.

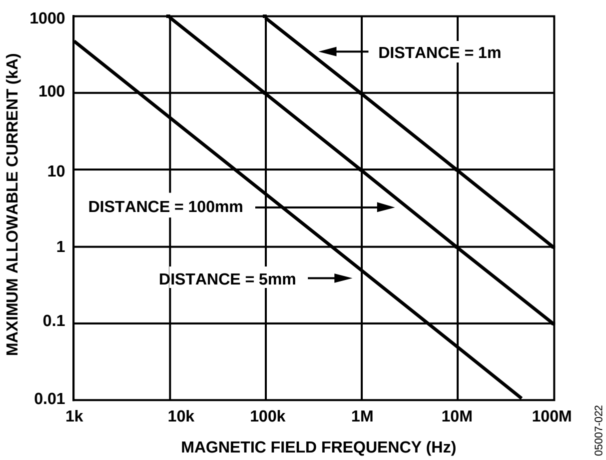

Figure 20. Maximum Allowable Current for Various Current-to-ADuM240x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM240x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by:

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by:

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3} \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 8 and Figure 9 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 14 provide total I_{DD1} and I_{DD2} supply current as a function of data rate for ADuM2400/ADuM2401/ADuM2402 channel configurations.

INSULATION LIFETIME

All insulation structures, subjected to sufficient time and/or voltage, are vulnerable to breakdown. In addition to the testing performed by the regulatory agencies, ADI has carried out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM240x.

These tests subjected populations of devices to continuous cross-isolation voltages. To accelerate the occurrence of failures, the selected test voltages were values exceeding those of normal use. The time to failure values of these units were recorded and used to calculate acceleration factors. These factors were then used to calculate the time to failure under normal operating conditions. The values shown in Table 10 are the lesser of the following two values:

- The value that ensures at least a 50-year lifetime of continuous use.
- The maximum CSA/VDE approved working voltage.

It should also be noted that the lifetime of the ADuM240x varies according to the waveform type imposed across the isolation barrier. The *i*Coupler insulation structure is stressed differently depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate the different isolation voltage waveforms.

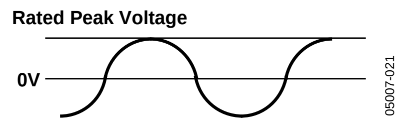

Figure 21. Bipolar AC Waveform

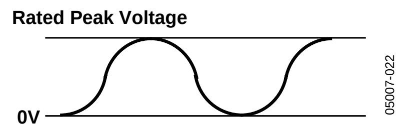

Figure 22. Unipolar AC Waveform

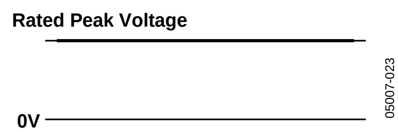

Figure 23. DC Waveform

OUTLINE DIMENSIONS

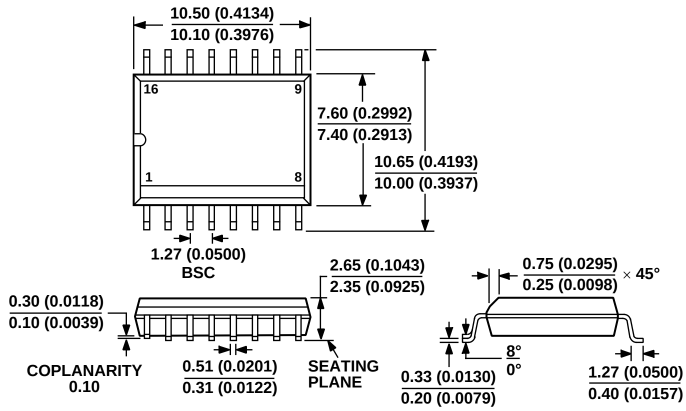

Figure 24. 16-Lead Standard Small Outline Package [SOIC]
Wide Body (RW-16)
Dimension shown in millimeters and (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse-Width Distortion (ns)	Temperature Range	Package Option[1]
ADuM2400ARWZ[2, 3]	4	0	1	100	40	–40°C to +105°C	RW-16
ADuM2400BRWZ[2, 3]	4	0	10	50	3	–40°C to +105°C	RW-16
ADuM2400CRWZ[2, 3]	4	0	90	32	2	–40°C to +105°C	RW-16
ADuM2401ARWZ[2, 3]	3	1	1	100	40	–40°C to +105°C	RW-16
ADuM2401BRWZ[2, 3]	3	1	10	50	3	–40°C to +105°C	RW-16
ADuM2401CRWZ[2, 3]	3	1	90	32	2	–40°C to +105°C	RW-16
ADuM2402ARWZ[2, 3]	2	2	1	100	40	–40°C to +105°C	RW-16
ADuM2402BRWZ[2, 3]	2	2	10	50	3	–40°C to +105°C	RW-16
ADuM2402CRWZ[2, 3]	2	2	90	32	2	–40°C to +105°C	RW-16

[1] RW-16 = 16-lead wide body SOIC.
[2] Tape and reel is available. The addition of an -RL suffix designates a 13” (1,000 units) tape and reel option.
[3] Z = Pb-free part.

NOTES

D05007–0–9/05(0)