AS3931

DataSheet

3D Low Power Wakeup Receiver

1 General Description

The AS3931 is an ultra low power, three channel LF ASK receiver designed to operate in various applications such as LF identifications systems and LF tag receivers. AS3931 detects a low frequency ASK-modulated signal by looking for a digital wakeup pattern and generates a WAKE signal after successful pattern detection. The device incorporates an intelligent pattern detection algorithm that provides reliable operation in presence of strong interference. An RSSI signal can be generated at the RSSI pin for each receiver channel.

The product is available in 16 Pin TSSOP package.

The AS3931 contains:

- Antenna rotation switch
- Three independent LF receiver chains
- Wakeup output combining the three receiver chains
- Low power 32.768kHz crystal oscillator circuit
- Serial programming interface
- Voltage regulator with 2.4 V output, on/off switchable

Each independent LF receiver chain contains:

- Input overload protection
- Input attenuator
- Ultra low power LF amplifier with logarithmic envelope output
- Robust data detector with adaptive slicing threshold that translates the logarithmic envelope into a digital data signal.
- Error tolerant digital pattern correlator that detects a given code sequences in the received data signal and generates a wakeup signal.
- Sophisticated power management logic that powers down the correlator if no data is received.

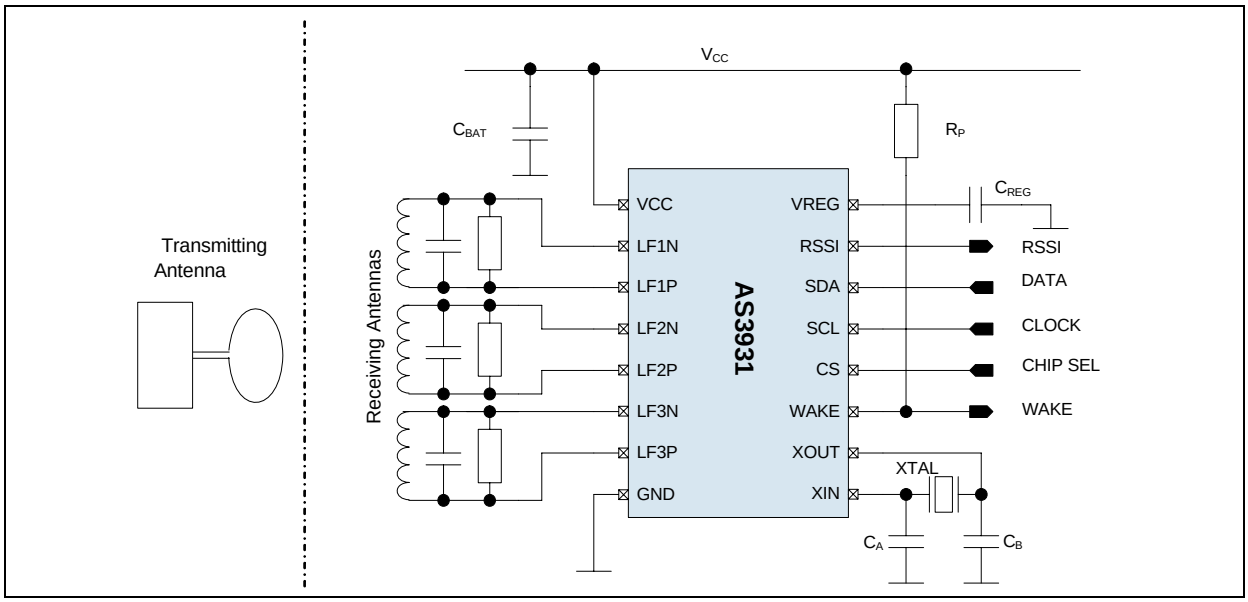
2 Key Features

- Programmable Serial Data Interface
- Flexible carrier frequencies
- Three axis wakeup pattern detection
- Three axis LF field strength measurement
- Antenna rotation for easy calibration
- High sensitivity and high dynamic range
- Wide operating frequency range
- Reliable, interference resistant wakeup decoding
- Highly protected differential inputs
- Ultra low power consumption
- 16 Pin TSSOP Package

3 Applications

The device is ideal for LF identification systems, LF tag receivers, three dimensional LF field strength measurement systems, and Ultra low power wake up systems.

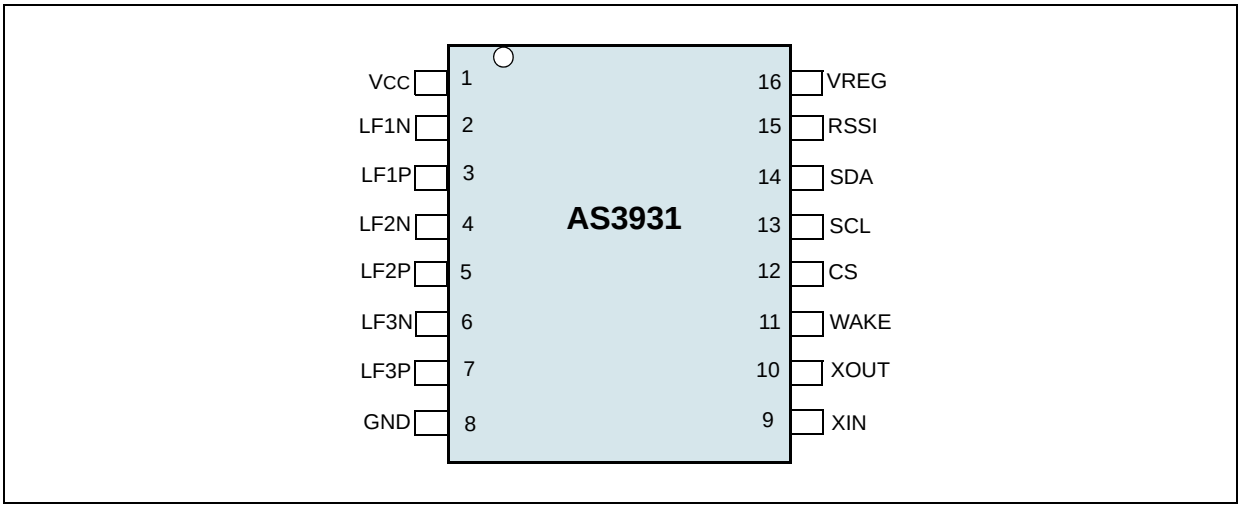
Figure 1. Typical Application Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments 16 Pin TSSOP Package



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
VCC	1	Supply Input	Positive Supply Voltage
LF1N	2	Analog Input	Channel 1 negative input
LF1P	3	Analog Input	Channel 1 positive input
LF2N	4	Analog Input	Channel 2 negative input
LF2P	5	Analog Input	Channel 2 positive input
LF3N	6	Analog Input	Channel 3 negative input
LF3P	7	Analog Input	Channel 3 positive input
GND	8	Ground	Negative Supply Voltage
XIN	9	Analog Input	Crystal Oscillator Pin 1
XOUT	10	Analog Output	Crystal Oscillator Pin 2
WAKE	11	Open Drain	Wake Up Detect output/Reset output
CS	12	Digital Input with Pulldown	Chip Select
SCL	13	Digital Input with Pulldown	Serial Clock
SDA	14	Digital Input with Pulldown	Serial Data
RSSI	15	Analog/Digital output	Received Signal Strength Indicator signal/ Digital Test mode signal output
VREG	16	Analog Output	Regulator Output Voltage

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Positive supply voltage (V_{CC})	-0.5	5.5	V	
Analog ground (GND)	0	0	V	
Voltage at any pin except pin 2 to pin 7 (V_{IN})	GND-0.5	V_{CC}+0.5	V	
Voltage at Pin 2 to Pin 7 (V_{IN})	GND-0.5	GND+0.5	V	
Input current (Latchup Immunity) (I_{in})	-100	+100	mA	
Electrostatic discharge (V_{ESD})		1000	V	HBM: R=1.5 kΩ, C=100 pF
Total power dissipation (P_{tot})		300	mW	
Storage temperature (T_{stg})	-55	125	ºC	
Solder temperature (T_{body})		240	ºC	According to: IEC 61760-1, soldering conditions
Operating Ambient Temperature Range (T_{AMB})	-20	+65	ºC	
Recommended Operating Conditions				
Positive supply voltage (V_{CC})	2.6	5.5	V	Regulator used
Positive supply voltage (V_{CC})	2.4	3.5	V	Regulator not used
Analog Ground (GND)	0	0	V	

6 Electrical Characteristics

T_{AMB} = -20° to +65° C, V_{CC} = 3.0 V, f_{IN} = 20 kHz, register settings as after POR, CS = low, transmission protocol according to Figure 15, Figure 16 and application circuit according to Figure 1 unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
General							
f_{IN}	LF input carrier frequency range			19		150	kHz
B_R	Half-bit rate[1]			2.704	2.731	2.758	kB/s
B_M	Manchester Bit Rate[2]			1.352	1.365	1.379	kB/s
W	Manchester Code Word[3]				96		hex
N_{PRE}	Preamble half-bits[4]			8			
V_{REG}	Regulator Voltage[5]	V_{CC} = 2.6 V to 5.5 V		2.30	2.4	2.60	V
T_{POR}	Power On Reset time[6]	V_{CC} = 2.4 V to 5.5 V		5			ms
I_{CC}	operating current	regulator off, V_{CC} = 2.4 V; T_{AMB} = 27° C	sleep mode		0.3		µA
			standby mode		6.5		µA
			receive mode		6.7		µA
		regulator off, V_{CC} = 2.4V to 3.5V; T_{AMB} = 27° C	sleep mode		0.5		
			standby mode		6.8		
		regulator on, T_{AMB} = 27° C	sleep mode		0.8	1.5	µA
			standby mode		7.0	8.8	µA
			receive mode		7.2	9	µA
		regulator on, RSSI-step = low; T_{AMB} = 27° C	standby mode		6.6		
I_{BUF}	RSSI buffer operating current[7]	No load at RSSI-Pin			2		µA
ΔV_{CC}	V_{CC} transient compliance[8]	recovery time = 10 ms; regulator on[8], 2.6 V < V_{CC} < 5.5 V for V_{CC} after step				2	V
		recovery time = 10 ms; regulator off[8]; 2.4 V < V_{CC} < 5.5 V for V_{CC} before step				0.3	V
Z_{IN}	Differential small sig. input impedance	normal operation; T_{AMB} = 27º			2		MΩ
		input attenuator active; T_{AMB} = 27º			1.5		kΩ
		input shortcutting active; T_{AMB} = 27º			0.5		kΩ
f_{XTAL}	crystal oscillator frequency	Crystal type: CC4 from MicroCrystal[9]			32.768		kHz

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
WAKEUP						
$V_{in,min}$	minimum differential input voltage for wake up detection[10]	N_{PRE} = 8 t_{rise},t_{fall} < 150 µs; V_{REG} = 2.4 V to 3.5 V[11]	350			µVpp
$V_{in,max}$	maximum differential input voltage for wake up detection[10]				1	Vpp
I_{WAKE}	WAKE pin current	Voltage at WAKE pin: V_{OL} < 0.4 V; V_{REG} = 2.4 V to 3.5 V[11]			0.33	mA
RSSI						
V_{RSSI}	RSSI output voltage range		0.5		1.7	V
V_{RSSI0}	RSSI output voltage (RSSI offset)	V_{IN} = 0;	0.5	0.76	1.2	V
V_{STEP}	RSSI output voltage step[12]	V_{IN} = 1 mV_{pp};	100	290		mV
V_{LOG}	logarithmic input voltage range	V_{IN} = 1 mV_{pp}, RSSI step = high	0.3		300	mV
S_{RSSI}	RSSI slope in log. range	RSSI step = high		12		mV/dB
C_{RSSI}	cap. loading of RSSI pin	RSSI buffer active			10	pF
I_{RSSI}	RSSI buffer output current				5	µA
T_{step}	RSSI voltage step time[13]	C_L = 10 pF, R_L = 1 MΩ; Input signal amplitude 100 mVpp; CS from low to high (Buffer activation in presence of a strong input signal);			350	µs
		C_L = 10 pF, R_L = 1 MΩ; channel switching from ChA(100 mVpp) to ChB (0 mVpp)[14], with CS deactivation of 10 µs			350	µs
V_{RIP}	RSSI Ripple Voltage	RSSI buffer active, C_L = 10 pF, R_L = 1 MΩ; V_{IN} = 1 mV_{pp};		70		mV
Serial Programming Interface						
V_{IL}	Digital input L level	Pins SCL, SDA, CS; V_{REG} = 2.4 V to 3.5 V[11]			0.3 * V_{REG}[11]	V
V_{IH}	Digital input H level	Pins SCL, SDA, CS V_{REG} = 2.4 V to 3.5 V[11]	0.7 * V_{REG}[11]			V
I_{IH}	Digital Input current	Pins SCL, SDA, CS V_{IH} = 2.4 V; V_{REG} = 2.4 V to 3.5 V[11]	30	60	100	µA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCLK	Clock period	V_{REG} = 2.4 V to 3.5 V[11]	2			µs
TCH	Clock high duration	V_{REG} = 2.4 V to 3.5 V[11]	500			ns
TCL	Clock low duration	V_{REG} = 2.4 V to 3.5 V[11]	500			ns
TDVCH	Data valid to pos. Clock edge	V_{REG} = 2.4 V to 3.5 V[11]	100			ns
TCHDI	pos. Clock edge to Data invalid	V_{REG} = 2.4 V to 3.5 V[11]			100	ns
TSHCH	Select active to pos. Clock edge	V_{REG} = 2.4 V to 3.5 V[11]	100			ns
TCHSL	pos. Clock to Select inactive	V_{REG} = 2.4 V to 3.5 V[11]	100			ns
TSL	Select low time	V_{REG} = 2.4 V to 3.5 V[11]	500			ns

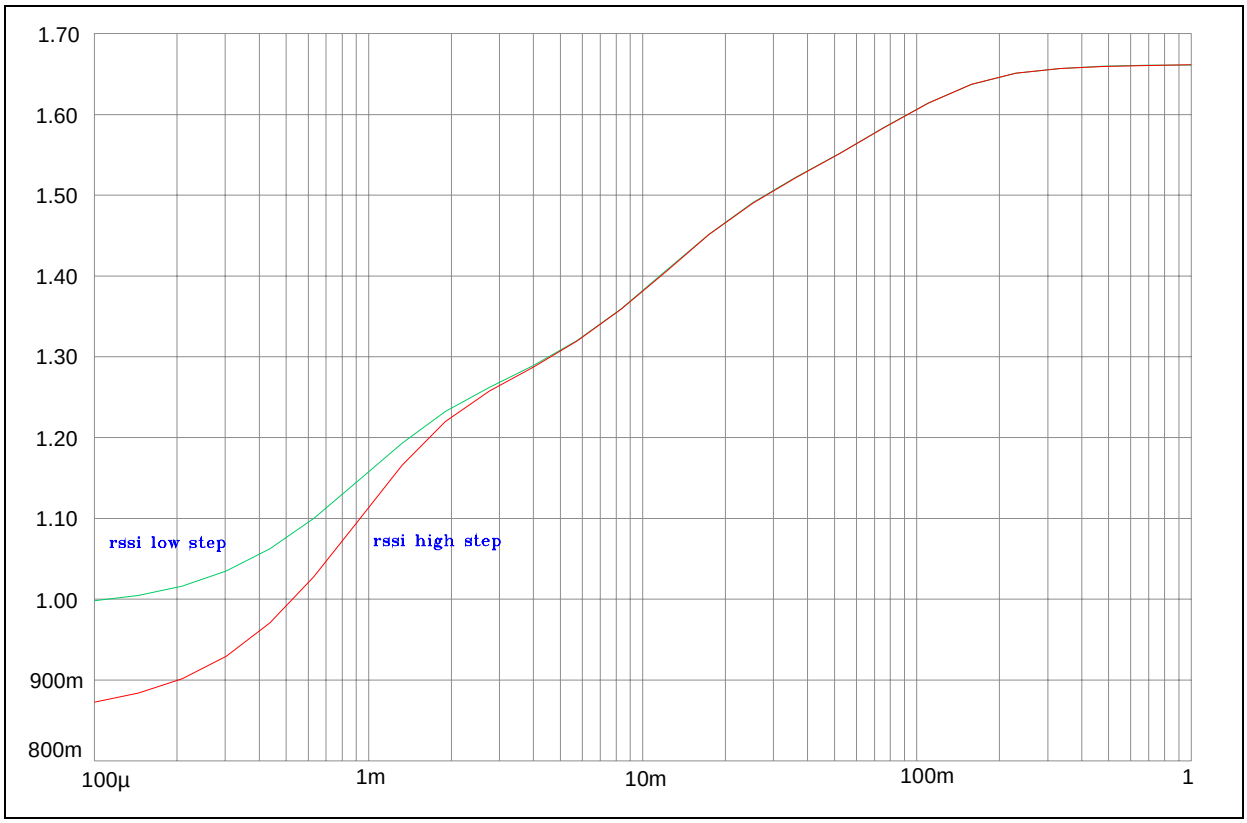
1. The half-bit rate correlates with the crystal oscillator clock frequency f_{clk} as follows: $B_R = f_{CLK}/12$
2. The Manchester bit rate correlates with the Half-Bit Rate as follows: $B_M = B_R/2$
3. Code word can be changed by metal option
4. 8 preamble half-bits are equivalent to 4 manchester bits
5. VREG output may not be used as a supply for other circuits
6. This is the internal Power on Reset time generated by the chip. To ensure proper start-up conditions, the supply voltage VCC must be ramped up to its final value during TPOR
7. This is the additional operating current when the RSSI buffer is activated without load
8. ΔV_{CC} means a *hard step of the supply voltage down to a lower value by an amount of* ΔV_{CC}; after such a step, the analog circuits in the chip take some time to recover for working properly again. The maximum step value is listed.
9. Crystal tolerance: 100ppm
10. Values refer to production test
11. If regulator is on, then V_{REG} = 2.4 V; If regulator is off, then $V_{REG} = V_{CC}$, where V_{CC} = 2.4 V to 3.5 V
12. The RSSI step is the change of the RSSI output voltage when the input signal amplitude changes from 0 to specified value
13. Time to step from initial RSSI value to 95% of the final value
14. ChA may be any channel 1 – 3, whereas ChB may be any other remaining channel.

7 Typical Operating Characteristics

All graphs refer to Tab = 27°C and VREG = 2.4 V, unless otherwise stated.

RSSI Characteristic

Figure 3. RSSI-Characteristic VRSSI [V] vs Vin [Vpp]



Temperature Dependence of RSSI

Figure 4. RSSI-step [V] @ Vin = 1 mVpp and 2 mV vs temp [deg C]

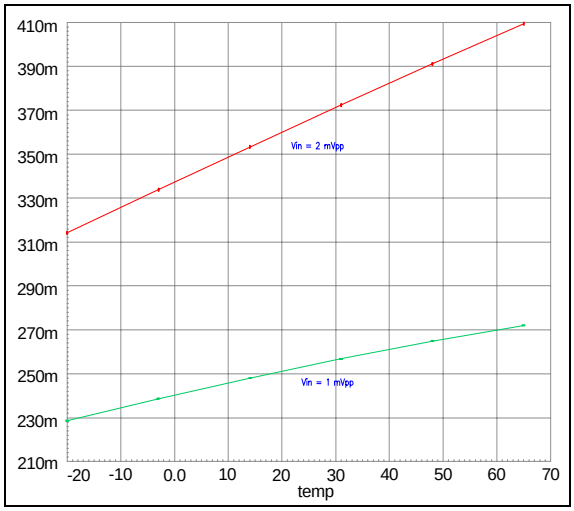


Figure 5. RSSI-step [V] @ Vin = 300 µVpp and offset vs. temp [deg C]

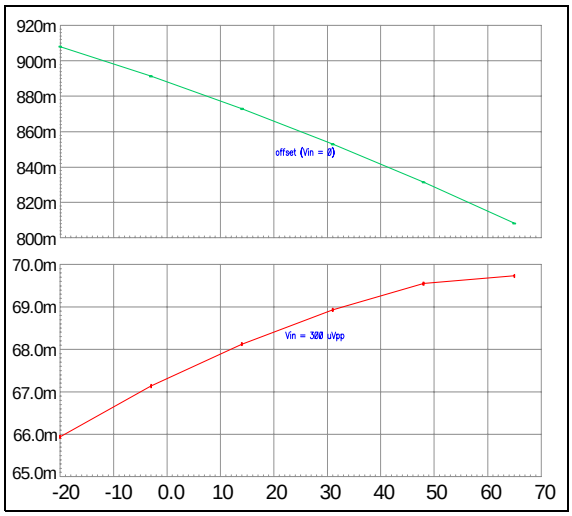


Figure 6. RSSI-step [V] @ Vin = 1 mV and 2 mV vs. temp [deg C], reduced step

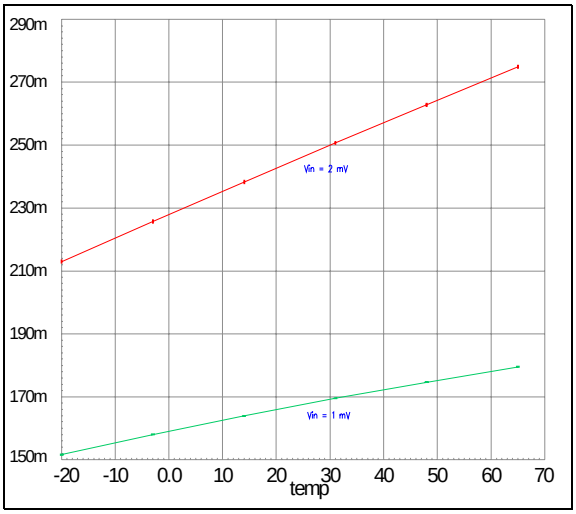
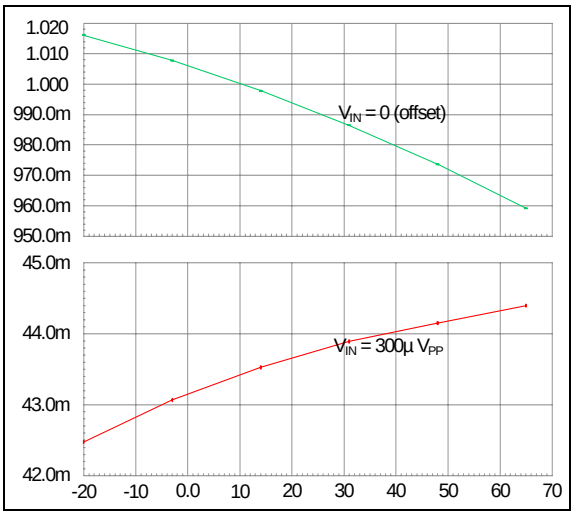


Figure 7. RSSI-step [V] @ Vin=300µ Vpp and offset vs. temp [deg C], reduced step



Supply Voltage Dependence of RSSI

Figure 8. RSSI-step [V] @ Vin = 1 mVpp and 2 mV vs. VCC [V]

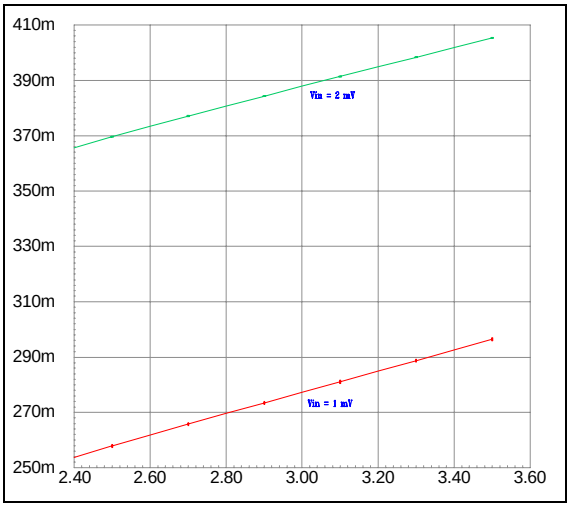


Figure 9. RSSI-step [V] @ Vin = 300 µVpp and offset vs. VCC [V]

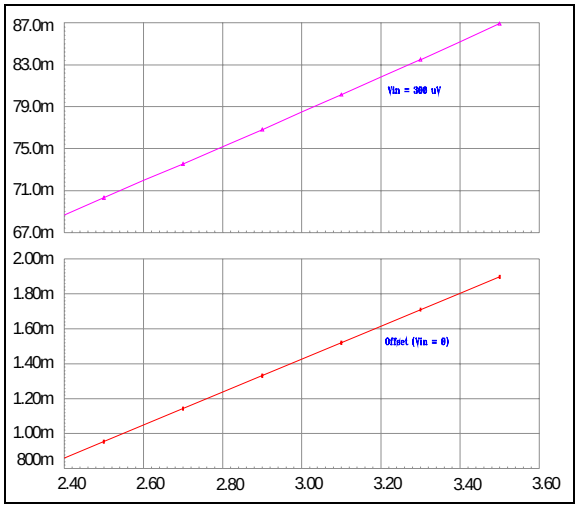


Figure 10. RSSI-step [V] @ Vin = 1 mVpp and 2 mV vs VCC [V],reduced step

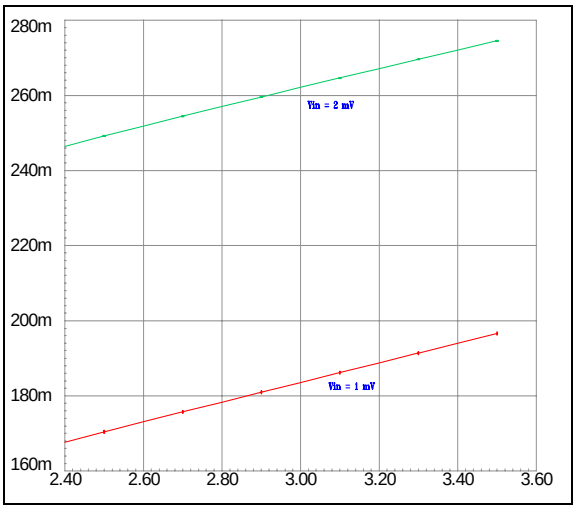
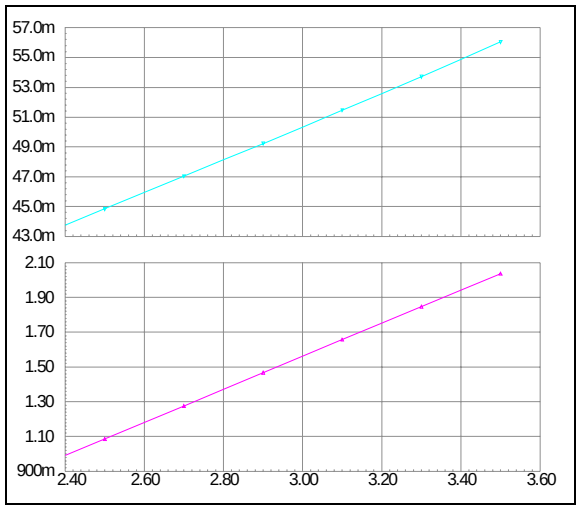
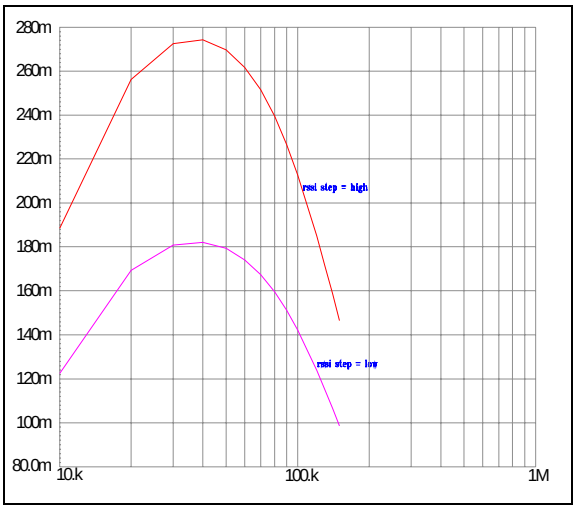


Figure 11. RSSI-step [V] @ Vin =300 µVpp and offset vs. VCC [V], reduced step



Frequency Dependence of RSSI

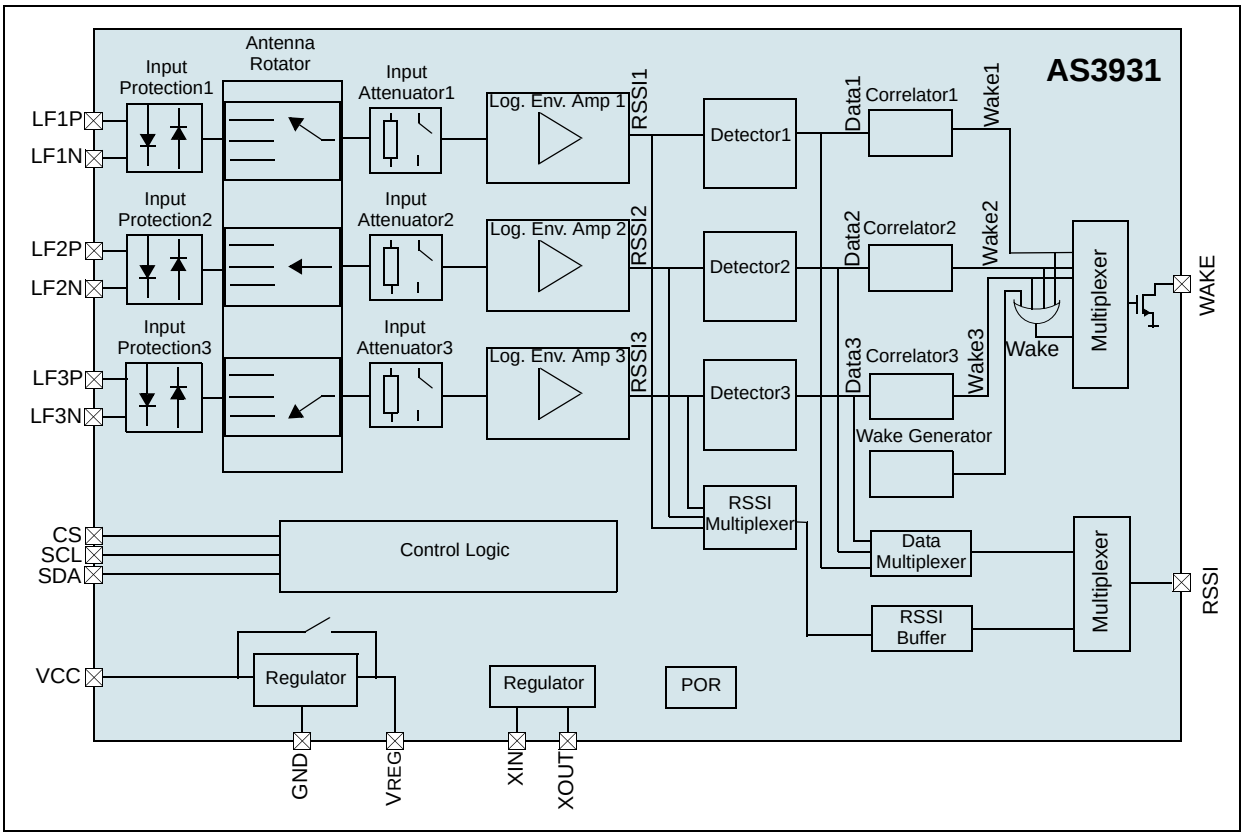
Figure 12. RSSI-step [V] @ Vin = 1 mVpp vs. fin [Hz],
RSSI high step and low step



8 Detailed Description

Block Diagram

Figure 13. Block Diagram



Block Description

Antenna Rotator

In order to achieve an optimum assignment of the antennas to the receiving channels, the connection of the antennas to the channels can be changed cyclically with a multiplexed (antenna rotator), which is controlled by an internal register. The register setting can be changed by the serial interface.

Input Attenuator

Input signal attenuation is provided for each channel by means of connecting a 1.5 kΩ resistor across the differential inputs. An internal register controls attenuation.

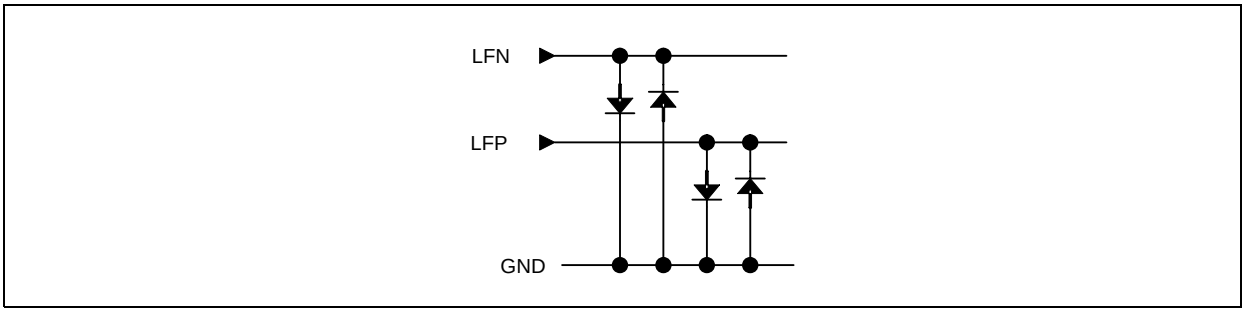
Input Shortcutting

The differential inputs can be shortened by register settings to measure the RSSI offset. In this case, the resistance between the differential inputs is reduced to approximately 500 Ω.

Input Protection Circuit

Each signal input has a powerful input overload protection circuit consisting of two anti-parallel protection diodes connected to ground (see Figure 14). This connection ensures that the differential input voltage can never exceed the supply voltage of the chip. To obtain proper operation, the differential input receiving circuits (resonant RLC-circuits) must be floating and shall be grounded nowhere (see Figure 1)

Figure 14. Input Protection Circuit



Logarithmic Envelope Amplifiers

The logarithmic envelope amplifiers amplify the ASK coded LF input signals. They generate Received Signal Strength Indicator (RSSI) signals, which are proportional to the logarithm of the received field strengths within the specified dynamic range. These signals are used for data detection and distance measurements. The RSSI signals are bandwidth limited to reduce noise influence. The slope of the amplifiers in the low signal range can be controlled by register settings: a high slope for increased sensitivity but also increased current consumption and a weak slope with reduced current consumption are possible.

Detectors

The detectors convert the logarithmic envelope signal containing ASK coded data into digital signals. Each detector consists of a lowpass filter for generation of an adaptive threshold and a slicing comparator. A preamble is required for a proper adaptation of the threshold prior to the decision of the first valid data bit. A constant positive threshold offset is included in the comparator to ensure no data output in case of no input signal. This increases the overall system noise immunity.

Digital Correlators

The AS3931 uses a 16-bit digital wakeup pattern. Digital correlators perform the identification of this pattern. They use a sophisticated detection algorithm that provides high immunity against noise injection as a result of stochastic and periodic interference's. The AS3931 provides the possibility to double the length of the wake pattern to 32 bit. This is useful in environments with high noise levels to reduce the possibility of spurious (parasitic) wakeups. In this case the usual wake pattern must be sent twice before a wake up is recognized and a WAKE signal is generated. This active low WAKE signal is generated after successful pattern identification. Otherwise WAKE is high. Setting a register bit via the serial-programming interface resets the correlators. In order to save power the correlators are stopped when no data has been received for a specified amount of time. The correlators can be configured regarding their error tolerance by register settings.

Wake Generator

A counter, clocked by the 32 kHz crystal oscillator, generates an artificial wake up app. every 2 hours. This wake up can be used to manage the quiescent current consumption of the AS3931. The idea behind is, to switch off one or more of the receiving channels in case of no true wake up detection for long times; that is when only parasitic wakeups or no wakeup at all is detected. An external controlling unit (µC) can identify this case by counting the parasitic wake ups and powering down one or more of the receiver channels to save current. When no wake ups are detected at all, e.g. if the application device is stored in a stock, then the wake generator's artificial parasitic wakeups (every 2 hours) can be used to identify the situation.

Crystal Oscillator

The crystal oscillator generates the clock signal for the digital correlators. It has been optimized for a 32.768 kHz quartz crystal connected to pins XIN and XOUT. The oscillator provides extremely low current consumption, so it can be operated permanently by a battery.

Regulator

A regulator is implemented to provide the amplifiers and digital circuits with a stable and clean supply. The regulator can be switched off; in this case the external supply voltage is bypassed to the amplifiers and digital circuits. The regulator shall always be used for external supply voltages higher then 3.3V, otherwise the current consumption is significantly increased. The regulated voltage can be seen at the VREG pin, but may not be used to supply any other external circuits.

Power On Reset (POR)

A power on reset circuit guarantees proper circuit operation after power supply starts up. All internal registers are reset to their default states after power on. After the Power On Reset time, the active low WAKE output is activated and set to low (Power On Wake Up). During the Power On Reset time, the WAKE output pin is set to high. By this, it is ensured that this triggers the Power On Wake Up triggered only when the internal registers are reset and ready to be programmed.

Basic Operation

LF Transmission Protocol

Data Pattern

The AS3931 identifies a 16 half-bit binary coded data pattern, which is ASK-modulated on a LF carrier. The pattern must contain 8 LOGIC 0 half-bits and 8 LOGIC 1 half-bits in order to be DC free. Furthermore, for a proper detector threshold adaptation it has to be ensured that there are no long groups of LOGIC 0 and LOGIC 1 half-bits. Therefore coding of the 16 half-bit binary data to 8 Manchester bits is common. This means that 8 consecutive half-bit pairs are grouped to Manchester bits whereas a Manchester bit 1 is a HIGH to LOW transition and a Manchester bit 0 is a LOW to HIGH transition. The AS3931 supports the Manchester bit pattern 96 [hex] which in binary code is: 10 01 01 10 01 10 10 01. MSB is transmitted first. The Manchester bit pattern i.e. the binary DATA pattern can be changed on demand by a metal mask modification.

Double Data Pattern

To increase the immunity against parasitic wakeups, the data pattern necessary for a successful wakeup can be doubled by programming the AS3931: if the double data pattern is used, the pattern 96 has to be sent twice; after recognition of the first data pattern, the second data pattern has to be sent immediately after the first one, otherwise no WAKE signal is generated. For the timing see Wake Up Frame on page 15. Setting the bit M1 to 1 can program the double data pattern feature.

Wake Up Frame

The Wake Up Frame of AS3931 consists of a preamble used for detector threshold adaptation followed by the DATA pattern once (normal or single Wake Up) or twice (double Wake Up) to be identified. We recommend a transmission protocol as shown on Figure 15 and Figure 16. The preamble consists of a half-bit pattern 1010... with a specified number N_{PRE} of half-bits (N_{PRE} must be an even number in order to get complete 1/0 pairs). N_{PRE} depends on the application and has influence on the wakeup and overload sensitivity. We recommend a minimum of N_{PRE} = 8 half-bits (according to 4 manchester bits “1”).

Figure 15. Wake Up Frame of AS3931 *with Single WAKE Data Pattern*

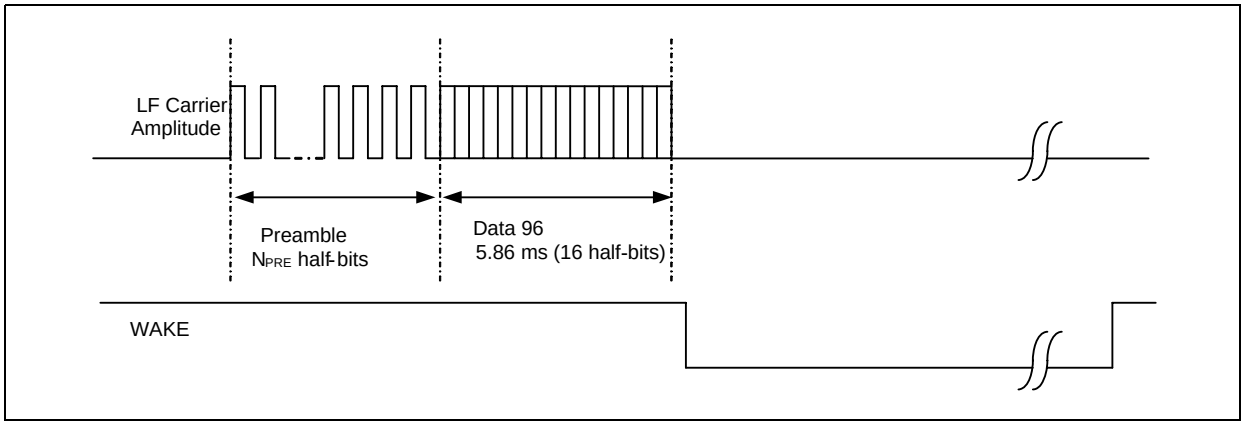
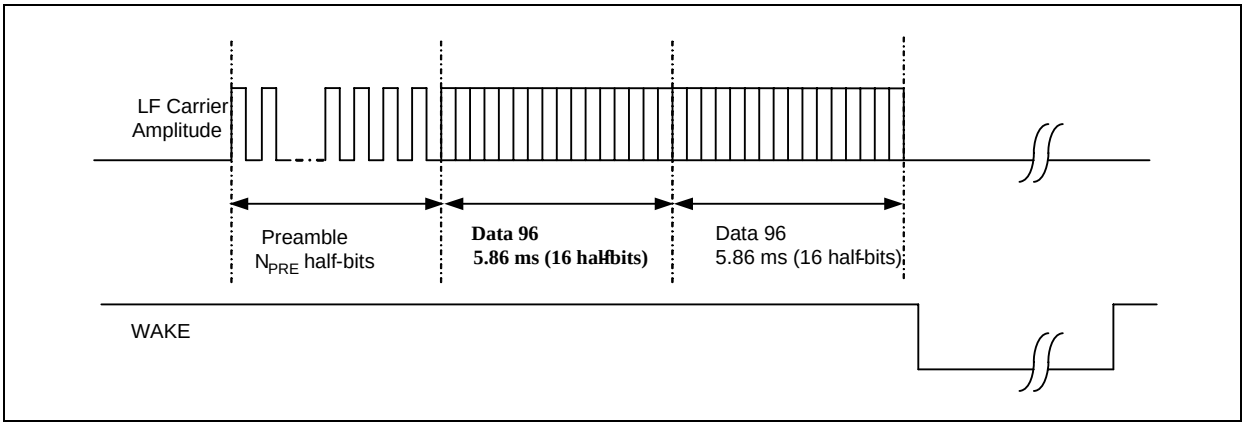


Figure 16. Wake Up Frame of AS3931 *with Double WAKE Data Pattern*



Wake Up Detection

A WAKE signal is generated if and only if all 8 LOGIC 1 half-bits and a predefined number of LOGIC 0 half-bits have been identified as correct. The wakeup detection criteria can be changed: the number of invalid zero half-bits can be programmed from 0 to 3. A valid Wake Up Frame can be detected at only one of the 3 channels or at more then one channel simultaneously. The single WAKE signals of each channel are ored together to a common WAKE signal Figure 13.

In case of using the double wake up feature, the settings of the allowed zero half-bit errors apply for each of the sent data pattern individually. E.g. if you configure the AS3931 to allow 2 zero half-bit errors, the first data pattern can contain up to two invalid zero half-bits as well as the second data pattern, but it is not possible that the first pattern contains 3 and the second data pattern contains one zero half-bit error (what in total would give the same number of allowed zero half-bit errors as before). Note that a Double-Wake-Pattern detection is possible also if the two consecutive Single-Wake-Patterns are assigned to different channels: e.g. if the first pattern is recognized at channel 2 and the second pattern is recognized at channel 3, then a Double-Wake-Pattern is recognized and the WAKE Pin is activated. All channel combinations are possible. In case of different channels, it is not possible to decide which channel received the first and which channel received the second data pattern.

WAKE Signal Clearing

After a Wake Up detection, the WAKE output signal must be reset via the Serial Programming Interface. This is done by toggling the bit C5 in the Channel Select register from low to high and vice versa. This is valid for both cases the Single Wake pattern and the Double Wake pattern detection. Furthermore, it is also valid for an internal generated Artificial Wakeup (see Extended Operation on page 25).

WAKE Signal After POR

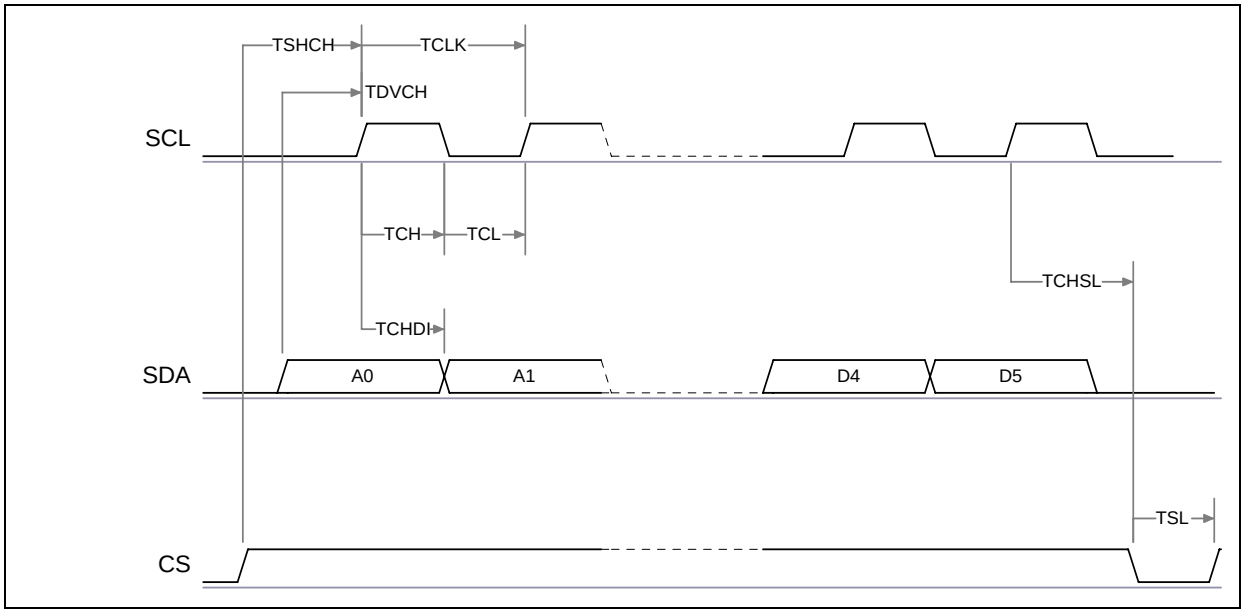
After a power on reset (POR), the WAKE signal is activated (LOW). Therefore, after startup the WAKE signal must be cleared as if a valid Wake Up would have been detected.

RSSI Operation

The RSSI signal of a selected channel can be measured at the RSSI pin. Each channel can be selected by register settings. To calibrate the RSSI measurement, the LF inputs can be shortcutted with approximately 500 Ω by internal register settings. Doing so, the RSSI voltage offset can be measured. The RSSI – signal is buffered at the RSSI pin. The buffer can be deactivated by register settings; in this case the RSSI pin is tristated (high impedance). However, if the CS signal is not activated, the RSSI pin is tristated. This has to be kept in mind when programming the AS3931 via the Serial Programming Interface (the CS signal is used to latch the serial data into the selected register at the falling edge of CS).

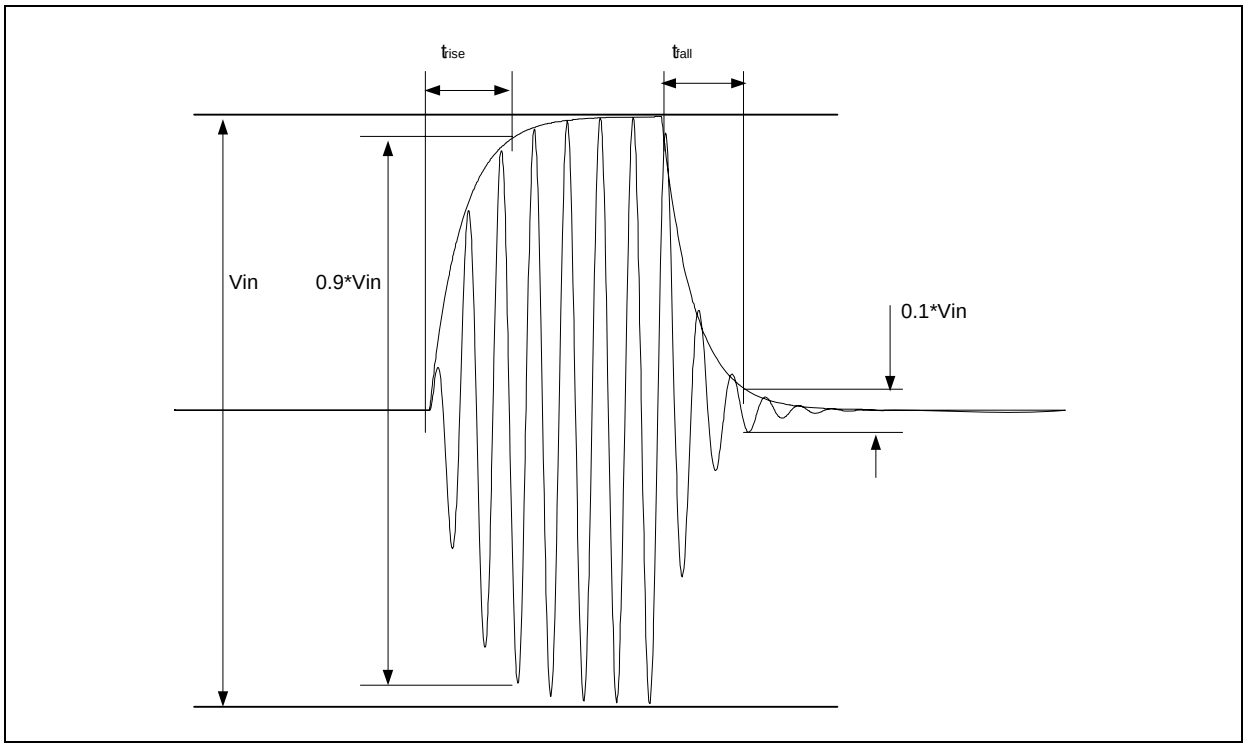
Serial Programming Interface Timing

Figure 17. SPI Timing Waveforms



Input Signal Waveform Definition

Figure 18. Input Signal Waveform



9 Configuring the Product

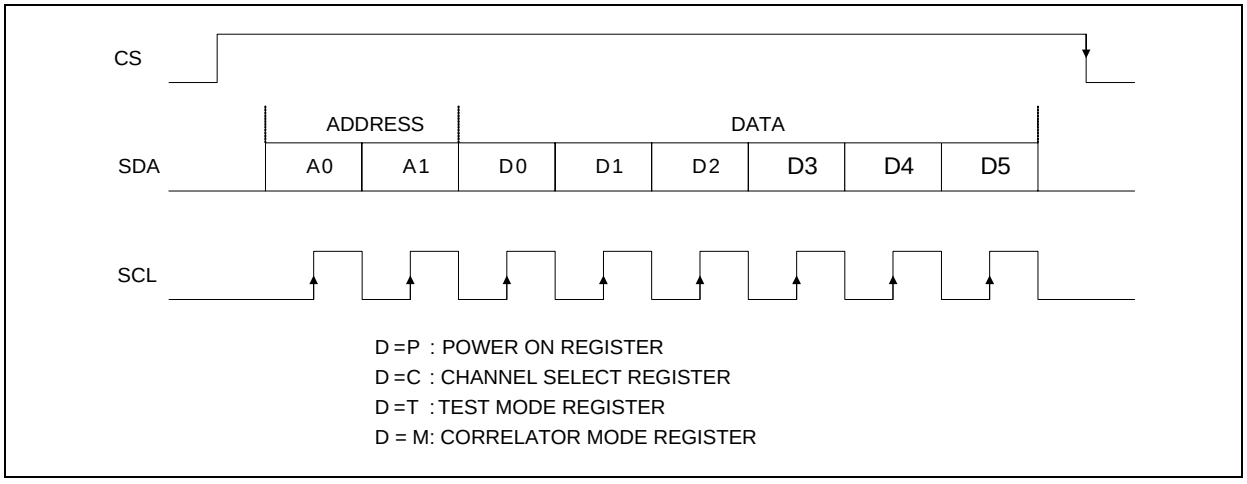
Serial Programming Interface

The AS3931 is programmed via an unidirectional three wire Serial Programming Interface.The 3 lines are:

- **CS:** Chip Select, used for selecting AS3931 and for data latching
- **SCL:** Serial Clock
- **SDA:** Serial Data

A block of 8 bit data starting with the LSB is sent according to the diagram shown in Figure 19. The received block of 8 bit data is shifted into an 8 bit latch. The two LSBs are register address bits and the remaining 6 bits are data bits. The register address bits A1 and A0 are decoded and the 6 data bits are stored into one of three 6 bit registers with the falling edge of CS.

Figure 19. Protocol of 8 Bit Data Serial Transmission



Power On Register

Table 4. Register Data

Bit	POR state	Description
P0	1	Enable Channel 1
P1	1	Enable Channel 2
P2	1	Enable Channel 3
P3	1	Enable Regulator
P4	0	Antenna Rotator Bit 1
P5	0	Antenna Rotator Bit 2

Table 5. Register Address

Bit	Value
A0	0
A1	0

P0, P1, P2 (Channel Enable)

If the bit P0, P1 or P2 is set to 1, the related channel is enabled. That means, the logarithmic envelope amplifier and the correlator are enabled and ready to receive a Wake Up Frame. When disabled, the channel is off, taking no current except for the bias cell to the amplifier. After a power on, all channels are enabled.

Note: Shaded cells show POR-states

Table 6. P0, P1, P2 Bit Mode

P0, P1, P2	Mode
0	Channel Disabled
1	Channel Enabled

P3 (Regulator Enable)

Bit P3 enables the regulator (VREG 2.4 V) or switches off the regulator (VREG = VCC). If the regulator is switched off, then the voltage at Pin VCC is bypassed unregulated to the internal circuits. After a power on, the regulator is on.

Table 7. P3 Bit Mode

P3	Mode
0	Regulator Disabled
1	Regulator Enabled

P4, P5 (Antenna Rotator/Input Shortcut)

Bits P4 and P5 are used to set the Antenna Connection Mode or to shortcut the differential inputs of each amplifier. See Table 28 for the description of the rotator modes.

Table 8. P4, P5 Bit Mode

P4	P5	Mode
0	0	Connection Mode1
0	1	Connection Mode2
1	0	Connection Mode3
1	1	Amplifier Inputs Shorted

Table 9. Antenna Rotation Modes

Connection Mode1	Connection Mode2	Connection Mode3
Antenna 1 → Channel 1	Antenna 2 → Channel 1	Antenna 3 → Channel 1
Antenna 2 → Channel 2	Antenna 3 → Channel 2	Antenna 1 → Channel 2
Antenna 3 → Channel 3	Antenna 1 → Channel 3	Antenna 2 → Channel 3

RSSI Channel Select Register

Table 10. Register Data

Bit	POR state	Description
C0	0	RSSI select Bit 1
C1	0	RSSI select Bit 2
C2	0	RSSI output mode Bit 1
C3	0	RSSI output mode Bit 2
C4	0	Channel attenuator
C5	0	WAKE clear

Table 11. Register Address

Bit	Value
A0	1
A1	0

C0, C1 (RSSI Channel Select)

Bits C0 and C1 are used to select the channel whose RSSI signal is multiplexed to the RSSI pin. In case of both bits C0 and C1 set to 1, a bandgap voltage VBG (1.25 V) appears at the RSSI pin. After power on, channel 1 is selected.

Table 12. C0, C1 Bit Mode

C0	C1	Mode
0	0	Channel 1
1	0	Channel 2
0	1	Channel 3
1	1	VBG (T0=0), WAKE (T0=1)

C2, C3 (RSSI Output Mode)

Bits C2 and C3 define the RSSI pin function.

Table 13. C2, C3 Bit Mode

C2	C3	RSSI Pin Function
0	0	high Z
1	0	Analog output: RSSI of selected channel or VBG
0	1	Digital output: WAKE, single WAKE or DATA
1	1	not used

Note: The RSSI pin function also depends on the signal CS. If CS = 0, the RSSI pin is always in the high impedance state. This is also the case after power on.

The WAKE or single WAKE function is selected together with bits T0 – T2 and C0 – C1. For more information see Extended Operation on page 25

C4 (Channel Attenuator)

When bit C4 is set, a resistor (app. 1.5 kΩ) is connected across the differential inputs of each channel. This resistor reduces the Q-factor of the antenna resonant circuit; therefore the received signal is reduced too. The amount of damping depends on the Q-factor of the antenna circuit.

Table 14. C4 Bit Mode

C4	Mode
0	Input attenuators disabled
1	Input attenuators enabled

C5 (WAKE Clear)

Bit C5 is used to reset the active low WAKE pin after the pin has been set as a result of receiving a valid code word (single or double wake pattern) by one of the 3 channels, a POR or an internally generated Wakeup. Setting Bit C5 to 1, the WAKE pin is reset to high and held in high state, to enable the channels for the next wake up signal, the bit C5 must be toggled to 0 afterwards. After power on, the WAKE-pin is activated and the bit C5 has to be toggled high and low after a power on.

Table 15. C5 Bit Mode

C5	Mode
0	no effect
1	WAKE=H

Test Mode Register

Table 16. Register Data

Bit	POR state	Description
T0	0	Test mode enable
T1	0	Test mode select Bit 1
T2	0	Test mode select Bit 2
T3	0	not used
T4	1	RSSI step
T5	0	WAKE Generator on/off

Table 17. Register Address

Bit	Value
A0	0
A1	1

T0 (Test Mode Enable)

Bit T0 is used to define the pin function of the WAKE pin. When bit T0 is reset to 0, the WAKE pin is used for normal Wake Up detection (Single or Double Wakeup from the receiver channels or internally generated wakeup). When bit T0 is set to 1, testmode signals are multiplexed to the WAKE pin according to the selected test mode (T1, T2). After power on, the normal wake up detection mode is selected.

Table 18. T0 Bit Mode

T0	WAKE Pin function
0	WAKE
1	Test Mode Signals

T1, T2 (Test Mode Select)

When bit T0 is set to 1, the following signals can be mapped to the WAKE pin. For signal description (see Figure 13).

- DATA: received bit stream of the selected channel
- WAKE: detected wake up of the selected channel

For the DATA and WAKE signal select the desired channel by setting Bits C0 and C1.

Table 19. T1, T2 Bit Mode

T1	T2	WAKE Pin Function
0	0	DATA of selected channel
1	0	WAKE of selected channel
0	1	not used
1	1	not used

T3

Not used; must always be programmed to 0 by the user!

T4 (RSSI Step Select)

Bit T4 is used to switch between a high and a low RSSI step. For more information on RSSI steps see Extended Operation on page 25.

Table 20. T4 Bit Mode

T4	Mode
0	Low RSSI step
1	High RSSI step

T5 (Wake Generator On/Off)

Bit T5 is used to activate the Wake Generator. If activated, an artificial parasitic wakeup is generated every 2 hours.

Table 21. T5 Bit Mode

T5	Mode
0	Wake Generator off
1	Wake Generator on

Correlator Mode Register

Table 22. Register Data

Bit	POR state	Description
M0	0	Correlator Off
M1	0	single/double wake pattern
M2	0	Zero-Bit Detection Mode bit1
M3	1	Zero-Bit Detection Mode bit2
M4	1	detector threshold τ select
M5	0	not used

Table 23. Register Address

Bit	Value
A0	1
A1	1

M0 (Correlator Off)

Bit M0 is used to simultaneously turn off all 3 correlators. This is done by turning off the correlator clocks. This can be used to reduce power consumption when the Direct Data Mode is used.

Table 24. M0 Bit Mode

M0	Mode
0	Low RSSI step
1	High RSSI step

M1 (Single/Double Wake Pattern)

Bit M1 selects the number of data patterns that are necessary for wakeup detection.

Table 25. M1 Bit Mode

M1	Mode
0	Single Data pattern
1	Double Data pattern

M2, M3 (Zero-Half-Bit Detection Mode)

Bits M2 and M3 select the number of Zero-Half-bits that are allowed to be invalid. A high level of allowed invalid Zero-Half-bits increases the error tolerance related to noise or interference's, that means that the probability for the detection of a valid WAKE pattern increases. Note that in turn the immunity against parasitic wakeups (WAKE detection when no data has been sent, due to noise or interference's) is reduced.

Table 26. M2, M3 Bit Mode

M2	M3	WAKE Pin Function
0	0	3 invalid Zero-bits allowed
1	0	2 invalid Zero-bits allowed
0	1	1 invalid Zero-bits allowed
1	1	0 invalid Zero-bits allowed

M4 (Detector Time Constant)

Bit M4 is used to switch between a large and a small τ of the detector threshold adoption filter. A large τ is recommended, because it increases the noise margin. A small τ can be used to improve the wake sensitivity when non-specified wake-patterns are used.

Table 27. M4 Bit Mode

M4	Mode
0	small τ
1	large τ

M5

Not used; must always be programmed to 0 by the user!

10 Extended Operation

Power Management

Sleep Mode

In sleep mode, all channels are switched off, taking no current except for the bias cells of the amplifiers. Sleep mode is entered by register setting, bits P0, P1, P2 set to 0. The remaining elements that take current are the oscillator and the regulator (if used). The Serial Programming Interface remains active also in the sleep mode.

Standby Mode

In standby mode, selected channels are switched on, ready to receive data. The amplifier of the selected channel is on, whereas the correlator is powered down as long as no input signal is detected at the input. Enabling the related channel when setting bits P0, P1 or P3 enters the standby mode. In the standby mode, the current consumption increases by the amplifier currents compared to the sleep mode.

Receive Mode

An enabled channel automatically changes from the standby mode to the receive mode as soon as an input signal is detected. The channel stays in receive mode as long as an input signal is detected. In receive mode, the correlator of the channel is active, scanning the input signal waveform for a valid wake up pattern. The channel goes back to standby mode if no input signal is detected for more then a fixed timeout period. The timeout period is approximately 3.3 ms. by this operating principle it is guaranteed, that the correlators are only active and taking current as long as it is really necessary.

Regulator On/Off

The regulator can be switched off to reduce the current consumption. When switching off, the supply voltage is bypassed unregulated to the internal circuits, so VREG = VCC. Otherwise, the internal voltage is regulated to 2.4 V. Switching off the regulator saves about 1 µA of current. The regulator should only be switched off, when VCC is not higher then 3.3 V, otherwise the current consumption is increased because the internal circuits will then take more current.

Typical Current Consumption in Different Modes

The Table 28 gives an overview of the typical current consumptions in the different modes. All three channels are used in this case. Power consumption of course can be further reduced when not all three channels are enabled.

Table 28. Typical Current Consumption

Operating Mode	Regulator on, VCC = 3 V	Regulator off, VCC = 2.4 V
Sleep	0.8 µA	0.3 µA
Standby	7.0 µA	6.5 µA
Receive	7.2 µA	6.8 µA
Standby & RSSI low step	6.6 µA	6.1 µA

RSSI Step

The RSSI step is defined as the change in the RSSI signal voltage if the input amplitude steps from zero to a defined (small) value. For example when changing the input signal amplitude from zero to 1 mVpp, the RSSI signal makes a step of app. 175 mV if the bit T4 is set to 1 (compare to Figure 8 on page 21). If not needed, this step can be reduced to a lower value (T4 = 0), which decreases the current consumption of each channel by app. 120 nA.

Antenna Rotation

The 3 possible input signals can be distributed to the 3 channels in 3 different connection modes. Using this feature, the differences between the individual antenna voltages and also the differences of the individual RSSI-voltages of the channels can be handled. For example to eliminate the differences of the RSSI-voltages it is possible to use only one channel and to multiplex it to each antenna. The Bits P4 and P5 select the Antenna Rotation Modes.

Input Attenuation and Input Shortcutting

All differential LF-inputs are each shorted by approximately 500 Ω when setting Bits P4 and P5 both to 1. This can be used to measure the RSSI-voltage with no input signal present; therefore the RSSI offset can be calibrated. It should be taken into account that the shortcut resistance can not be made zero due to design restrictions, so the input signal cancellation is not 100% (depending on the antenna circuit).

Similar to the input shortcutting option, a 1.5 kΩ resistor can be connected across the differential inputs when setting bit C4 to 1. This input attenuation allows handling of very strong input signals by damping the antenna circuit. The damping depends on the Q-factor of the receiver circuits.

WAKE Signal at the RSSI Pin

The WAKE signal, which is normally available at the WAKE pin, can be mapped to the RSSI pin additionally, which then becomes a digital output. To do this, set the following bits:

C3 = 1 and C2 = 0 in the Channel Select Register (RSSI output mode digital)

C0 = 1 and C1 = 1 in the Channel Select Register

Note: The RSSI pin is only active if the CS signal is active (CS = 1), otherwise RSSI is high Z.

Single WAKE Operation

The single WAKE signals of each channel can be mapped to the WAKE pin. Normally, the 3 WAKE signals are “ored“ together and mapped to the WAKE pin, so the channel with the strongest input signal will generate a WAKE signal. To map a single WAKE signal to the WAKE pin, follow the steps:

1. Enable Test Mode: set T0 = 1 in Test Mode Register
2. Select Test Mode: set T1 = 1 and T2 = 0 in Test Mode Register
3. Select Channel: set C0 and C1 in the Channel Select Register

The single WAKE signals can also be mapped to the RSSI pin, which then becomes a digital output pin. To do this, make this step:

- Select RSSI output mode digital:set C2 = 0 and C3 = 1 in the Channel Select Register

The RSSI pin is only active if the CS signal is active (CS = 1), otherwise RSSI is high Z.

It is possible to operate the WAKE pin in the normal mode first (that is all three single WAKE signals ored together) and after a wake up detection, to use the Single WAKE mode to check which channel received the wake pattern. This must be done before clearing the WAKE pin. It is also possible to operate the WAKE pin in normal WAKE mode and simultaneously to operate the RSSI-pin in single WAKE mode.

Using the Wake Generator

The wake generator generates artificial parasitic wakeup’s every 2 hours as a time base for an external-controlling unit to identify situations where no true wakeup’s can be detected for a long time. For this purpose the external controlling unit must be able to distinguish between a true wakeup (generated by one of the receiving channels) or an Artificial Wakeup. This is done by checking the receiving channels using the single WAKE operation (see Single WAKE Operation on page 26). If a wakeup has occurred and no one of the receiving channels can be identified as the trigger for the wake up, then the Wake Generator has triggered the wakeup. In this case, the WAKE signal has to be cleared as if a receiving channel would have triggered the Wake Up.

Note: The internal counter, that generates the internal wakeup by an overflow, can not be reset by clearing the wake pin or other actions.

The time between two artificial wakeups is approximately 2 hours (2h 16min 32sec); however, the first artificial wakeup generated by the Wake Generator after activation of the feature (by setting bit T5 = 1) may come earlier then in 2:16:32 hours. This time is not defined. After the first artificial wakeup, the time between two wake ups is then 2 hours.

The Wake Generator must be activated by programming the bit T5 = 1 in the Test Mode Register.

Direct DATA Mode

In Direct Data Mode, the received DATA of a selected channel can be mapped to the WAKE pin. The DATA signal is the digital output of the detector and is normally fed to the correlator, where it is scanned for the WAKE pattern (see Figure 13). To get the DATA signal at the WAKE pin, follow the steps:

1. Enable Test Mode: set T0 = 1 in Test Mode Register
2. Select Test Mode: set T1 = 0 and T2 = 0 in Test Mode Register
3. Select Channel: set C0 and C1 in the Channel Select Register

The Direct DATA signals can also be mapped to the RSSI pin, which then becomes a digital output pin. To do this, make this step:

- Select RSSI output mode digital:set C2 = 0 and C3 = 1 in the Channel Select Register

Note: The RSSI pin is only active if the CS signal is active (CS = 1), otherwise RSSI is high Z.

Correlator Modes

Operation of the correlators can be modified regarding the error tolerances for the Zero-Half-Bits. In this case, the number of Zero-Half-Bits that is allowed to be invalid can be set from 0 to 2. Please take into account that an increased error tolerance also reduces the immunity against parasitic wakeups (WAKE detection when no data has been sent, due to noise or interferences).

Threshold Adaptation Filter Time Constant

Bit M4 is used to switch between a large and a small τ of the detector threshold adaptation filter. A large τ is recommended, because it increases the noise margin. A small τ can be used to improve the wake sensitivity when non-specified Wake-Patterns are used.

RSSI and WAKE Pin Modes

This table gives an overview of the different signals that can be mapped to the RSSI and WAKE pin and how to program it.

Table 29. RSSI/WAKE-Pin Modes

Bit/Pin	Chip Select Pin	RSSI Output Mode 2	RSSI Output Mode 1	Channel Select 2	Channel Select 1	WAKE Test Mode Enable	Test Mode Select 2	Test Mode Select 1
Mode	**CS**	**C3**	**C2**	**C1**	**C0**	**T0**	**T2**	**T1**
WAKE-Pin: WAKE	X	X	X	X	X	0	X	X
WAKE-Pin: DATA1	X	X	X	0	0	1	0	0
WAKE-Pin: DATA2	X	X	X	0	1	1	0	0
WAKE-Pin: DATA3	X	X	X	1	0	1	0	0
WAKE-Pin: WAKE1	X	X	X	0	0	1	0	1
WAKE-Pin: WAKE2	X	X	X	0	1	1	0	1
WAKE-Pin: WAKE3	X	X	X	1	0	1	0	1
RSSI-Pin: WAKE	1	1	0	1	1	X	X	X
RSSI-Pin: DATA1	1	1	0	0	0	X	0	0
RSSI-Pin: DATA2	1	1	0	0	1	X	0	0

Table 29. RSSI/WAKE-Pin Modes

Bit/Pin	Chip Select Pin	RSSI Output Mode 2	RSSI Output Mode 1	Channel Select 2	Channel Select 1	WAKE Test Mode Enable	Test Mode Select 2	Test Mode Select 1
Mode	**CS**	**C3**	**C2**	**C1**	**C0**	**T0**	**T2**	**T1**
RSSI-Pin: DATA3	1	1	0	1	0	X	0	0
RSSI-Pin: WAKE1	1	1	0	0	0	X	0	1
RSSI-Pin: WAKE2	1	1	0	0	1	X	0	1
RSSI-Pin: WAKE3	1	1	0	1	0	X	0	1

11 Package Drawings and Markings

The product is available in 16 Pin TSSOP package.

Figure 20. Package Diagram

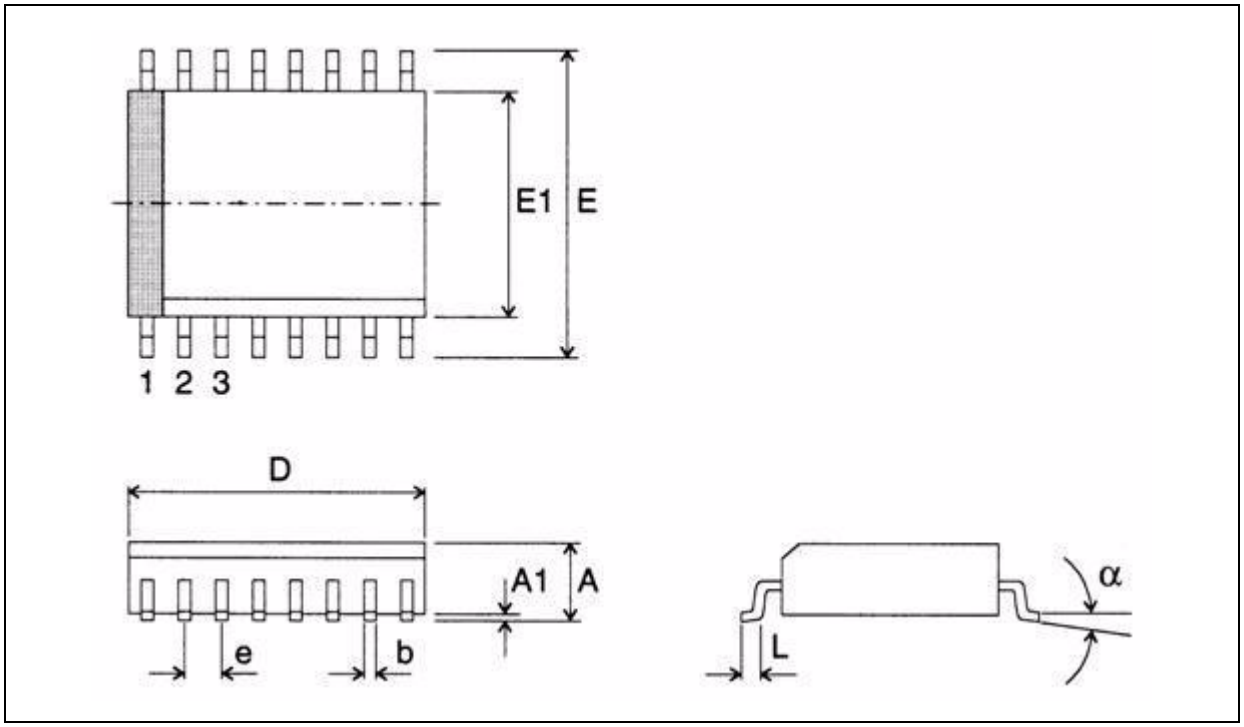


Table 30. Package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	-	-	1.20	E	-	6.40	-
A1	0.05	-	0.15	E1	4.30	-	4.50
b	0.19	-	0.30	L	0.45	-	0.75
D	4.90	-	5.10	∝	0º		8º
e	0.65 BSC						

12 Ordering Information

Table 31. Ordering Information

Part Number	Marking	Description	Delivery Form[1]
AS3931	AS3931	Lead free Package, 16 Pin TSSOP	Tubes
AS3931	AS3931	Lead free Package, 16 Pin TSSOP	Tape and Reel

1. Dry pack sensitivity level = 3, according to IPC/JEDEC J-STD-033A

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