20 V, 6 A, Synchronous, Step-Down DC-to-DC Regulator

Data Sheet **ADP2387**

FEATURES

- Input voltage range: 4.5 V to 20 V
- Integrated MOSFET: 44 mΩ typical/11 mΩ typical
- Reference voltage: 0.6 V ± 1%
- Continuous output current: 6 A
- Programmable current-limit threshold
- Programmable switching frequency: 200 kHz to 1400 kHz
- Precision enable and power good
- External compensation
- Internal soft start with external adjustable option
- Startup into a precharged output
- Supported by ADIsimPower design tool

APPLICATIONS

- Communications infrastructure
- Networking and servers
- Industrial and instrumentation
- Healthcare and medical
- Intermediate power rail conversion
- DC-to-dc point of load applications

TYPICAL APPLICATIONS CIRCUIT

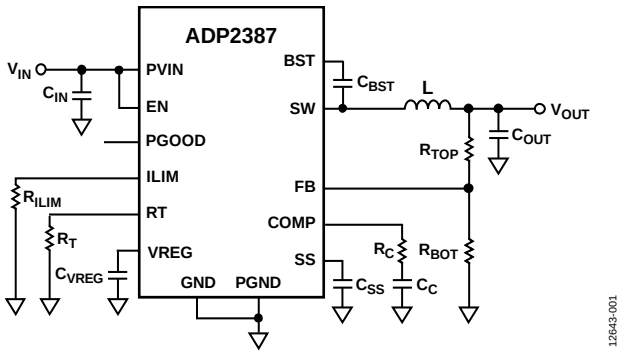

Figure 1.

GENERAL DESCRIPTION

The ADP2387 is a synchronous step-down, dc-to-dc regulator with an integrated 44 mΩ, high-side power, metal oxide semiconductor field effect transistor (MOSFET) and an 11 mΩ, synchronous rectifier MOSFET to provide a high efficiency solution in a compact 4 mm × 4 mm LFCSP. This device uses a peak current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. The switching frequency of the ADP2387 can be programmed between 200 kHz to 1400 kHz.

The ADP2387 requires minimal external components and operates from an input voltage of 4.5 V to 20 V. The output voltage can be adjusted from 0.6 V to 90% of the input voltage and delivers up to 6 A of continuous current. Each IC draws less than 110 µA current from the input source when it is disabled.

This regulator targets high performance applications that require high efficiency and design flexibility. External compensation and an adjustable soft start function provide design flexibility. The power-good output and precision enable input provide simple and reliable power sequencing. The programmable current-limit function allows the inductor to be optimized by output current.

Other key features include undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP), and thermal shutdown (TSD).

The ADP2387 operates over the −40°C to +125°C junction temperature range and is available in a 24-lead, 4 mm × 4 mm LFCSP.

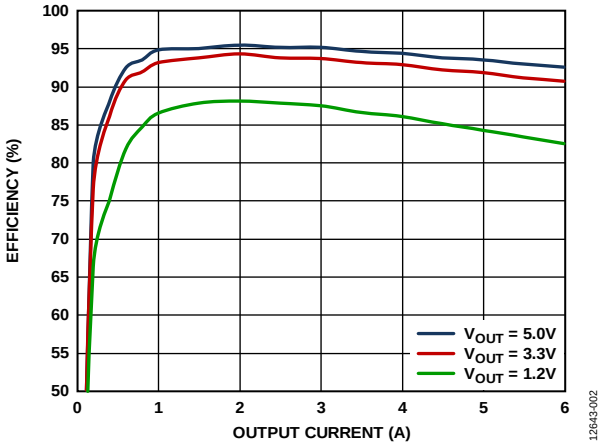

Figure 2. Efficiency vs. Output Current, V_{IN} = 12 V, f_{SW} = 300 kHz

Rev. B
Document Feedback

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COMPARABLE PARTS

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EVALUATION KITS

- ADP2387 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP2387: 20 V, 6 A, Synchronous, Step-Down DC-to-DC Regulator Data Sheet

User Guides

- UG-786: Evaluation Board for the ADP2387 20 V, 6 A Synchronous, Step-Down, DC-to-DC Regulator

DESIGN RESOURCES

- ADP2387 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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1/16—Revision B: Initial Version

FUNCTIONAL BLOCK DIAGRAM

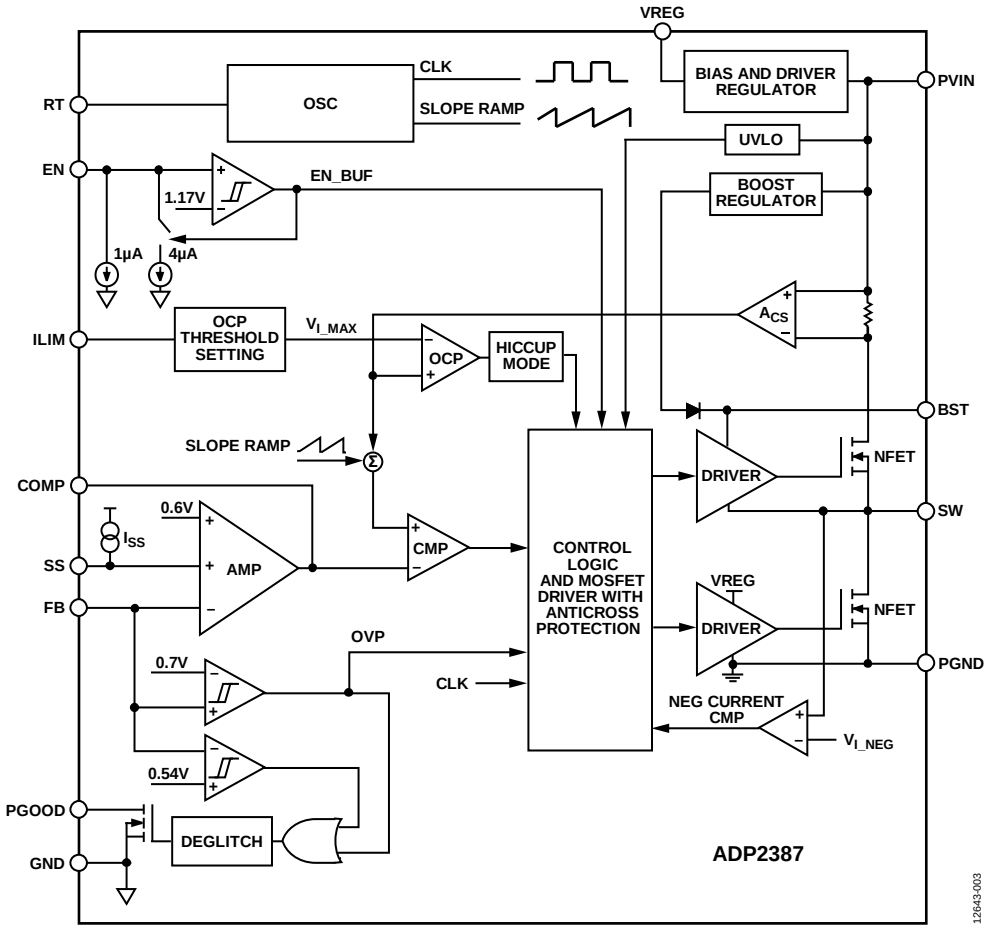


Figure 3. Functional Block Diagram

SPECIFICATIONS

V_{PVIN} = 12 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PVIN						
PVIN Voltage Range	V_{PVIN}		4.5		20	V
Quiescent Current	I_Q	No switching	2.4	2.9	3.6	mA
Shutdown Current	I_{SHDN}	EN = GND	50	80	110	µA
PVIN Undervoltage Lockout Threshold	UVLO	PVIN rising		4.3	4.4	V
		PVIN falling	3.6	3.8		V
FB						
FB Regulation Voltage	V_{FB}	0°C < T_J < 85°C	596.4	600	603.6	mV
		−10°C < T_J < +115°C	595.2	600	604.8	mV
		−40°C < T_J < +125°C	594	600	606	mV
FB Bias Current	I_{FB}			0.01	0.1	µA
ERROR AMPLIFIER (EA)						
Transconductance	g_m		380	480	580	µS
EA Source Current	I_{SOURCE}		40	60	80	µA
EA Sink Current	I_{SINK}		40	60	80	µA
INTERNAL REGULATOR (VREG)						
VREG Voltage	V_{VREG}	V_{PVIN} = 12 V, I_{VREG} = 50 mA	7.6	8	8.4	V
Dropout Voltage		V_{PVIN} = 12 V, I_{VREG} = 50 mA		350		mV
Current-Limit Regulator			62	100	138	mA
SW						
High-Side On Resistance[1]	R_{DSON_HS}	$V_{BST} - V_{SW}$ = 5 V		44	70	mΩ
Low-Side On Resistance[1]	R_{DSON_LS}	V_{VREG} = 8 V		11	18	mΩ
SW Minimum On Time	t_{MIN_ON}			130	165	ns
SW Minimum Off Time	t_{MIN_OFF}			200	260	ns
BST						
Bootstrap Voltage	V_{BOOT}		4.6	5	5.4	V
OSCILLATOR (RT PIN)						
Switching Frequency	f_{SW}	R_T = 100 kΩ	540	600	660	kHz
Switching Frequency Range			200		1400	kHz
CURRENT LIMIT						
High-Side Peak		R_{ILIM} = 44.2 kΩ	7.7	9.2	10.7	A
		R_{ILIM} = 66.5 kΩ	5.1	6.1	7.1	A
		R_{ILIM} = 133 kΩ	2.3	2.9	3.5	A
Low-Side Negative[2]				2.5		A
ILIM Voltage[2]	V_{ILIM}			0.6		V
ILIM Current Range[2]	I_{ILIM}		4		15	µA
SS						
Internal Soft Start				1600		Clock cycles
SS Pin Pull-Up Current	I_{SS_UP}		2.2	3.1	3.8	µA
PGOOD						
Power-Good Range						
FB Rising Threshold		PGOOD from low to high		95		%
FB Rising Hysteresis		PGOOD from high to low		5		%
FB Falling Threshold		PGOOD from low to high		105		%
FB Falling Hysteresis		PGOOD from high to low		11.7		%
Power-Good Deglitch Time		PGOOD from low to high		1024		Clock cycles
		PGOOD from high to low		16		Clock cycles
Power-Good Leakage Current		V_{PGOOD} = 5 V		0.01	0.1	µA
Power-Good Output Low Voltage		I_{PGOOD} = 1 mA		125	190	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN						
EN Rising Threshold				1.17	1.25	V
EN Falling Threshold			0.97	1.07		V
EN Source Current		EN voltage below falling threshold		5		µA
		EN voltage above rising threshold		1		µA
THERMAL SHUTDOWN (TSD)						
Threshold				150		°C
Hysteresis				25		°C

[1] Pin-to-pin measurement.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, SW, EN, PGOOD	−0.3 V to +22 V
SW 10 ns Transient	−2.5 V to +22 V
SW 100 ns Transient	−1 V to +22 V
BST	V_{SW} + 6 V
FB, SS, COMP, ILIM, RT	−0.3 V to +6 V
VREG	−0.3 V to +12 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in the circuit board (4-layer, JEDEC standard board) for surface mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	42.6	6.8 (EP, SW)	°C/W
		2.3 (EP, GND)	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

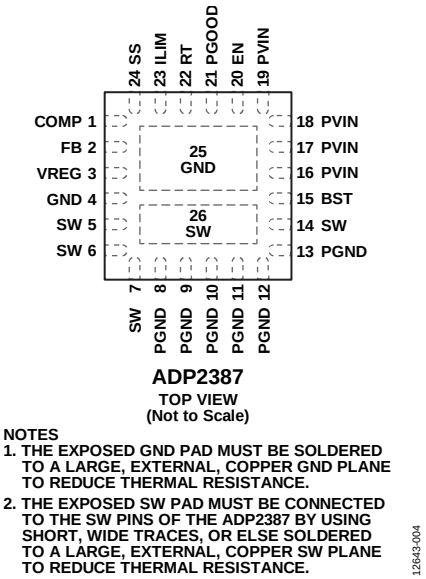


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	Error Amplifier Output. Connect an RC network from COMP to GND.
2	FB	Feedback Voltage Sense Input. Connect this pin to a resistor divider from the output voltage, V_{OUT}.
3	VREG	Output of the Internal 8 V Regulator. The control circuits are powered from this voltage. Place a 1 µF, X7R or X5R ceramic capacitor between this pin and GND.
4	GND	Analog Ground. This pin is the return of the internal control circuit.
5 to 7, 14	SW	Switch Node Outputs. Connect these pins to the output inductor.
8 to 13	PGND	Power Ground. This pin is the return of the low-side power MOSFET.
15	BST	Supply Rail for the High-Side Gate Drive. Place a 0.1 µF, X7R or X5R capacitor between SW and BST.
16 to 19	PVIN	Power Inputs. Connect these pins to the input power source and connect a bypass capacitor between these pins and PGND.
20	EN	Precision Enable Pin. An external resistor divider can set the turn on threshold. To enable the device automatically, connect the EN pin to the PVIN pin.
21	PGOOD	Power-Good Output (Open Drain). Connecting a pull-up resistor of 10 kΩ to 100 kΩ to this pin is recommended.
22	RT	Frequency Setting. Connect a resistor between RT and GND to program the switching frequency between 200 kHz to 1400 kHz.
23	ILIM	Current-Limit Threshold Setting. Connect a resistor between ILIM and GND to program the current-limit threshold.
24	SS	Soft Start Control. Connect a capacitor from SS to GND to program the soft start time. If this pin is open, the regulator uses the internal soft start time.
25	EP, GND	The exposed GND pad must be soldered to a large, external, copper GND plane to reduce thermal resistance.
26	EP, SW	The exposed SW pad must be connected to the SW pins of the ADP2387 by using short, wide traces, or else soldered to a large, external copper SW plane to reduce thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 2.2 µH, C_{OUT} = 100 µF + 47 µF, f_{SW} = 600 kHz, unless otherwise noted.

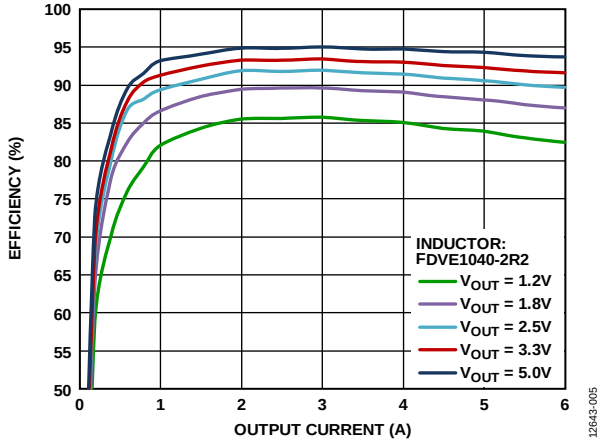


Figure 5. Efficiency at V_{IN} = 12 V, f_{SW} = 600 kHz

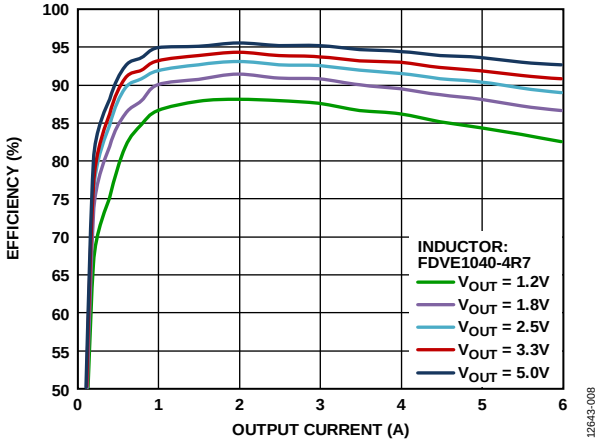


Figure 8. Efficiency at V_{IN} = 12 V, f_{SW} = 300 kHz

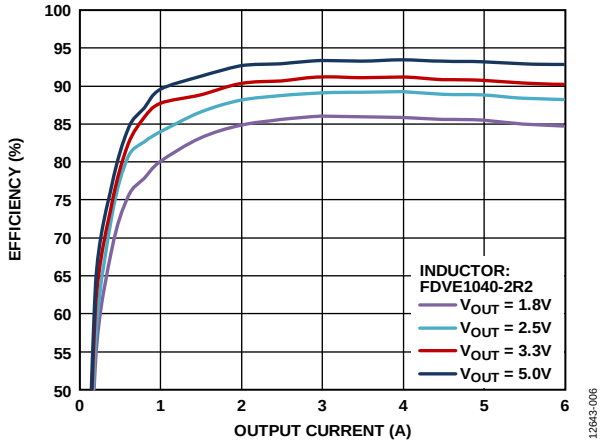


Figure 6. Efficiency at V_{IN} = 18 V, f_{SW} = 600 kHz

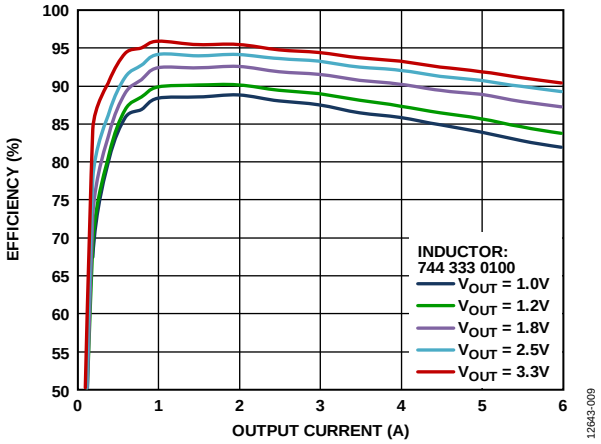


Figure 9. Efficiency at V_{IN} = 5 V, f_{SW} = 600 kHz

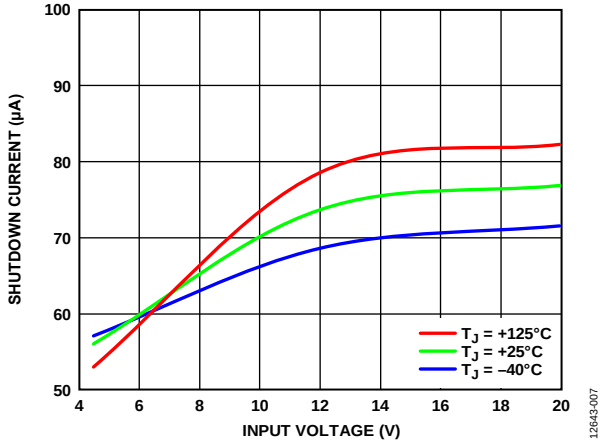


Figure 7. Shutdown Current vs. Input Voltage

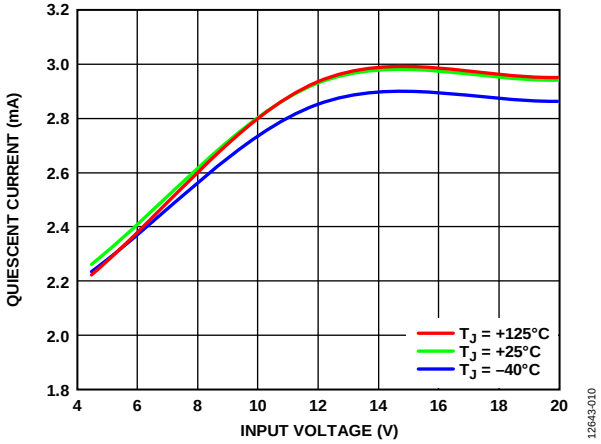


Figure 10. Quiescent Current vs. Input Voltage

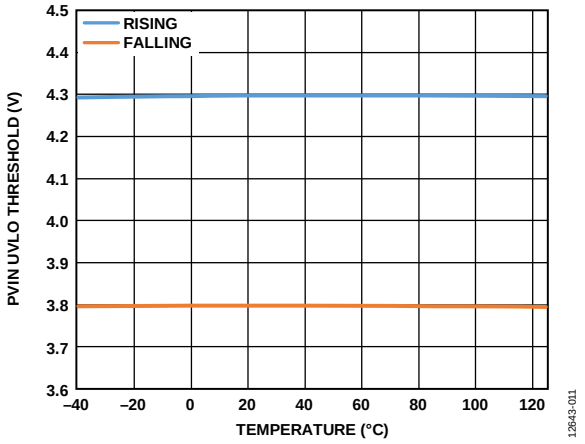


Figure 11. PVIN UVLO Threshold vs. Temperature

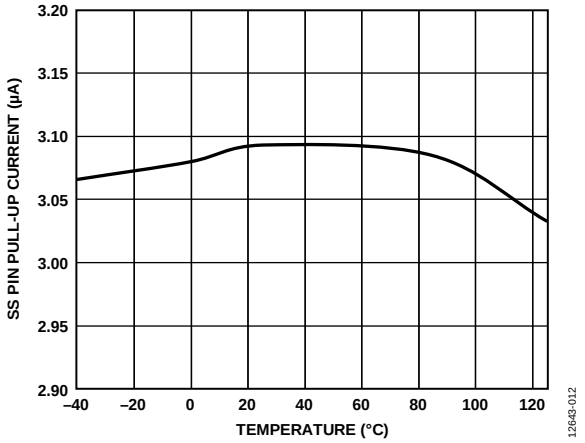
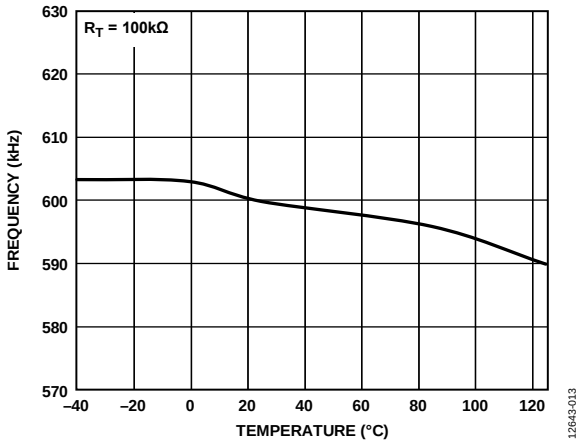


Figure 12. SS Pin Pull-Up Current vs. Temperature



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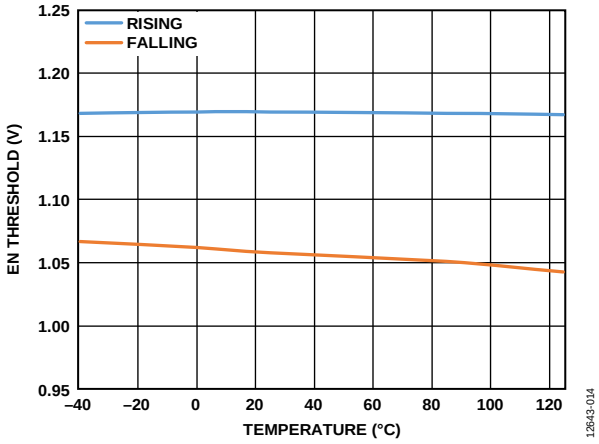

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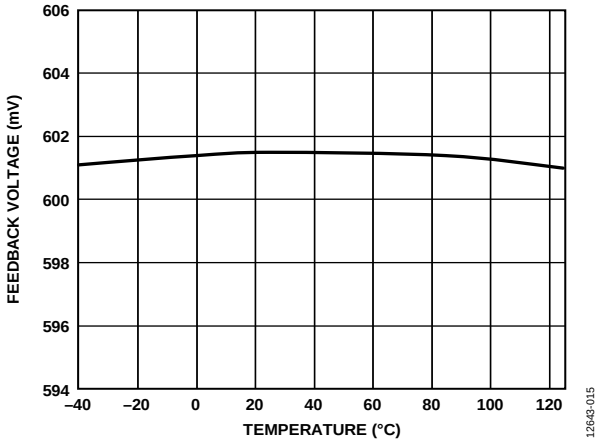

Figure 15. Feedback Voltage vs. Temperature

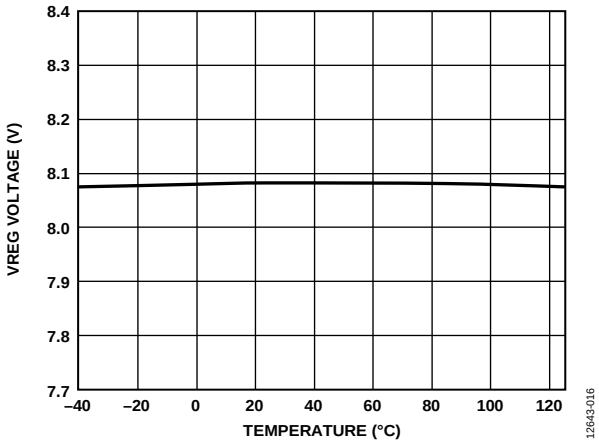

Figure 16. VREG Voltage vs. Temperature

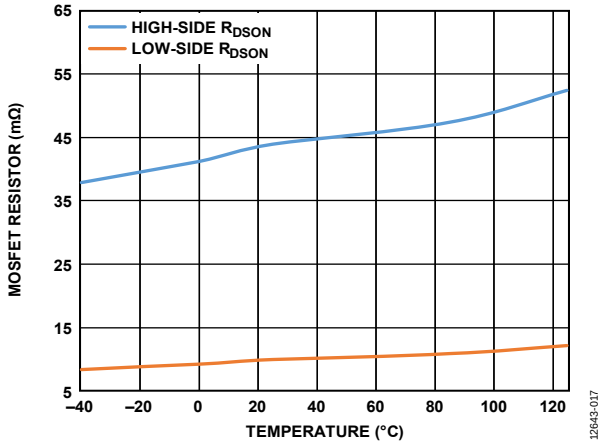

Figure 17. MOSFET Resistor vs. Temperature

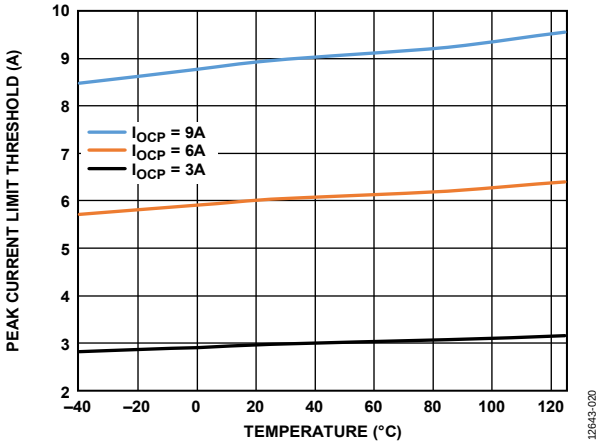

Figure 20. Peak Current-Limit Threshold vs. Temperature

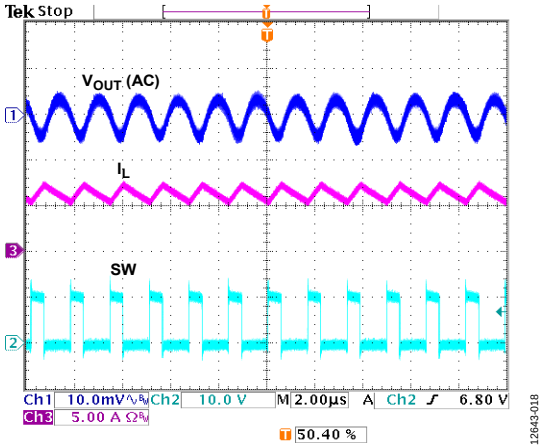

Figure 18. Working Mode Waveform

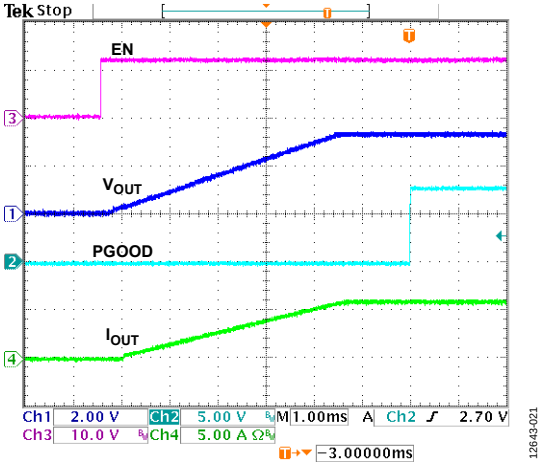

Figure 21. Soft Start with Full Load

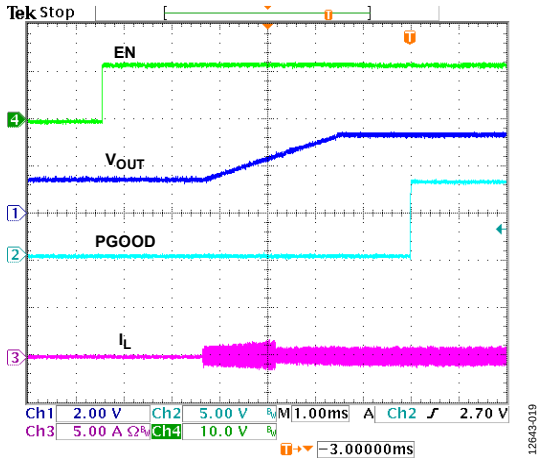

Figure 19. Precharged Output

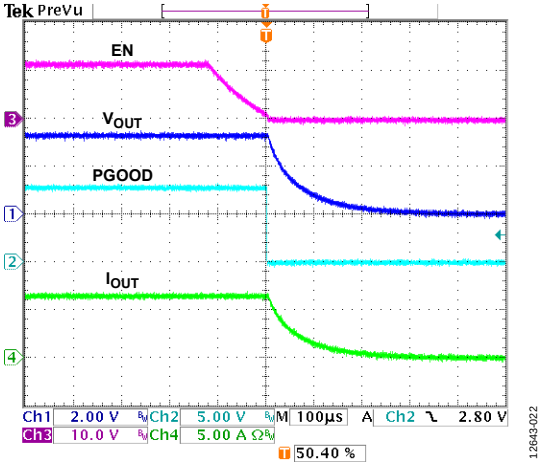

Figure 22. Shutdown with Full Load

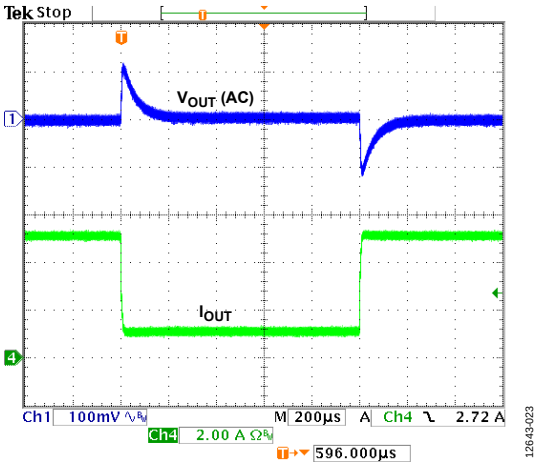

Figure 23. Load Transient Response, 1 A to 5 A

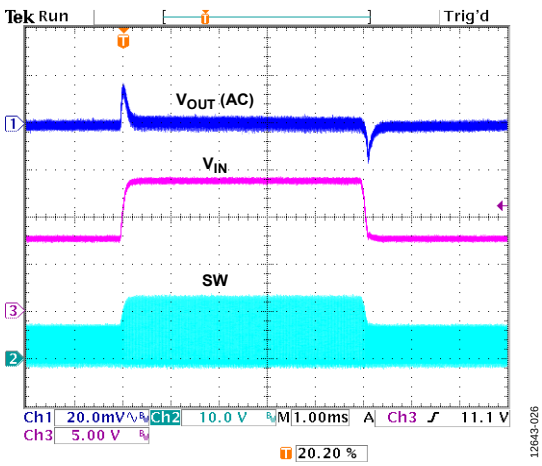

Figure 26. Line Transient Response, V_{IN} from 8 V to 14 V, I_{OUT} = 6 A

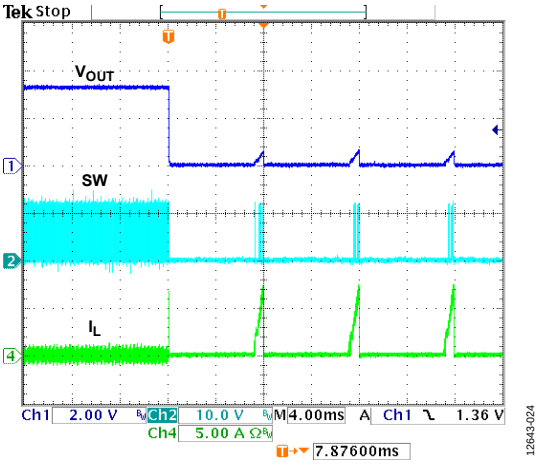

Figure 24. Output Short Entry

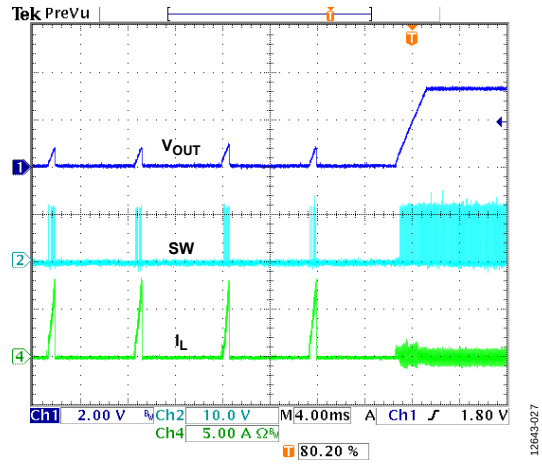

Figure 27. Output Short Recovery

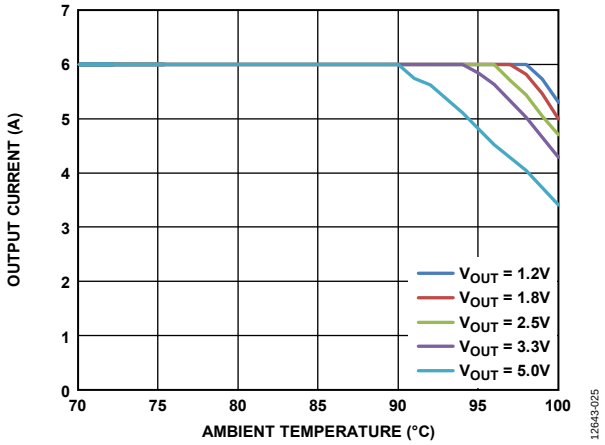

Figure 25. Output Current vs. Ambient Temperature at V_{IN} = 12 V, f_{SW} = 600 kHz, Measured on the ADP2387 Evaluation Board

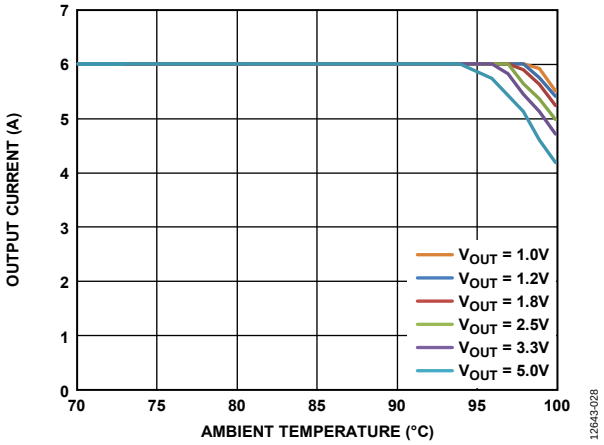

Figure 28. Output Current vs. Ambient Temperature at V_{IN} = 12 V, f_{SW} = 300 kHz, Measured on the ADP2387 Evaluation Board

THEORY OF OPERATION

The ADP2387 is a synchronous step-down, dc-to-dc regulator that uses a current mode architecture with an integrated high-side power switch and a low-side synchronous rectifier. The regulator targets high performance applications that require high efficiency and design flexibility.

The ADP2387 operates with an input voltage from 4.5 V to 20 V and regulates the output voltage from 0.6 V to 90% of the input voltage. Additional features that maximize design flexibility include programmable current-limit threshold, programmable switching frequency, programmable soft start, external compensation, precision enable, and a power-good output.

CONTROL SCHEME

The ADP2387 uses a fixed frequency, peak current mode PWM control architecture. At the start of each oscillator cycle, the high-side MOSFET turns on, generating a positive voltage across the inductor. When the inductor current crosses the peak inductor current threshold, the high-side MOSFET turns off, and the low-side MOSFET turns on. Turning on the low-side MOSFET generates a negative voltage across the inductor, which causes the inductor current to decrease. The low-side MOSFET stays on for the rest of cycle (see Figure 18).

PRECISION ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.17 V (typical) with 100 mV of hysteresis. When the enable voltage exceeds 1.17 V, the regulator turns on. When the enable voltage falls below 1.07 V (typical), the regulator turns off. To force the regulator to start automatically when input power is applied, connect EN to PVIN.

The precision EN pin has an internal pull-down current source (5 µA) that provides a default turn off when the EN pin is open.

When the EN pin voltage exceeds 1.17 V (typical), the ADP2387 is enabled and the internal pull-down current source at the EN pin decreases to 1 µA, which allows users to program the PVIN UVLO and hysteresis.

INTERNAL REGULATOR (VREG)

The on-board regulator provides a stable supply for the internal circuits. Place a 1 µF, X7R or X5R ceramic capacitor between the VREG pin and the GND pin. The internal regulator includes a current-limit circuit to protect the output if the maximum external load current is exceeded.

BOOTSTRAP CIRCUITRY

The ADP2387 includes a regulator to provide the gate drive voltage for the high-side MOSFET. It uses differential sensing to generate a 5 V bootstrap voltage between the BST and SW pins.

Place a 0.1 µF, X7R or X5R ceramic capacitor between the BST and the SW pins.

OSCILLATOR

The RT pin controls the ADP2387 switching frequency. A resistor (R_T) from RT to GND can program the switching frequency according to the following equation:

$$f_{SW}\,(\text{kHz}) = \frac{69{,}120}{R_T\,(\text{k}\Omega) + 15}$$

A 100 kΩ resistor sets the frequency to 600 kHz, and a 42.2 kΩ resistor sets the frequency to 1.2 MHz. Figure 29 shows the typical relationship between the switching frequency (f_{SW}) and R_T.

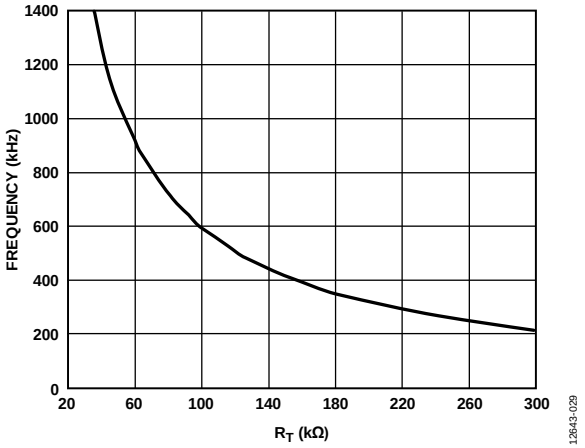

Figure 29. Switching Frequency vs. R_T

SOFT START

The ADP2387 has integrated soft start circuitry to limit the output voltage rising time and reduce inrush current at startup. Calculate the internal soft start time (t_{SS_INT}) by using the following equation:

$$t_{SS\_INT} = \frac{1600}{f_{SW}\,(\text{kHz})}\,(\text{ms})$$

To program a slower soft start time, use the SS pin. When a capacitor is connected between the SS pin and GND, an internal current charges the capacitor to establish the soft start ramp. Calculate the external soft start time (t_{SS_EXT}) by using the following equation:

$$t_{SS\_EXT} = \frac{0.6\ \text{V} \times C_{SS}}{I_{SS\_UP}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS_UP} is the soft start pull-up current (3.1 µA).

The internal error amplifier includes three positive inputs: the internal reference voltage, the internal digital soft start voltage, and the SS pin voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages.

When the output voltage is charged prior to turn on, the ADP2387 prevents the reverse inductor current from discharging the output capacitor. This function remains active until the soft start voltage exceeds the voltage on the FB pin.

POWER GOOD

The power-good pin (PGOOD) is an active high, open-drain output that requires an external resistor to pull it up to a voltage. A logic high on the PGOOD pin indicates that the voltage on the FB pin (and, therefore, the output voltage) is within regulation.

The power-good circuitry monitors the output voltage on the FB pin and compares it to the rising and falling thresholds that are specified in Table 1. If the rising output voltage exceeds the target value, the PGOOD pin is held low. The PGOOD pin continues to be held low until the falling output voltage returns to the target value.

If the output voltage falls below the target output voltage, the PGOOD pin is held low. The PGOOD pin continues to be held low until the rising output voltage returns to the target value.

The power-good rising and falling thresholds are shown in Figure 30. There is a 1024 clock cycle waiting period before the PGOOD pin is pulled from low to high, and there is a 16 clock cycle waiting period before the PGOOD pin is pulled from high to low.

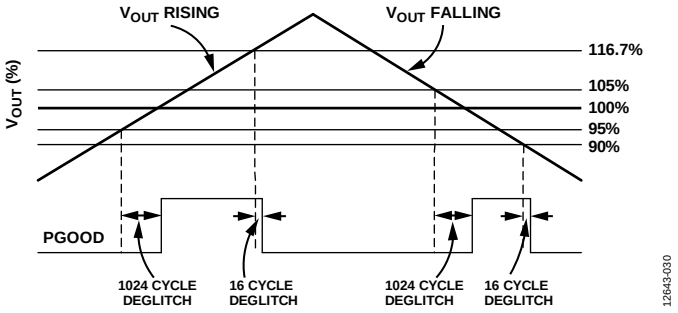

Figure 30. PGOOD Rising and Falling Thresholds

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2387 has a peak current-limit protection circuit to prevent current runaway. A resistor between ILIM and GND programs the peak current-limit threshold according to the following equation:

$$I_{OCP}(\text{A}) = \frac{405}{R_{ILIM}(\text{k}\Omega) + 0.5}$$

where:
I_{OCP} is the peak current-limit threshold.
R_{ILIM} is the resistor between ILIM and GND.

Figure 31 shows the typical relationship between the peak current-limit threshold and R_{ILIM}.

During the initial soft start, the ADP2387 uses frequency foldback to prevent output current runaway. The switching frequency reduces according to the voltage on the FB pin, which allows more time for the inductor to discharge. Table 5 shows the correlation between the switching frequency and FB pin voltage.

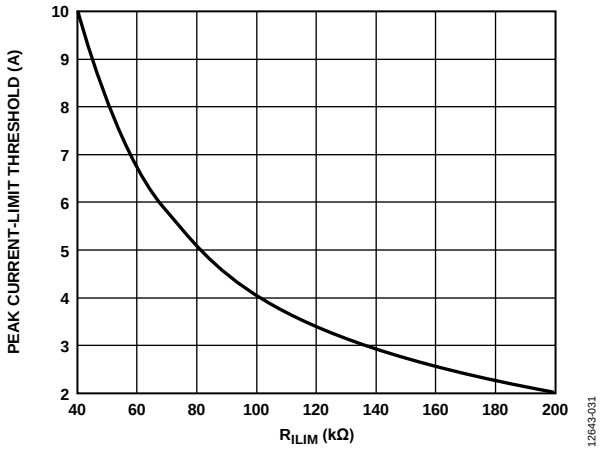

Figure 31. Peak Current-Limit Threshold vs. R_{ILIM}

Table 5. FB Pin Voltage and Switching Frequency

FB Pin Voltage	Switching Frequency
$V_{FB} \geq 0.4$ V	f_{SW}
0.4 V > $V_{FB} \geq$ 0.2 V	$f_{SW}/2$
$V_{FB} < 0.2$ V	$f_{SW}/4$

For protection against heavy loads, the ADP2387 uses a hiccup mode for overcurrent protection. When the inductor peak current reaches the current-limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this process. If the overcurrent counter reaches 10 or if the FB pin voltage falls to 0.4 V after the soft start, the regulator enters hiccup mode. The high-side and low-side MOSFETs both turn off. The regulator remains in hiccup mode for 4096 clock cycles and then attempts to restart. If the current-limit fault clears, the regulator resumes normal operation. Otherwise, it reenters hiccup mode.

The ADP2387 also provides a sink current-limit to prevent the low-side MOSFET from sinking excessive current from the load. When the voltage across the low-side MOSFET exceeds the sink current-limit threshold, which is typically 2.5 A, the low-side MOSFET turns off immediately for the rest of the cycle. Both high-side and low-side MOSFETs turn off until the next clock cycle.

In some cases, the input voltage (V_{PVIN}) ramp rate is too slow or the output capacitor is too large for the output to reach regulation during the soft start process, which causes the regulator to enter hiccup mode. To avoid such occurrences, use a resistor divider at the EN pin to program the input voltage UVLO, or use a longer soft start time.

OVERVOLTAGE PROTECTION (OVP)

The ADP2387 includes an overvoltage protection feature to protect the regulator against an output short to a higher voltage supply or when a strong load disconnect transient occurs. If the feedback voltage increases to 0.7 V, the internal high-side and low-side MOSFETs turn off until the voltage at the FB pin decreases to 0.63 V. At that time, the ADP2387 resumes normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry is integrated in the ADP2387 to prevent the occurrence of power-on glitches. If the V_{PVIN} voltage drops below 3.8 V typical, the device shuts down and both the power switch and synchronous rectifier turn off. When the V_{PVIN} voltage rises again above 4.3 V typical, the soft start period is initiated and the device is enabled.

THERMAL SHUTDOWN

If the ADP2387 junction temperatures rises above 150°C, the internal thermal shutdown circuit turns off the regulator for self protection. Extreme junction temperatures can be the result of high current operation, poor circuit board thermal design, and/or high ambient temperature. If an overtemperature event occurs, the ADP2387 does not return to normal operation until the on-chip temperature falls below 125°C because a 25°C hysteresis is included in the thermal shutdown circuit. Upon recovery, a soft start initiates before normal operation begins.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A ceramic capacitor in the 10 µF to 47 µF range is recommended. Keep the loop that is composed of this input capacitor, the high-side MOSFET, and the low-side MOSFET as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor must be larger than the value calculated by the following equation:

$$I_{C_{IN-RMS}} = I_{OUT} \times \sqrt{D \times (1-D)}$$

OUTPUT VOLTAGE SETTING

An external resistive divider sets the output voltage of the ADP2387. Use the following equation to calculate the resistor values:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

where:
R_{TOP} is the top feedback resistor between VOUT and FB.
R_{BOT} is the bottom feedback resistor between FB and GND.

To limit output voltage accuracy degradation due to the FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} < 30 kΩ.

Table 6 lists the recommended resistor divider values for various output voltages.

Table 6. Resistor Divider Values for Various Output Voltages

V_{OUT} (V)	R_{TOP} ± 1% (kΩ)	R_{BOT} ± 1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2387 is typically 130 ns. Calculate the minimum output voltage for a given input voltage and switching frequency by using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the series resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is constrained by the minimum off time and the maximum duty cycle. The minimum off time is typically 200 ns, and the maximum duty cycle of the ADP2387 is typically 90%.

Calculate the maximum output voltage, limited by the minimum off time for a given input voltage and switching frequency, by using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

Calculate the maximum output voltage, limited by the maximum duty cycle for a given input voltage, using the following equation:

$$V_{OUT\_MAX} = D_{MAX} \times V_{IN} \quad (3)$$

where D_{MAX} is the maximum duty cycle.

As shown in Equation 1 to Equation 3, reducing the switching frequency alleviates the minimum on time and minimum off time limitation.

INDUCTOR SELECTION

The operating frequency, input voltage, output voltage, and inductor ripple current determine the inductor value. Using a small inductor leads to a faster transient response, but it degrades efficiency due to a larger inductor ripple current; whereas using a large inductor value leads to smaller ripple current and better efficiency but results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current. Calculate the inductor value by using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor current ripple.
f_{SW} is the switching frequency.

The ADP2387 uses adaptive slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

For a duty cycle that is larger than 50%, determine the minimum inductor value by using the following equation:

$$L\ (Minimum) = \frac{V_{OUT} \times (1 - D)}{4 \times f_{SW}}$$

Calculate the peak inductor current as follows:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be higher than the current-limit threshold of the switch. This higher rating prevents the inductor from reaching saturation.

Calculate the rms current of the inductor as follows:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 7 lists some recommended inductors.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects the output ripple voltage load step transient and the loop stability of the regulator.

For example, during a load step transient where the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current. The delay caused by the control loop causes output undershoot. Calculate the output capacitance that is required to satisfy the voltage droop requirement by using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor, with a typical setting of $K_{UV} = 2$.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example occurs when a load is suddenly removed from the output, and the energy stored in the inductor rushes into the output capacitor, causing the output to overshoot.

Calculate the output capacitance required to meet the overshoot requirement by using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times {\Delta I_{STEP}}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - {V_{OUT}}^2}$$

where:
K_{OV} is a factor, with a typical setting of $K_{OV} = 2$.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The equivalent series resistance (ESR) and capacitance value determine the output ripple. Use the following equations to select a capacitor to meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
ΔV_{OUT_RIPPLE} is the allowable output ripple voltage.
R_{ESR} is the ESR of the output capacitor in ohms (Ω).

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple performance.

The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor must be larger than the value calculated by

$$I_{C_{OUT\_RMS}} = \frac{\Delta I_L}{\sqrt{12}}$$

Table 7. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)
Toko	FDVE0630-R47M	0.47	15.6	14.1	3.7
	FDVE0630-R75M	0.75	10.9	10.7	6.2
	FDVE0630-1R0M	1.0	9.5	9.5	8.5
	FDVE1040-1R5M	1.5	13.7	14.6	4.6
	FDVE1040-2R2M	2.2	11.4	11.6	6.8
	FDVE1040-3R3M	3.3	9.8	9.0	10.1
	FDVE1040-4R7M	4.7	8.2	8.0	13.8
Vishay	IHLP3232DZ-R47M-11	0.47	14	25	2.38
	IHLP3232DZ-R68M-11	0.68	14.5	22.2	3.22
	IHLP3232DZ-1R0M-11	1.0	12	18.2	4.63
	IHLP4040DZ-1R5M-01	1.5	27.5	15	5.8
	IHLP4040DZ-2R2M-01	2.2	25.6	12	9
	IHLP4040DZ-3R3M-01	3.3	18.6	10	14.4
	IHLP4040DZ-4R7M-01	4.7	17	9.5	16.5
Wurth Elektronik	744 325 120	1.2	25	20	1.8
	744 325 180	1.8	18	16	3.5
	744 325 240	2.4	17	14	4.75
	744 325 330	3.3	15	12	5.9
	744 325 420	4.2	14	11	7.1

PROGRAMMING INPUT VOLTAGE UVLO

The ADP2387 has a precision enable input that can program the UVLO threshold of the input voltage (see Figure 32).

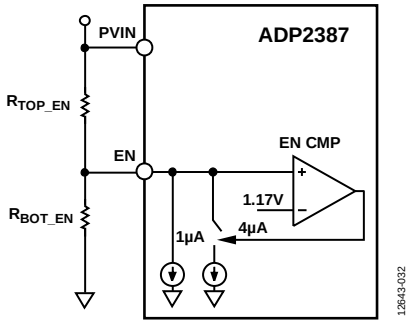

Figure 32. Programming the Input Voltage UVLO

Use the following equations to calculate R_{TOP_EN} and R_{BOT_EN}:

$$R_{TOP\_EN} = \frac{1.07\ \text{V} \times V_{IN\_RISING} - 1.17\ \text{V} \times V_{IN\_FALLING}}{1.07\ \text{V} \times 5\ \mu\text{A} - 1.17\ \text{V} \times 1\ \mu\text{A}}$$

$$R_{BOT\_EN} = \frac{1.17\ \text{V} \times R_{TOP\_EN}}{V_{IN\_RISING} - R_{TOP\_EN} \times 5\ \mu\text{A} - 1.17\ \text{V}}$$

where:
V_{IN_RISING} is the V_{IN} rising threshold.
$V_{IN\_FALLING}$ is the V_{IN} falling threshold.

COMPENSATION DESIGN

For peak current-mode control, simplify the power stage as a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero that is contributed by the output capacitor ESR. The control-to-output transfer function is based on the following:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_Z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_P}\right)}$$

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
A_{VI} = 8.7 A/V.
R is the load resistance.
R_{ESR} is the equivalent series resistance of the output capacitor.
C_{OUT} is the output capacitance.

A transconductance amplifier is used on the ADP2387 as an error amplifier and to compensate the system. Figure 33 shows the simplified, peak current mode control, small signal circuit.

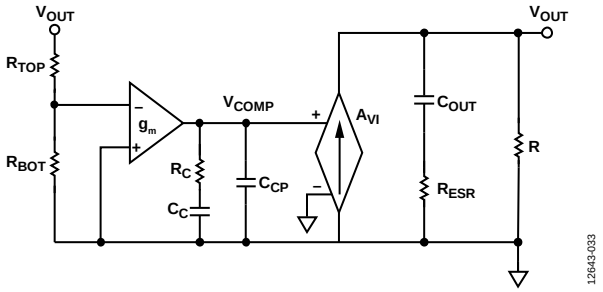

Figure 33. Simplified, Peak Current Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and the optional components, C_{CP} and R_C, contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C \times C_{CP}} \times s\right)} \times G_{VD}(s)$$

The following design guideline shows how to select the R_C, C_C, and C_{CP} compensation components for ceramic output capacitor applications.

Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.

Calculate R_C by using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6\,\text{V} \times g_m \times A_{VI}}$$

Place the compensation zero at the domain pole (f_P), then determine C_C by using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

ADIsimPower DESIGN TOOL

The ADP2387 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and to calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count, while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about the ADIsimPower design tools, go to www.analog.com/ADIsimPower. The tool set is available from the Analog Devices, Inc., website, and users can request an unpopulated board.

DESIGN EXAMPLE

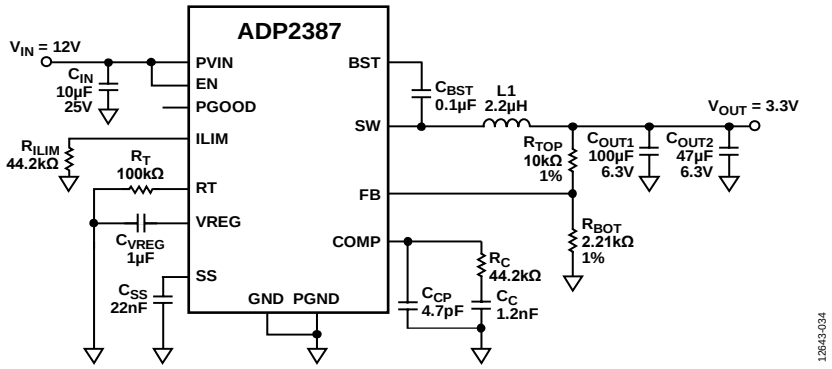

Figure 34. Schematic for Design Example

This section describes the procedures for selecting the external components, based on the example specifications that are listed in Table 8. See Figure 34 for the schematic of this design example.

Table 8. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification
Input Voltage (V_{IN})	12.0 V ± 10%
Output Voltage (V_{OUT})	3.3 V
Output Current (I_{OUT})	6 A
Output Voltage Ripple (ΔV_{OUT_RIPPLE})	33 mV
Load Transient	±5%, 1 A to 5 A, 2 A/µs
Switching Frequency (f_{SW})	600 kHz

OUTPUT VOLTAGE SETTING

Choose a 10 kΩ resistor as the top feedback resistor (R_{TOP}), and calculate the bottom feedback resistor (R_{BOT}) by

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 3.3 V, the resistors values are as follows: R_{TOP} = 10 kΩ, and R_{BOT} = 2.21 kΩ.

FREQUENCY SETTING

To set the switching frequency to 600 kHz, connect a 100 kΩ resistor from the RT pin to GND.

CURRENT-LIMIT THRESHOLD SETTING

Connect a 44.2 kΩ resistor between ILIM pin and GND to set the current-limit threshold at 9 A.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the maximum output current. To estimate the inductor value, use the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} = 12 V.
V_{OUT} = 3.3 V.
D = 0.275.
ΔI_L = 1.8 A.
f_{SW} = 600 kHz.

This calculation results in L = 2.215 µH. Choose the standard inductor value of 2.2 µH.

Calculate the peak-to-peak inductor ripple current by using the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This calculation results in ΔI_L = 1.81 A.

To calculate the peak inductor current, use the following equation:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This calculation results in I_{PEAK} = 6.905 A.

To calculate the rms current flowing through the inductor, use the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

This calculation results in I_{RMS} = 6.023 A.

Based on the calculated current value, select an inductor with a minimum rms current rating of 6.03 A and a minimum saturation current rating of 6.91 A.

However, to protect the inductor from reaching its saturation point under the current-limit condition, rate the inductor for at least a 9.2 A saturation current for reliable operation.

Based on the requirements previously described, select a 2.2 µH inductor, such as the FDVE1040-2R2M from Toko, which has a 6.1 mΩ DCR and an 11.4 A saturation current.

OUTPUT CAPACITOR SELECTION

The output capacitor is required to meet both the output voltage ripple and load transient response requirements.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance value of the output capacitor:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

This calculation results in C_{OUT_RIPPLE} = 11.4 µF, and R_{ESR} = 18 mΩ.

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}^2}$$

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
$K_{OV} = K_{UV} = 2$ are the coefficients for estimation purposes.
ΔI_{STEP} = 4 A is the load transient step.
ΔV_{OUT_OV} = 5% V_{OUT} is the overshoot voltage.
ΔV_{OUT_UV} = 5% V_{OUT} is the undershoot voltage.

This calculation results in C_{OUT_OV} = 63.1 µF, and C_{OUT_UV} = 24.5 µF.

According to the calculation, the output capacitance must be greater than 63 µF, and the ESR of the output capacitor must be smaller than 18 mΩ. It is recommended that one 100 µF/X5R/6.3 V ceramic capacitor and one 47 µF/X5R/6.3 V ceramic capacitor be used, such as the GRM32ER60J107ME20 and GRM32ER60J476ME20 from Murata, with an ESR of 2 mΩ.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency (f_C) to f_{SW}/10. In this case, f_{SW} is running at 600 kHz; therefore, f_C is set to 60 kHz.

The 100 µF and 47 µF ceramic output capacitors have a derated value of 62 µF and 32 µF, respectively.

$$R_C = \frac{2 \times \pi \times 3.3\ \text{V} \times 94\ \mu\text{F} \times 60\ \text{kHz}}{0.6\ \text{V} \times 480\ \mu\text{S} \times 8.7\ \text{A/V}} = 46.7\ \text{k}\Omega$$

$$C_C = \frac{(0.55\ \Omega + 0.002\ \Omega) \times 94\ \mu\text{F}}{46.7\ \text{k}\Omega} = 1111\ \text{pF}$$

$$C_{CP} = \frac{0.002\ \Omega \times 94\ \mu\text{F}}{46.7\ \text{k}\Omega} = 4.0\ \text{pF}$$

Choose standard components, as follows: R_C = 44.2 kΩ, C_C = 1200 pF, and C_{CP} = 4.7 pF.

Figure 35 shows the bode plot at 6 A. The cross frequency is 58 kHz, and the phase margin is 62°.

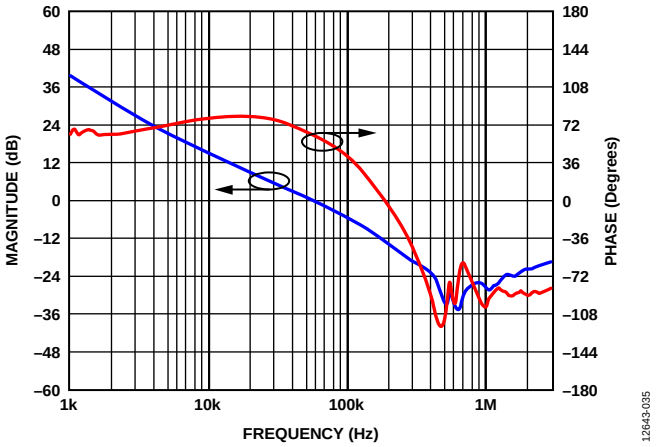

Figure 35. Bode Plot at 6 A

SOFT START TIME PROGRAM

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current. Set the soft start time to 4 ms.

$$C_{SS} = \frac{t_{SS\_EXT} \times I_{SS\_UP}}{0.6} = \frac{4\ \text{ms} \times 3.1\ \mu\text{A}}{0.6\ \text{V}} = 20.7\ \text{nF}$$

Choose a standard component value, as follows: C_{SS} = 22 nF.

INPUT CAPACITOR SELECTION

Place a minimum 10 µF ceramic capacitor near the PVIN pin. In this application, it is recommended that one 10 µF, X5R, 25 V ceramic capacitor be used.

RECOMMENDED EXTERNAL COMPONENTS

Table 9. Recommended External Components for Typical Applications with 6 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
300	12	1	1.5	680 + 2 × 100	10	15	57.6	2200	150
	12	1.2	2.2	680 + 2 × 100	10	10	68.1	2200	120
	12	1.5	2.2	680	15	10	73.2	2200	100
	12	1.8	3.3	680	20	10	88.7	2200	82
	12	2.5	3.3	470	47.5	15	84.5	2200	47
	12	3.3	4.7	3 × 100	10	2.21	44.2	2200	8.2
	12	5	4.7	100 + 47	22	3	33	2200	4.7
	5	1	1.5	680 + 2 × 100	10	15	57.6	2200	150
	5	1.2	1.5	680	10	10	57.6	2200	120
	5	1.5	2.2	680	15	10	73.2	2200	100
	5	1.8	2.2	470	20	10	61.9	2200	82
	5	2.5	2.2	3 × 100	47.5	15	33	2200	10
	5	3.3	2.2	3 × 100	10	2.21	44.2	2200	8.2
600	12	1.5	1	3 × 100	15	10	39	1200	10
	12	1.8	1.5	3 × 100	20	10	47	1200	8.2
	12	2.5	2.2	2 × 100	47.5	15	44.2	1200	4.7
	12	3.3	2.2	100 + 47	10	2.21	44.2	1200	4.7
	12	5	3.3	100	22	3	44.2	1200	2.2
	5	1	1	680	10	15	97.6	1200	68
	5	1.2	1	470	10	10	82	1200	47
	5	1.5	1	3 × 100	15	10	39	1200	10
	5	1.8	1	2 × 100	20	10	33	1200	8.2
	5	2.5	1	100	47.5	15	22	1200	4.7
	5	3.3	1	100 + 47	10	2.21	44.2	1200	4.7
1000	12	2.5	1	100	47.5	15	37.4	680	3.3
	12	3.3	1.5	100	10	2.21	47	680	2.2
	12	5	1.5	100	22	3	73.2	680	2.2
	5	1	0.47	3 × 100	10	15	44.2	680	8.2
	5	1.2	0.47	2 × 100	10	10	34.8	680	6.8
	5	1.5	0.68	100 + 47	15	10	33	680	4.7
	5	1.8	0.68	100 + 47	20	10	39	680	4.7
	5	2.5	0.68	100	47.5	15	37.4	680	3.3
	5	3.3	0.68	100	10	2.21	47	680	2.2

[1] 680 µF: 4 V, KEMET T520Y687M004ATE010; 470 µF: 6.3 V, KEMET T520X477M006ATE010; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; and 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good printed circuit board (PCB) layout is essential for obtaining the best performance from the ADP2387. Poor PCB layout can degrade the output regulation, as well as the EMI and electromagnetic compatibility (EMC) performance. Figure 37 shows an example of a good PCB layout for the ADP2387. For optimum layout, refer to the following guidelines:

- Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground reference of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed GND pad of the ADP2387.
- Place the input capacitor, inductor, and output capacitor as close as possible to the IC, and use short traces. Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible by ensuring that the input and output capacitors share a common power ground plane. In addition, ensure that the high current path from the power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the PGND pins of the ADP2387 to the PGND plane as close as possible to the input and output capacitors.
- Connect the exposed GND pad of the ADP2387 to a large, external copper ground plane to maximize its power dissipation capability and to minimize junction temperature. In addition, connect the exposed SW pad to the SW pins of the ADP2387, using short, wide traces; or connect the exposed SW pad to a large external copper plane of the switching node for high current flow.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce the parasitic capacitance pickup.

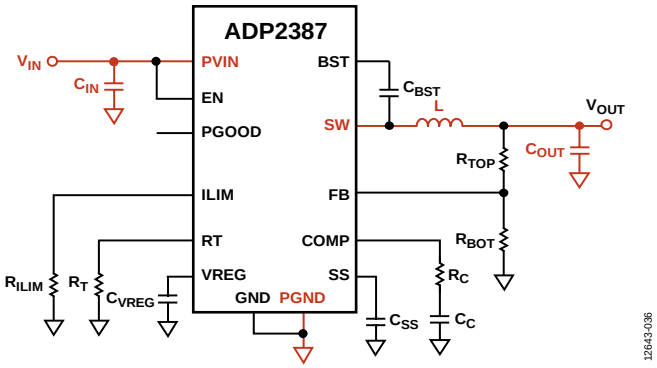

Figure 36. High Current Path in the PCB Circuit

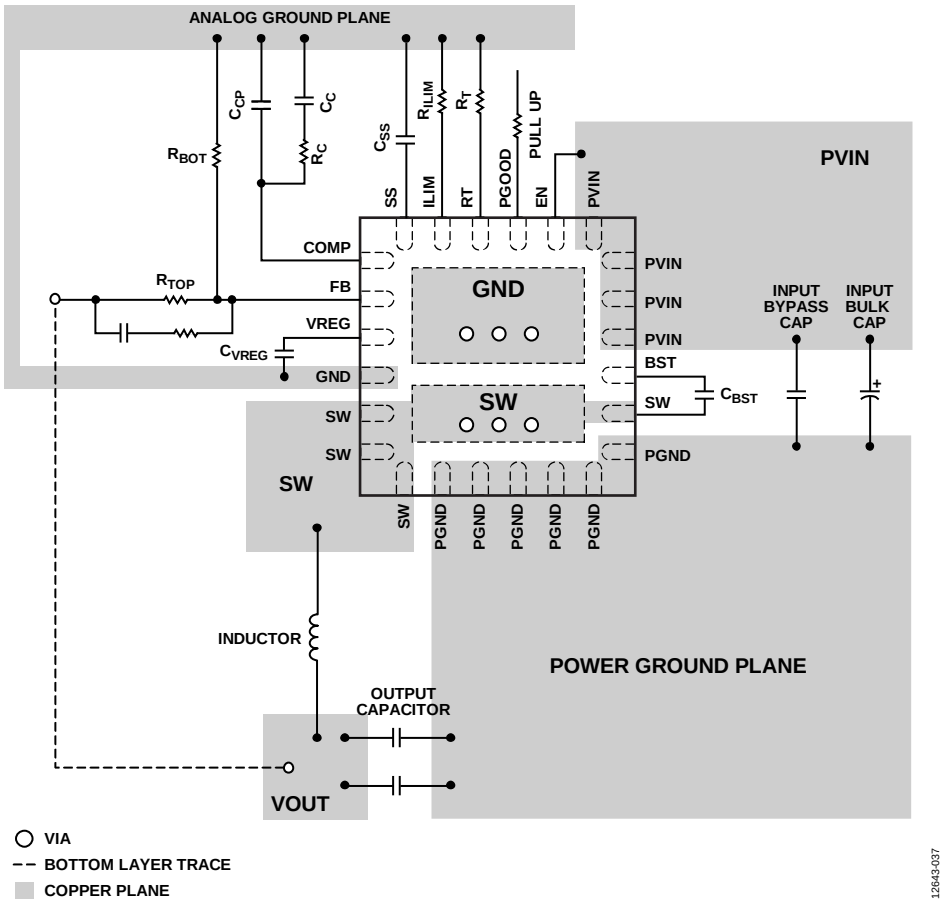

Figure 37. Recommended PCB Layout

TYPICAL APPLICATIONS CIRCUITS

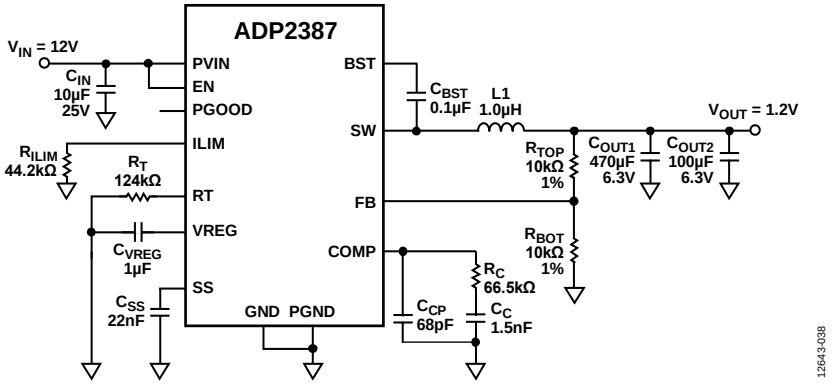

Figure 38. Typical Applications Circuit, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 500 kHz

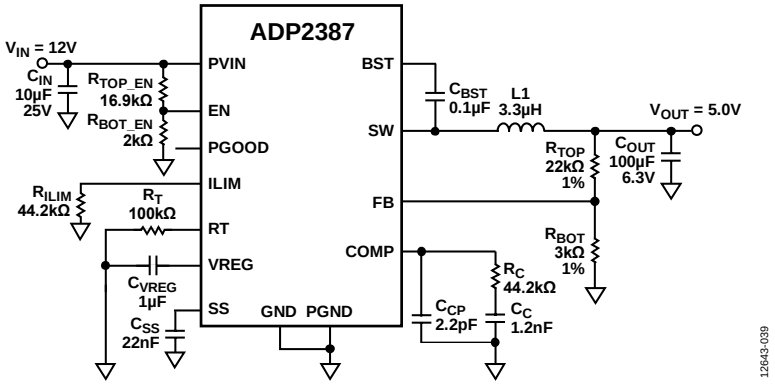

Figure 39. Programming Input Voltage UVLO Rising Threshold at 11 V, Falling Threshold at 10 V, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 6 A, f_{SW} = 600 kHz

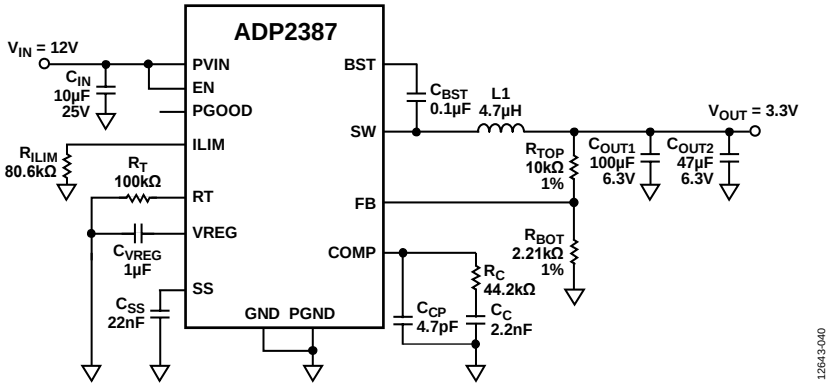

Figure 40. Programming Peak Current-Limit Threshold at 5 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, f_{SW} = 600 kHz

OUTLINE DIMENSIONS

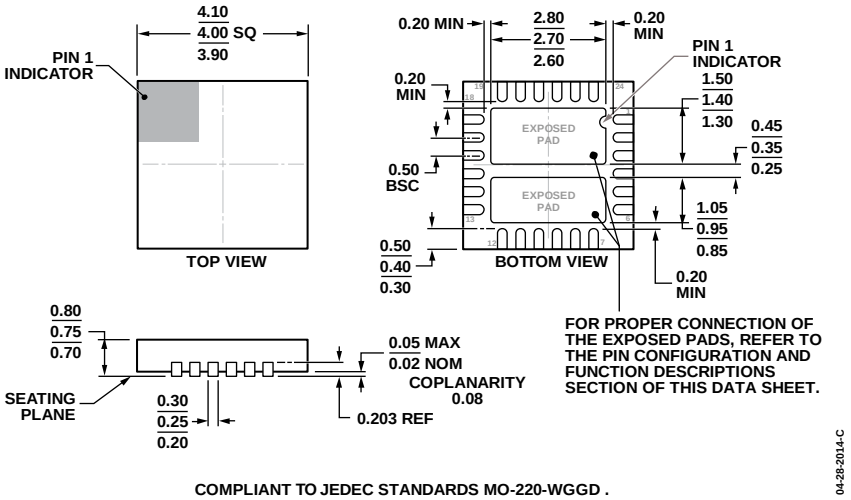

Figure 41. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP2387ACPZN-R7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7″ Tape and Reel	CP-24-12
ADP2387-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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