REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 13-04-09	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, QUAD UV/OV POSITIVE/NEGATIVE VOLTAGE SUPERVISOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12655**
	REV	**PAGE** 1 **OF** 11

AMSC N/A

5962-V061-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad UV/OV Positive/Negative voltage supervisor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12655	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADM2914-EP	Quad UV/OV Positive/Negative voltage supervisor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-137-AB	Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{CC}	-0.3 V to +6.0 V
$\overline{UV}$, $\overline{OV}$	-0.3 V to +16.0 V
Timer	-0.3 V to (V_{CC} + 0.3 V)
VL_X, VH_X, $\overline{LATCH}$, SEL	-0.3 V to +7.5 V
I_{CC}	10 mA
Reference load current (I_{REF})	±1 mA
$I_{\overline{UV}}$, $I_{\overline{OV}}$	10 mA
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Lead temperature (Soldering, 10 sec)	300°C

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	Unit
Case X	104	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 $\overline{\text{UV}}/\overline{\text{OV}}$ Timeout period vs Capacitance. The $\overline{\text{UV}}/\overline{\text{OV}}$ Timeout period vs Capacitance shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Shunt regulator						
V_{CC} shunt regulator voltage	V_{SHUNT}	I_{CC} = 5 mA	6.2	6.6	6.9	V
		T_A = -55°C to +125°C	6.2	6.6	7.0	V
V_{CC} shunt regulator load regulation	ΔV_{SHUNT}	I_{CC} = 2 mA to 10 mA		200	300	mV
Supply						
Supply voltage 3/	V_{CC}		2.3		V_{SHUNT}	V
Minimum VCC output valid	$V_{CCR(MIN)}$				1	
Supply under voltage lockout	$V_{CC(UVLO)}$	V_{CC} rising	1.9	2	2.1	
Supply under voltage lockout hysteresis	$\Delta V_{CC(HYST)}$		5	25	50	mV
Supply current	I_{CC}	V_{CC} = 2.3 V to 6 V		62	100	µA
Reference output						
Reference output voltage	V_{REF}	I_{VREF} = ±1 mA	0.985	1	1.015	V
		T_A = -55°C to +125°C	0.985	1	1.020	
Undervoltage/Overvoltage characteristics						
Undervoltage/Overvoltage threshold	V_{UOT}		492.5	500	507.5	mV
Undervoltage/Overvoltage threshold to output delay	t_{UOD}	VHx = V_{UOT} – 5 mV or VLx = V_{UOT} + 5 mV	50	125	500	µs
VHx, VLx input current	I_{VHL}				±15	nA
		T_A = -55°C to +125°C			±30	
$\overline{UV}/\overline{OV}$ timeout period	t_{UOTO}	C_{TIMER} = 1 nF	6	8.5	12.5	ms
		T_A = -55°C to +125°C	6	8.5	14	
$\overline{OV}$ Latch clear input						
$\overline{OV}$ Latch clear threshold input high	$V_{\overline{LATCH}(IH)}$		1.2			V
$\overline{OV}$ Latch clear threshold input low	$V_{\overline{LATCH}(IL)}$				0.8	
$\overline{LATCH}$ input current	I_{LATCH}	$V_{\overline{LATCH}}$ >0.5 V			±1	µA
Timer characteristics						
Timer pull up current	$I_{TIMER(UP)}$	V_{TIMER} = 0 V	-1.3	-2.1	-2.8	µA
		T_A = -55°C to +125°C	-1.2	-2.1	-2.8	
Timer pull down current	$I_{TIMER(DOWN)}$	V_{TIMER} = 1.6 V	1.3	2.1	2.8	
		T_A = -55°C to +125°C	1.2	2.1	2.8	
Timer disable voltage	$V_{TIMER(DIS)}$	Reference to V_{CC}	-180	-270		mV
Output voltage						
Output voltage high	$\overline{UV}/\overline{OV}$, V_{OH}	V_{CC} = 2.3 V; $I_{\overline{UV}/\overline{OV}}$ = -1 µA	1			V
Output voltage low	$\overline{UV}/\overline{OV}$, V_{OL}	V_{CC} = 2.3 V; $I_{\overline{UV}/\overline{OV}}$ = -2.5 mA		0.1	0.3	
		V_{CC} = 1 V; $I_{\overline{UV}}$ = -100 µA		0.01	0.15	
Three state input SEL						
Low level input voltage	V_{IL}				0.4	V
High level input voltage	V_{IL}		1.4			
Pin voltage when left in high-Z state	V_Z	I_{SEL} = ±10 µA	0.7	0.9	1.1	
		T_A = -55°C to +125°C	0.6	0.9	1.2	
SEL high, low input current	I_{SEL}				±25	µA
Maximum SEL input current	$I_{SEL(MAX)}$	SEL tied to V_{CC} or GND			±30	

See footnote at end of table.

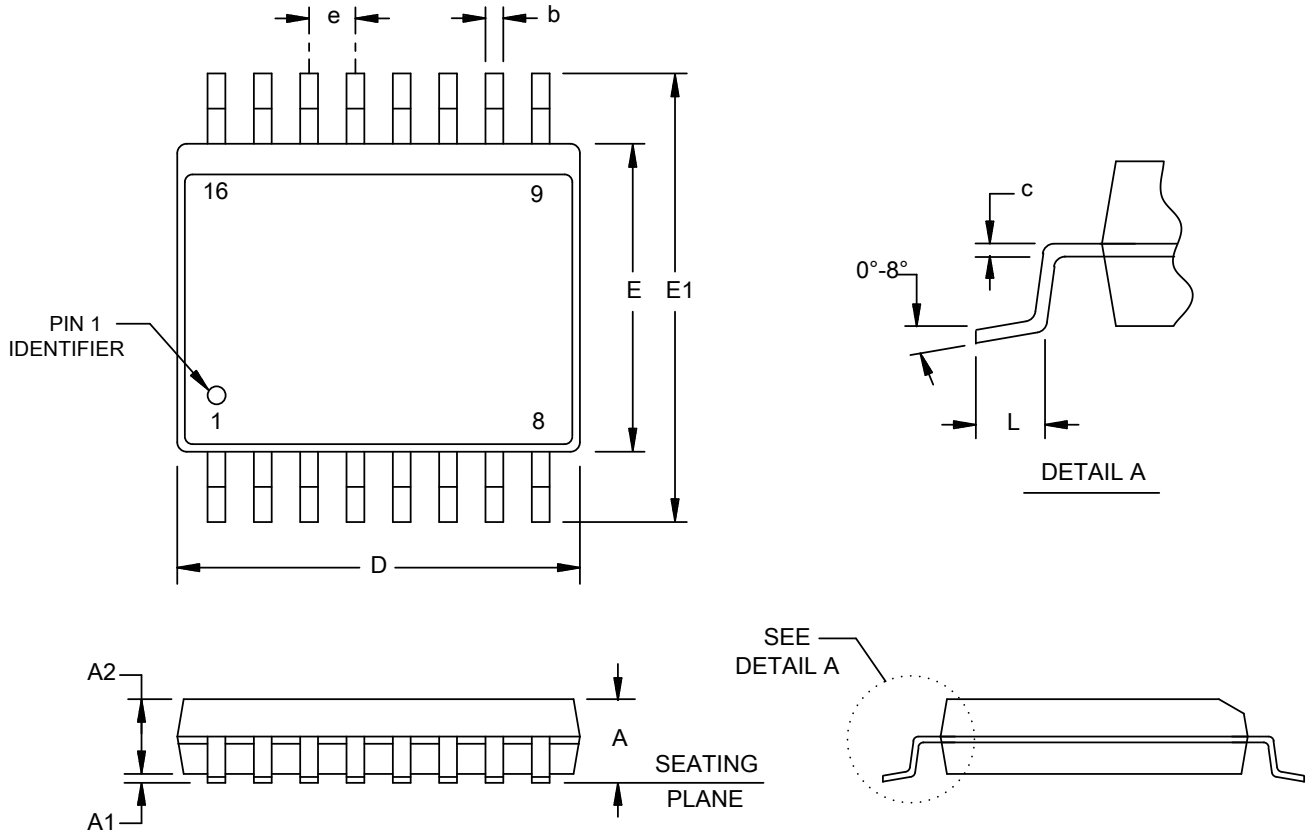
TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ -55°C ≤ T_A ≤ +125°C. Typical values at T_A = 25°C, unless otherwise noted. V_{CC} = 3.3 V, VL_X = 0.45 V, VH_X = 0.55 V, $\overline{LATCH}$ = V_{CC}, SEL = V_{CC}, unless otherwise noted.

3/ The maximum voltage on the V_{CC} pin is limited by the input current. The V_{CC} pin has an internal 6.5 V shunt regulator and, therefore, a low impedance supply greater than 6 V may exceed the maximum allowed input current. When operating from a higher supply then 6 V, always use a dropper resistor.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.053	.069	1.35	1.75	D	.189	.197	4.80	5.00
A1	.049	.065	1.25	1.65	E	.150	.158	3.81	4.01
A2	.004	.010	0.10	0.25	E1	.228	.244	5.79	6.20
b	.008	.012	0.20	0.30	e	.025 BSC		0.64 BSC	
c	.006	.010	0.15	0.25	L	.041 REF		1.04 REF	

NOTES:
1. Controlling dimensions are in inches; millimeters dimensions are rounded off inch; equivalents for reference only and are not appropriate for use in design..
2. Falls within JEDEC MO-137-AB.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VH1	16	V_{CC}
2	VL1	15	TIMER
3	VH2	14	SEL
4	VL2	13	$\overline{\text{LATCH}}$
5	VH3	12	$\overline{\text{UV}}$
6	VL3	11	$\overline{\text{OV}}$
7	VH4	10	REF
8	VL4	9	GND

FIGURE 2. Terminal connections.

Case outline X		
Terminal number	**Mnemonic**	**Description**
1	VH1	Voltage High Input 1 and Voltage High Input 2. If the voltage monitored by VH1 or VH2 drops below 0.5 V, an undervoltage condition is detected. Connect to V_{CC} when not in use.
3	VH2	
2	VL1	Voltage Low Input 1 and Voltage Low Input 2. If the voltage monitored by VL1 or VL2 rises above 0.5 V, an overvoltage condition is detected. Tie to GND when not in use.
4	VL2	
5	VH3	Voltage High Input 3 and Voltage High Input 4. The polarity of these inputs is determined by the state of the SEL pin. When the monitored input is configured as a positive voltage and the voltage monitored by VH3 and VH4 drops below 0.5 V, an undervoltage condition is detected. Conversely, when the input is configures as a negative voltage and the inputs drops below 0.5 V, an overvoltage condition is detected. Connect to V_{CC} when not in use.
7	VH4	
6	VL3	Voltage Low Input 3 and Voltage Low Input 4. The polarity of these inputs is determined by the state of the SEL pin. When the monitored input is configured as a positive voltage and the voltage monitored by VL3 and VL4 rises above 0.5 V, an overrvoltage condition is detected. Conversely, when the input is configures as a negative voltage and the inputs rises above 0.5 V, an undervoltage condition is detected. Tie to GND when not in use.
8	VL4	
9	GND	Device Ground.
10	REF	Buffered Reference Output. This pin is a 1 V reference that is used as an offset when monitoring negative voltages. This pin can source ro sink 1 mA and drive loads up to 1 nF. Larger capacitive loads may lead to instability. Leave unconnected when not in use.
11	$\overline{\text{OV}}$	Overvoltage Reset output. $\overline{\text{OV}}$ is asserted low if a negative polarity input voltage drops below its associated threshold or if a positive polarity input voltage exceeds its threshold. This device allows . $\overline{\text{OV}}$ to be latched low. This pin has a weak pull up to V_{CC} and can be pulled up to 16 V externally. Leave this pin unconnected when not in use.
12	$\overline{\text{UV}}$	Undervoltage Reset Output. . $\overline{\text{UV}}$ is asserted low if a negative polarity input voltage exceeds its associated threshold or if a positive polarity input voltage drops below its threshold. $\overline{\text{UV}}$ is held low for an adjustable time out period set by the external capacitor tied to the TIMER pin. The $\overline{\text{UV}}$ pin has a weak pull up to V_{CC} and can be pulled up to 16 V externally via an external pull up resistor. Leave this pin unconnected when not in use.

FIGURE 3. Terminal function.

Case outline X – Continued.		
Terminal number	**Mnemonic**	**Description**
13	$\overline{\text{LATCH}}$	$\overline{\text{OV}}$ Latch Bypass Input/Clear Pin. When pulled high, the $\overline{\text{OV}}$ latch is cleared. When held high, the $\overline{\text{OV}}$ output has the same delay and output characteristics as the $\overline{\text{UV}}$ output. When pulled low, the $\overline{\text{OV}}$ output is latched when asserted.
14	SEL	Input Polarity Select. This three state input pin allows the polarity of VH3, VL3, VH4 and VL4 to be configured. Connect to VCC or GND, or leave open to select one of three possible input polarity configurations.
15	TIMER	Adjustable Reset Delay Timer. Connect an external capacitor to the TIMER pin to program the reset timeout delay. Refer to FIGURE 5. Connect this pin to V_{CC} to bypass the timer.
16	V_{CC}	Supply Voltage. VCC operates as a direct supply for voltages up to 6 V. For voltages greater than 6 V, it operates as a shunt regulator. A dropper resistor must be used in this configuration to limit the current to less than 10 mA. When used without the resistor, the voltage at this pin must not exceed 6 V. A 0.1 µF bypass capacitor or greater should be used.

FIGURE 3. Terminal function - Continued.

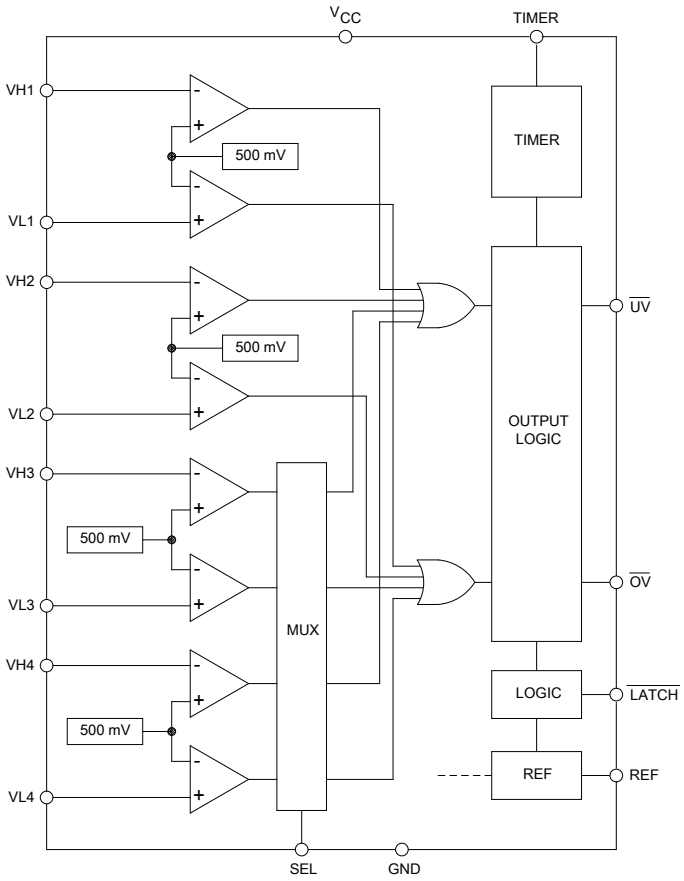


FIGURE 4. Functional block diagram

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12655
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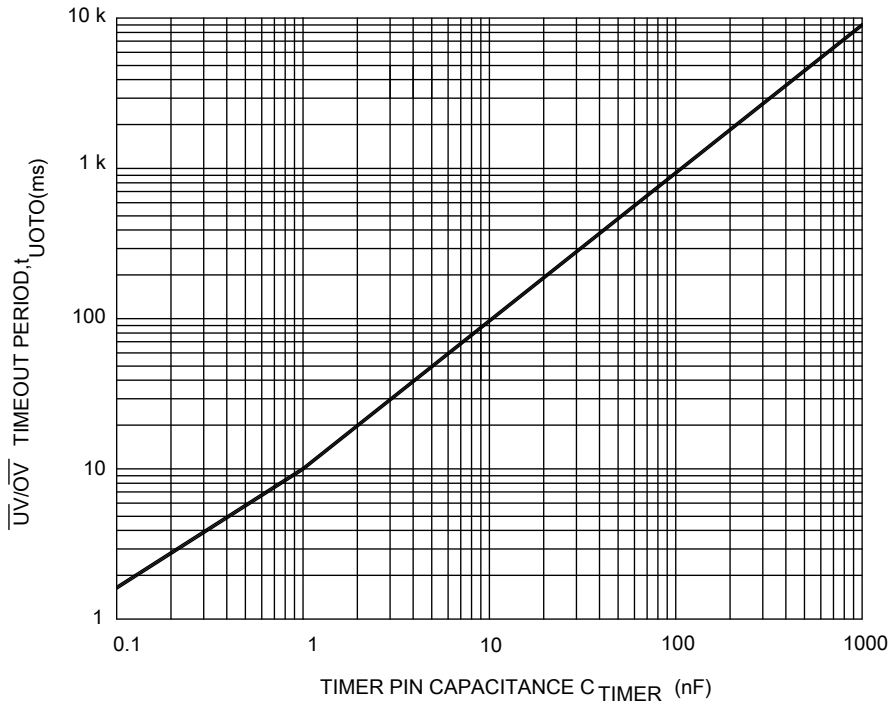

FIGURE 5. $\overline{UV}/\overline{OV}$ Timeout period vs Capacitance.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12655-01XE	24355	ADM2914-1SRQZEP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106