ANALOG
DEVICES

High Voltage, Latch-Up Proof, 4-/8-Channel Multiplexers

Data Sheet

ADG5208/ADG5209

FEATURES

Latch-up proof
2.9 pF off source capacitance
34 pF off drain capacitance
0.2 pC charge injection
Low on resistance: 160 Ω typical
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
48 V supply maximum ratings
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
V_{SS} to V_{DD} analog signal range
Human body model (HBM) ESD rating (TSSOP)
  8 kV I/O port to supplies
  2 kV I/O port to I/O port
  8 kV all other pins

APPLICATIONS

Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

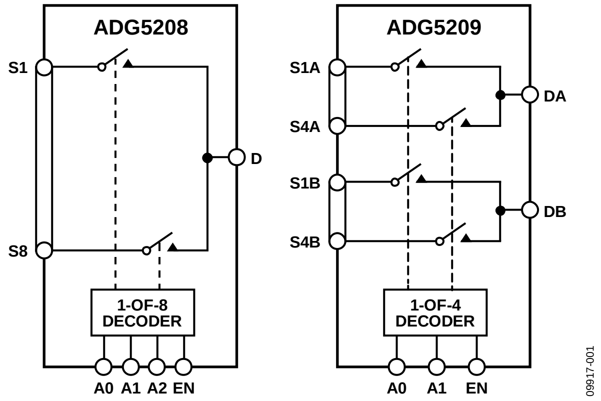

Figure 1.

GENERAL DESCRIPTION

The ADG5208/ADG5209 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG5208 switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The ADG5209 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1.

An EN input on both devices enables or disables the device. When EN is disabled, all channels switch off. The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make these devices suitable for video signal switching.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG5208/ADG5209 do not have V_L pins; instead, the logic power supply is generated internally by an on-chip voltage generator.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.
   A dielectric trench separates the P and N channel transistors to prevent latch-up even under severe overvoltage conditions.
2. 0.2 pC Charge Injection.
3. Dual-Supply Operation.
   For applications where the analog signal is bipolar, the ADG5208/ADG5209 can be operated from dual supplies of up to ±22 V.
4. Single-Supply Operation.
   For applications where the analog signal is unipolar, the ADG5208/ADG5209 can be operated from a single rail power supply of up to 40 V.
5. 3 V Logic-Compatible Digital Inputs.
   V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L Logic Power Supply Required.

Rev. B **Document Feedback**

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REVISION HISTORY

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3/12—Rev. 0 to Rev. A

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7/11—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	160			Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 37
	200	250	280	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	40			Ω typ	V_S = ±10 V, I_S = −1 mA
	50	65	70	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.005			nA typ	V_S = ±10 V, V_D = ∓ 10 V; see Figure 39
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.005			nA typ	V_S = ±10 V, V_D = ∓ 10 V; see Figure 39
	±0.1	±0.4	±1.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = ±10 V; see Figure 36
	±0.2	±0.5	±1.4	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	180	210	245	ns max	V_S = 10 V; see Figure 42
t_{ON} (EN)	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	150	185	215	ns max	V_S = 10 V; see Figure 44
t_{OFF} (EN)	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	210	230	ns max	V_S = 10 V; see Figure 44
Break-Before-Make Time Delay, t_D	55			ns typ	R_L = 300 Ω, C_L = 35 pF
			25	ns min	V_{S1} = V_{S2} = 10 V; see Figure 43
Charge Injection, Q_{INJ}	0.2			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 45
Off Isolation	−86			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5208	110			MHz typ	
ADG5209	240			MHz typ	
Insertion Loss	−6.4			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	2.9			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)					
ADG5208	34			pF typ	V_S = 0 V, f = 1 MHz
ADG5209	17			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	37			pF typ	V_S = 0 V, f = 1 MHz
ADG5209	21			pF typ	V_S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1] (LFCSP ONLY)					
Transition Time, $t_{TRANSITION}$	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	205	245	275	ns max	V_S = 10 V; see Figure 42
t_{ON} (EN)	145			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	220	245	ns max	V_S = 10 V; see Figure 44
t_{OFF} (EN)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	165	180	ns max	V_S = 10 V; see Figure 44
Break-Before-Make Time Delay, t_D	65			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 10 V; see Figure 43
Charge Injection, Q_{INJ}	0.4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 45
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5208	54			MHz typ	
ADG5209	133			MHz typ	
Insertion Loss	−6.4			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	5.5			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)					
ADG5208	52			pF typ	V_S = 0 V, f = 1 MHz
ADG5209	26			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	58			pF typ	V_S = 0 V, f = 1 MHz
ADG5209	31			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			μA typ	Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	140			Ω typ	V_S = ±15 V, I_S = −1 mA; see Figure 37
	160	200	230	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±15 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	34			Ω typ	V_S = ±15 V, I_S = −1 mA
	45	55	60	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.005			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 39
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.005			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 39
	±0.1	±0.4	±1.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = ±15 V; see Figure 36
	±0.2	±0.5	±1.4	nA max	

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	140			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	170	195	220	ns max	$V_S = 10$ V; see Figure 42
t_{ON} (EN)	120			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	140	170	195	ns max	$V_S = 10$ V; see Figure 44
t_{OFF} (EN)	160			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	185	205	220	ns max	$V_S = 10$ V; see Figure 44
Break-Before-Make Time Delay, t_D	45			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
			20	ns min	$V_{S1} = V_{S2} = 10$ V; see Figure 43
Charge Injection, Q_{INJ}	0.4			pC typ	$V_S = 0$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 45
Off Isolation	−86			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−80			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 41
ADG5208	121			MHz typ	
ADG5209	225			MHz typ	
Insertion Loss	−5.6			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 41
C_S (Off)	2.8			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (Off)					
ADG5208	33			pF typ	$V_S = 0$ V, f = 1 MHz
ADG5209	17			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	36			pF typ	$V_S = 0$ V, f = 1 MHz
ADG5209	21			pF typ	$V_S = 0$ V, f = 1 MHz
DYNAMIC CHARACTERISTICS[1] (LFCSP ONLY)					
Transition Time, $t_{TRANSITION}$	160			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	195	225	255	ns max	$V_S = 10$ V; see Figure 42
t_{ON} (EN)	145			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	170	200	225	ns max	$V_S = 10$ V; see Figure 44
t_{OFF} (EN)	120			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	140	155	170	ns max	$V_S = 10$ V; see Figure 44
Break-Before-Make Time Delay, t_D	55			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
			30	ns min	$V_{S1} = V_{S2} = 10$ V; see Figure 43
Charge Injection, Q_{INJ}	0.3			pC typ	$V_S = 0$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 45
Off Isolation	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 41
ADG5208	60			MHz typ	
ADG5209	130			MHz typ	
Insertion Loss	−5.6			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 41

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_S (Off)	5.5			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)					
ADG5208	51			pF typ	V_S = 0 V, f = 1 MHz
ADG5209	26			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	57			pF typ	V_S = 0 V, f = 1 MHz
ADG5209	31			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			µA typ	Digital inputs = 0 V or V_{DD}
	70		110	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	350			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA; see Figure 37
	500	610	700	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	20	22	24	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	160			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	280	335	370	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.005			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 39
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.005			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 39
	±0.1	±0.4	±1.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = 1 V/10 V; see Figure 36
	±0.2	±0.5	±1.4	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	250	295	335	ns max	V_S = 8 V; see Figure 42
t_{ON} (EN)	180			ns typ	R_L = 300 Ω, C_L = 35 pF
	225	280	320	ns max	V_S = 8 V; see Figure 44
t_{OFF} (EN)	165			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	225	245	ns max	V_S = 8 V; see Figure 44
Break-Before-Make Time Delay, t_D	95			ns typ	R_L = 300 Ω, C_L = 35 pF
			50	ns min	V_{S1} = V_{S2} = 8 V; see Figure 43

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Charge Injection, Q_{INJ}	0.2			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 45
Off Isolation	−86			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5208	95			MHz typ	
ADG5209	180			MHz typ	
Insertion Loss	−8.9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	3.3			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)					
ADG5208	38			pF typ	V_S = 6 V, f = 1 MHz
ADG5209	19			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	41			pF typ	V_S = 6 V, f = 1 MHz
ADG5209	24			pF typ	V_S = 6 V, f = 1 MHz
DYNAMIC CHARACTERISTICS[1] (LFCSP Only)					
Transition Time, $t_{TRANSITION}$	210			ns typ	R_L = 300 Ω, C_L = 35 pF
	270	330	380	ns max	V_S = 8 V; see Figure 42
t_{ON} (EN)	215			ns typ	R_L = 300 Ω, C_L = 35 pF
	275	345	400	ns max	V_S = 8 V; see Figure 44
t_{OFF} (EN)	115			ns typ	R_L = 300 Ω, C_L = 35 pF
	140	160	175	ns max	V_S = 8 V; see Figure 44
Break-Before-Make Time Delay, t_D	135			ns typ	R_L = 300 Ω, C_L = 35 pF
			70	ns min	V_{S1} = V_{S2} = 8 V; see Figure 43
Charge Injection, Q_{INJ}	0.3			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 45
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5208	60			MHz typ	
ADG5209	120			MHz typ	
Insertion Loss	−8.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	6			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)					
ADG5208	56			pF typ	V_S = 6 V, f = 1 MHz
ADG5209	28			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	63			pF typ	V_S = 6 V, f = 1 MHz
ADG5209	35			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			µA typ	Digital inputs = 0 V or V_{DD}
	50		65	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	150			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA; see Figure 37
	170	215	245	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	35			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	55	65	70	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.005			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 39
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.005			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 39
	±0.1	±0.4	±1.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = 1 V/30 V; see Figure 36
	±0.2	±0.5	±1.4	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	205	225	235	ns max	V_S = 18 V; see Figure 42
t_{ON} (EN)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	180	195	215	ns max	V_S = 18 V; see Figure 44
t_{OFF} (EN)	180			ns typ	R_L = 300 Ω, C_L = 35 pF
	225	225	230	ns max	V_S = 18 V; see Figure 44
Break-Before-Make Time Delay, t_D	55			ns typ	R_L = 300 Ω, C_L = 35 pF
			25	ns min	V_{S1} = V_{S2} = 18 V; see Figure 43
Charge Injection, Q_{INJ}	0.3			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 45
Off Isolation	−86			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5208	105			MHz typ	
ADG5209	195			MHz typ	
Insertion Loss	−6.2			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	2.7			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)					
ADG5208	32			pF typ	V_S = 18 V, f = 1 MHz
ADG5209	16			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	35			pF typ	V_S = 18 V, f = 1 MHz
ADG5209	20			pF typ	V_S = 18 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1] (LFCSP ONLY)					
Transition Time, $t_{TRANSITION}$	185			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	230	245	259	ns max	$V_S = 18$ V; see Figure 42
t_{ON} (EN)	170			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	210	230	255	ns max	$V_S = 18$ V; see Figure 44
t_{OFF} (EN)	125			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	180	180	180	ns max	$V_S = 18$ V; see Figure 44
Break-Before-Make Time Delay, t_D	70			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
			35	ns min	$V_{S1} = V_{S2} = 18$ V; see Figure 43
Charge Injection, Q_{INJ}	0.4			pC typ	$V_S = 18$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 45
Off Isolation	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 40
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 38
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 41
ADG5208	65			MHz typ	
ADG5209	130			MHz typ	
Insertion Loss	−6			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 41
C_S (Off)	5.5			pF typ	$V_S = 18$ V, f = 1 MHz
C_D (Off)					
ADG5208	51			pF typ	$V_S = 18$ V, f = 1 MHz
ADG5209	25			pF typ	$V_S = 18$ V, f = 1 MHz
C_D (On), C_S (On)					
ADG5208	57			pF typ	$V_S = 18$ V, f = 1 MHz
ADG5209	32			pF typ	$V_S = 18$ V, f = 1 MHz
POWER REQUIREMENTS					$V_{DD} = 39.6$ V
I_{DD}	80			µA typ	Digital inputs = 0 V or V_{DD}
	100		130	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, $V_{SS} = 0$ V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx, D, OR Dx

Table 5. ADG5208

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	40	24	14.5	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	69	37	18	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	42	26.5	14.5	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	75	40	18	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	28	19	12	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	40	25	14.5	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	40	26	14.5	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	72	39	18	mA maximum

Table 6. ADG5209

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	29	19	12	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	51	30	16	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	30	20	12.5	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	55	32	17	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	20	14	10	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	29	20	12.5	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	30	20	12.5	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	54	31	17	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx, D, or Dx Pins	
ADG5208	126 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5209	92 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx, D, or Dx Pins[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C
HBM ESD (TSSOP)	
I/O Port to Supplies	8 kV
I/O Port to I/O Port	2 kV
All Other Pins	8 kV
HBM ESD (LFCSP)	
I/O Port to Supplies	4 kV
I/O Port to I/O Port	1 kV
All Other Pins	4 kV

[1] Overvoltages at the Ax, EN, Sx, D, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

[2] See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

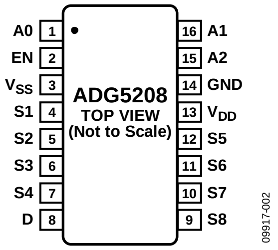
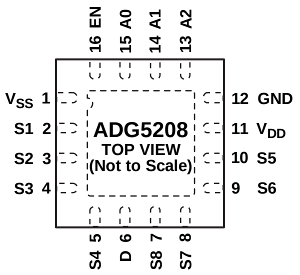


Figure 2. ADG5208 Pin Configuration (TSSOP)



NOTES
1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

09917-003

Figure 3. ADG5208 Pin Configuration (LFCSP)

Table 8. ADG5208 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, the Ax logic inputs determine the on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1	Source Terminal 1. This pin can be an input or an output.
5	3	S2	Source Terminal 2. This pin can be an input or an output.
6	4	S3	Source Terminal 3. This pin can be an input or an output.
7	5	S4	Source Terminal 4. This pin can be an input or an output.
8	6	D	Drain Terminal. This pin can be an input or an output.
9	7	S8	Source Terminal 8. This pin can be an input or an output.
10	8	S7	Source Terminal 7. This pin can be an input or an output.
11	9	S6	Source Terminal 6. This pin can be an input or an output.
12	10	S5	Source Terminal 5. This pin can be an input or an output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 9. ADG5208 Truth Table

A2	A1	A0	EN	On Switch
X[1]	X[1]	X[1]	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X is don't care.

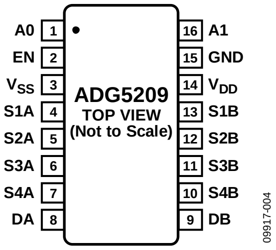
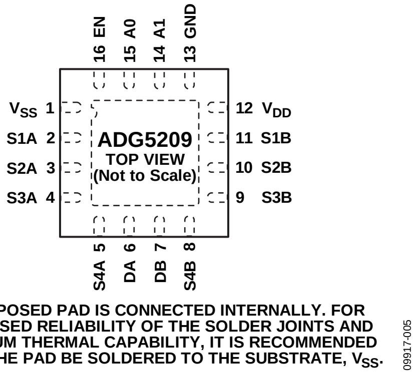


Figure 4. ADG5209 Pin Configuration (TSSOP)



NOTES
1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 5. ADG5209 Pin Configuration (LFCSP)

Table 10. ADG5209 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine the on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1A	Source Terminal 1A. This pin can be an input or an output.
5	3	S2A	Source Terminal 2A. This pin can be an input or an output.
6	4	S3A	Source Terminal 3A. This pin can be an input or an output.
7	5	S4A	Source Terminal 4A. This pin can be an input or an output.
8	6	DA	Drain Terminal A. This pin can be an input or an output.
9	7	DB	Drain Terminal B. This pin can be an input or an output.
10	8	S4B	Source Terminal 4B. This pin can be an input or an output.
11	9	S3B	Source Terminal 3B. This pin can be an input or an output.
12	10	S2B	Source Terminal 2B. This pin can be an input or an output.
13	11	S1B	Source Terminal 1B. This pin can be an input or an output.
14	12	V_{DD}	Most Positive Power Supply Potential.
15	13	GND	Ground (0 V) Reference.
16	14	A1	Logic Control Input.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG5209 Truth Table

A1	A0	EN	On Switch Pair
X[1]	X[1]	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

[1] X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

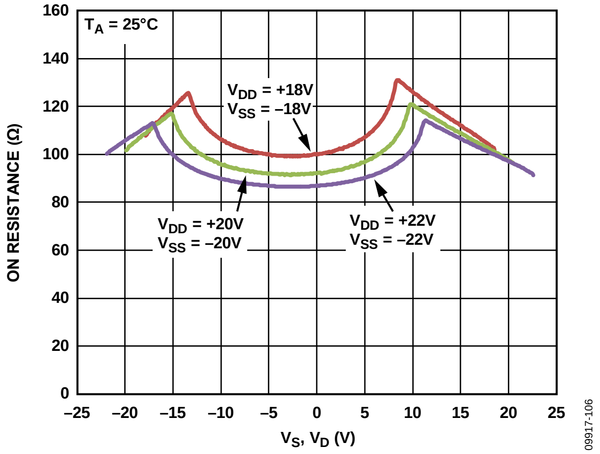


Figure 6. R_{ON} as a Function of V_S, V_D (±20 V Dual Supply)

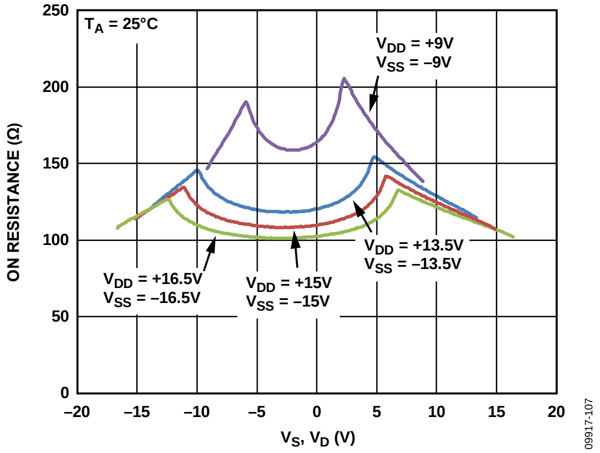


Figure 7. R_{ON} as a Function of V_S, V_D (±15 V Dual Supply)

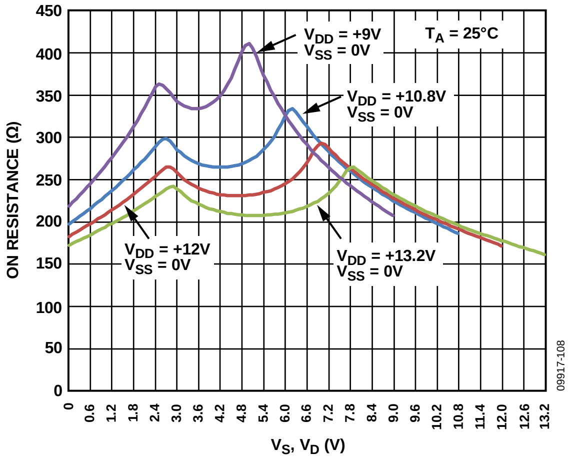


Figure 8. R_{ON} as a Function of V_S, V_D (12 V Single Supply)

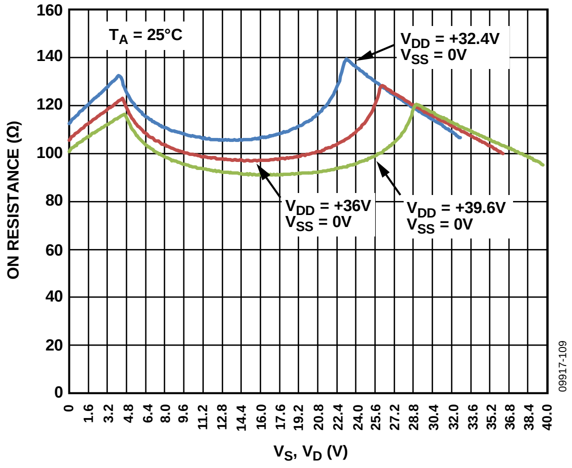


Figure 9. R_{ON} as a Function of V_S, V_D (36 V Single Supply)

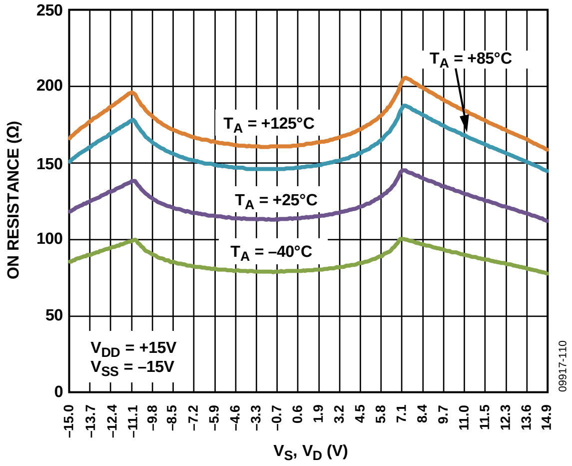


Figure 10. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±15 V Dual Supply

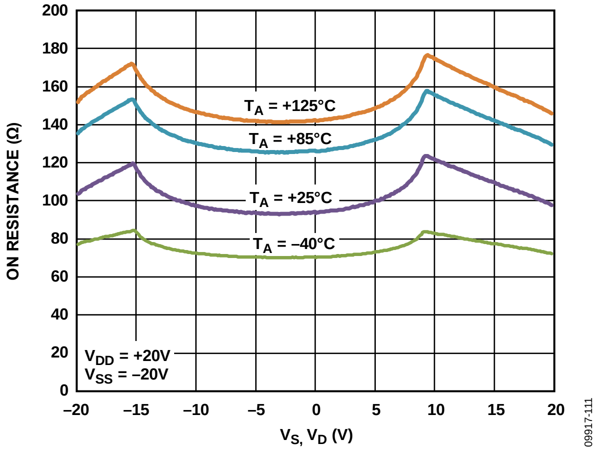


Figure 11. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±20 V Dual Supply

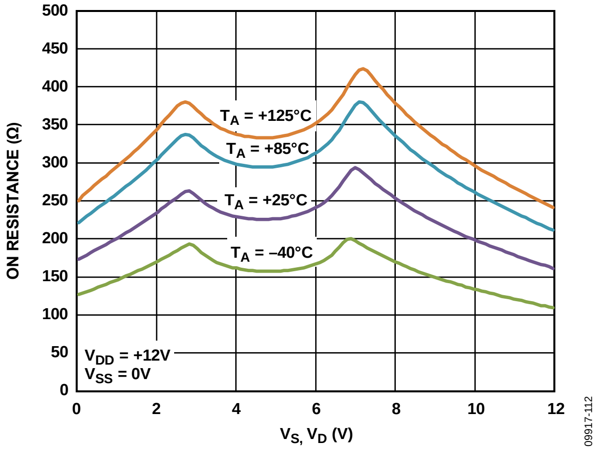


Figure 12. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

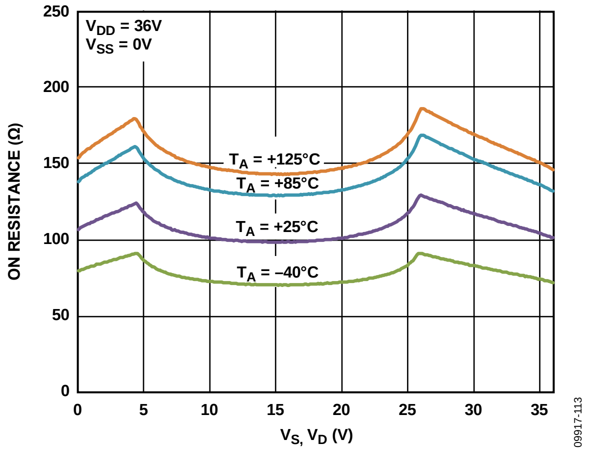


Figure 13. R_{ON} as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

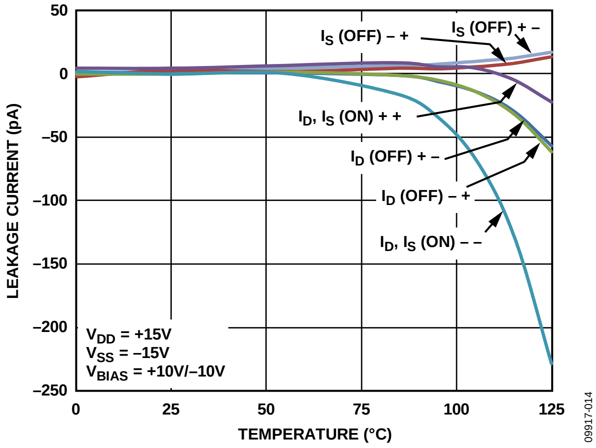


Figure 14. Leakage Currents vs. Temperature, ±15 V Dual Supply

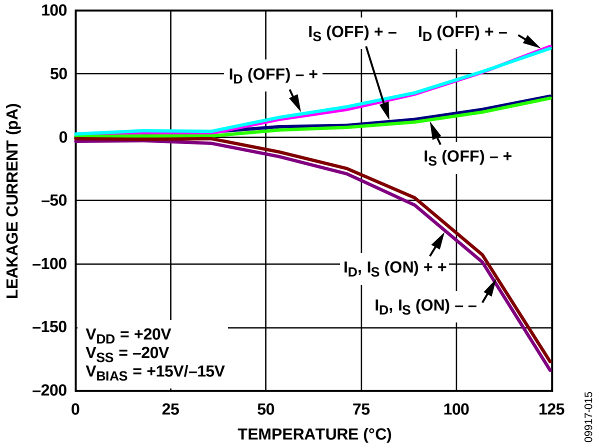


Figure 15. Leakage Currents vs. Temperature, ±20 V Dual Supply

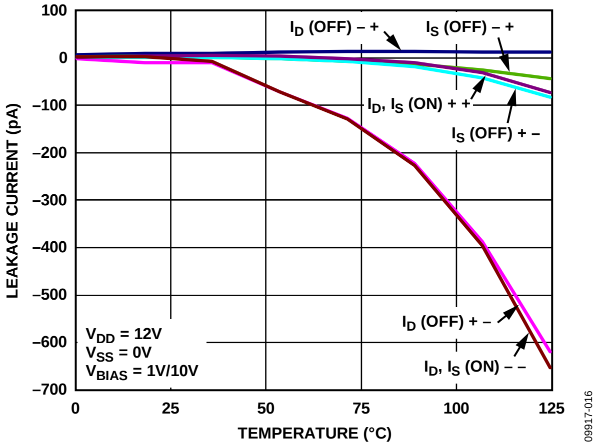


Figure 16. Leakage Currents vs. Temperature, 12 V Single Supply

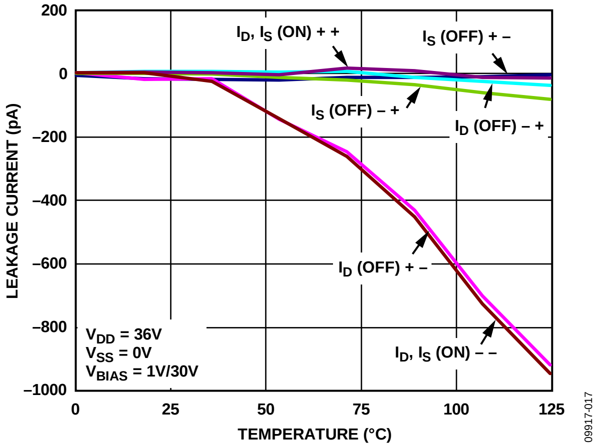


Figure 17. Leakage Currents vs. Temperature, 36 V Single Supply

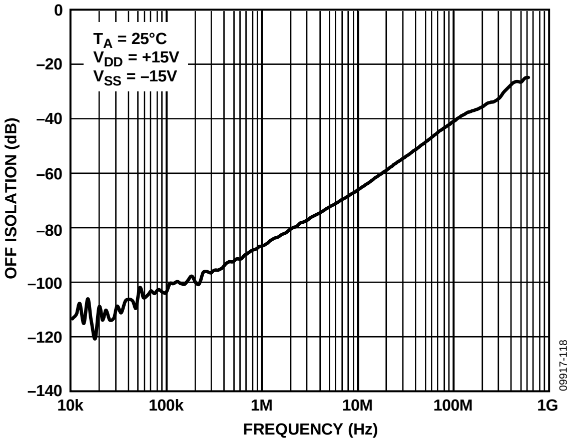


Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply (TSSOP)

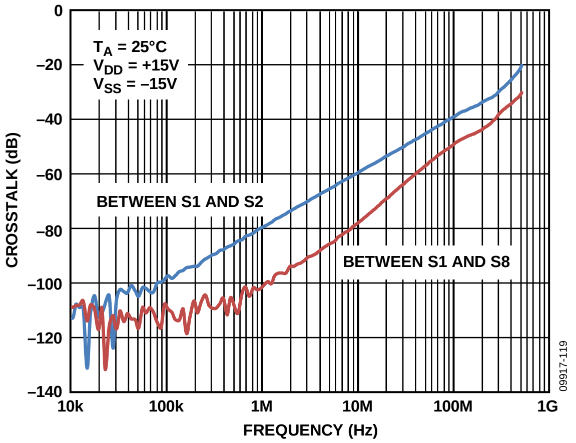


Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply (TSSOP)

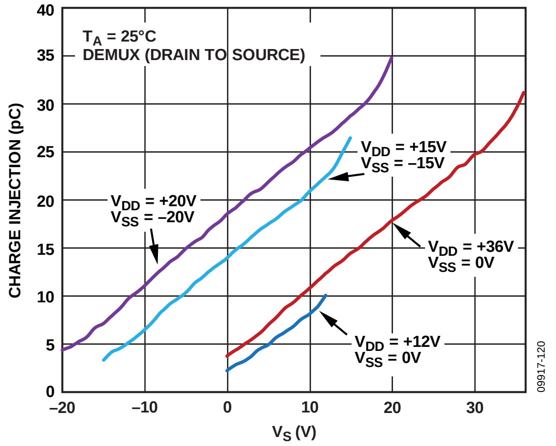


Figure 20. Charge Injection vs. Source Voltage, Drain to Source (TSSOP)

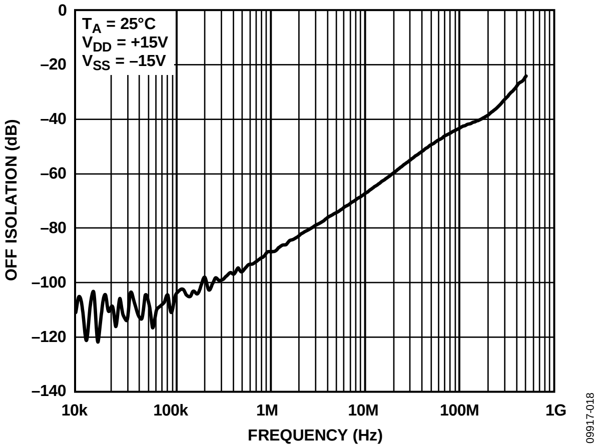


Figure 21. Off Isolation vs. Frequency, ±15 V Dual Supply (LFCSP)

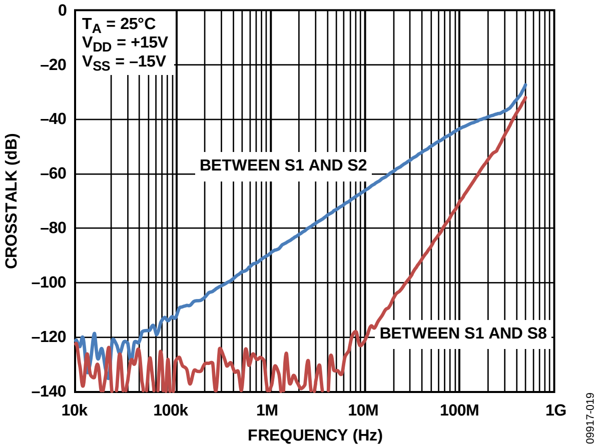


Figure 22. Crosstalk vs. Frequency, ±15 V Dual Supply (LFCSP)

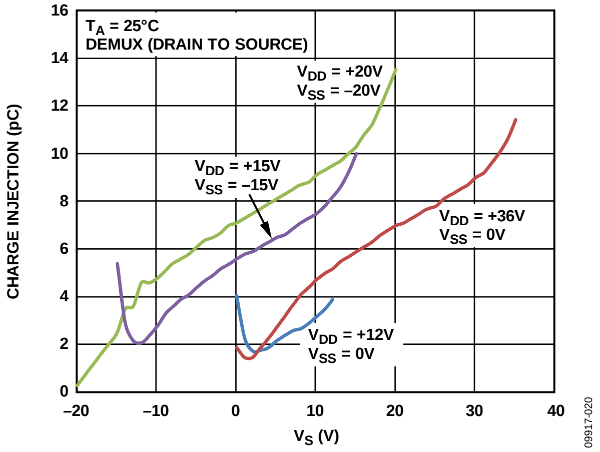


Figure 23. Charge Injection vs. Source Voltage, Drain to Source (LFCSP)

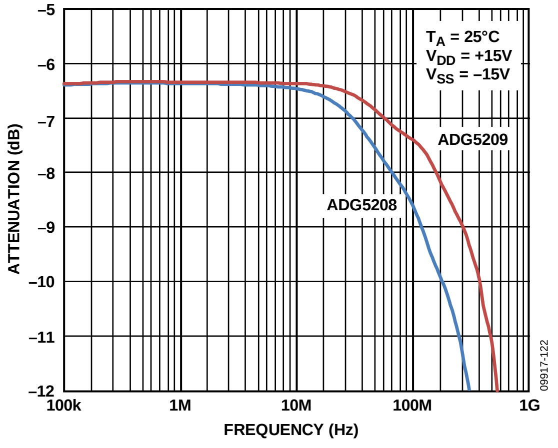


Figure 24. Bandwidth (TSSOP)

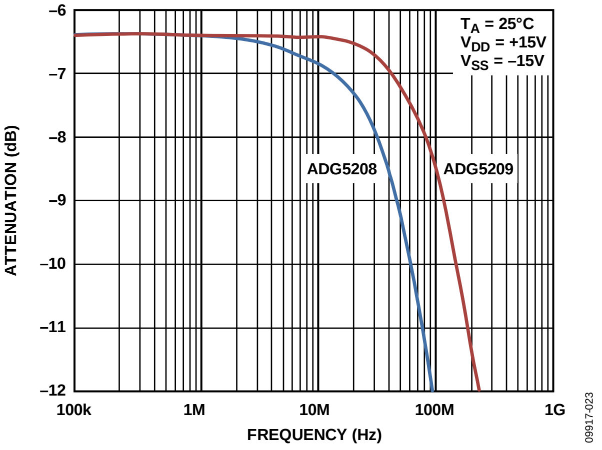


Figure 27. Bandwidth (LFCSP)

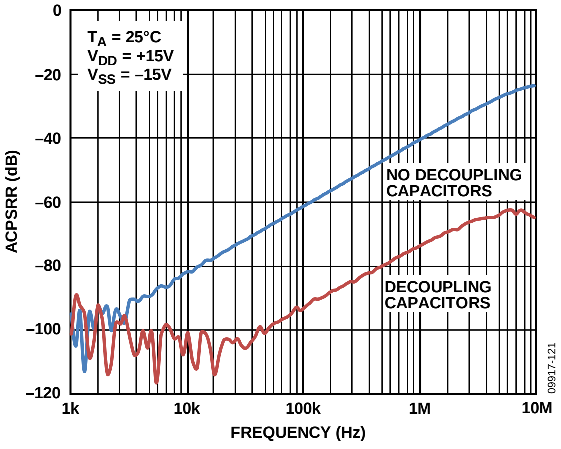


Figure 25. ACPSRR vs. Frequency, ±15 V Dual Supply (TSSOP)

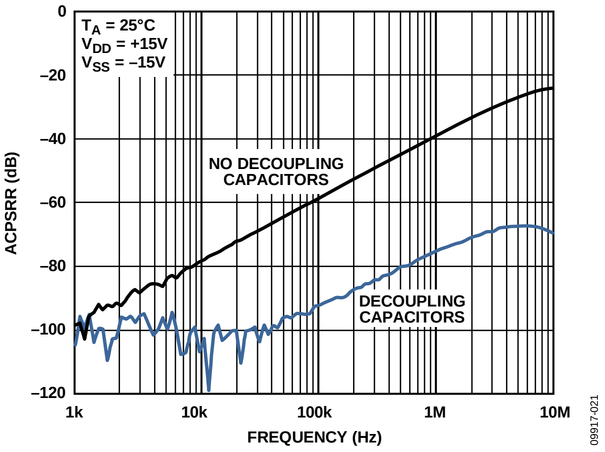


Figure 28. ACPSRR vs. Frequency, ±15 V Dual Supply (LFCSP)

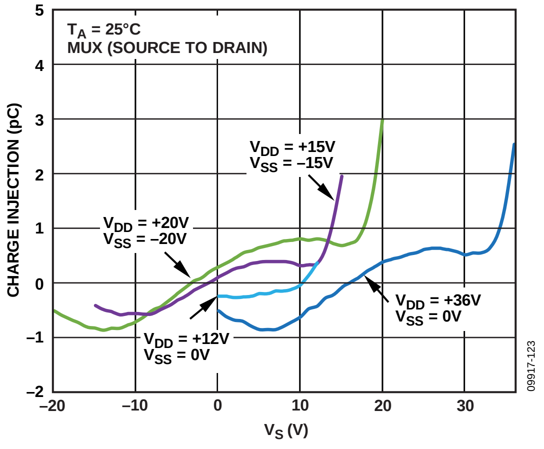


Figure 26. Charge Injection vs. Source Voltage, Source to Drain (TSSOP)

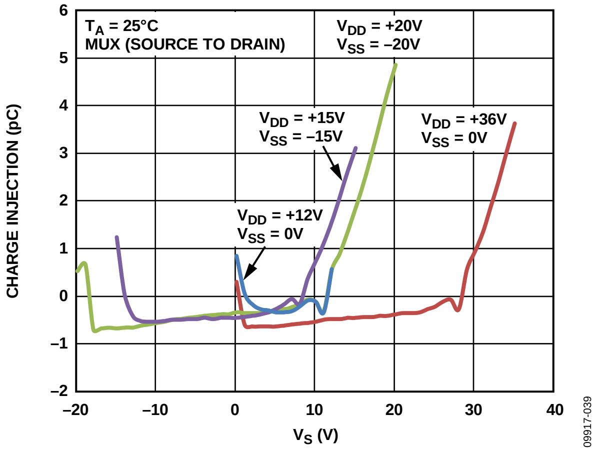


Figure 29. Charge Injection vs. Source Voltage, Source to Drain (LFCSP)

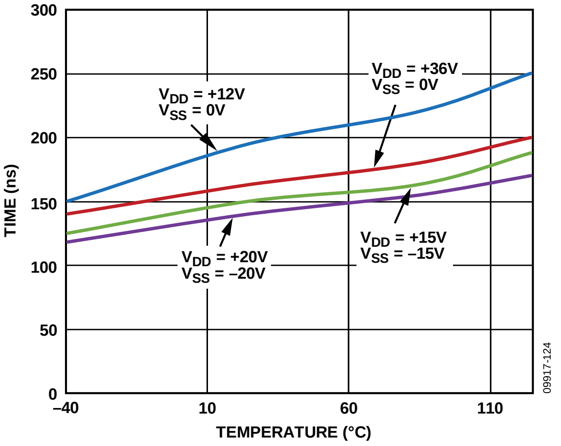


Figure 30. $t_{TRANSITION}$ Times vs. Temperature (TSSOP)

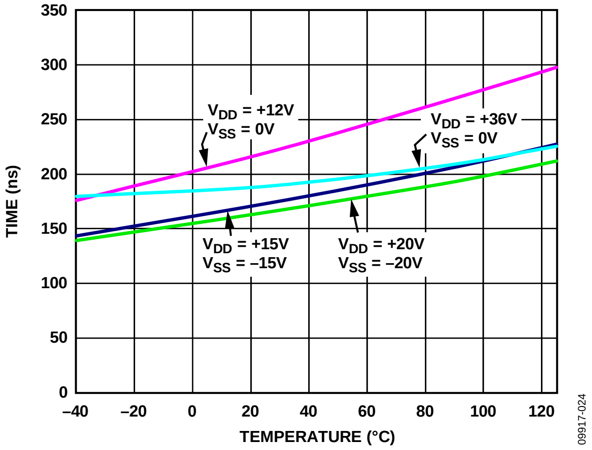


Figure 33. $t_{TRANSITION}$ Times vs. Temperature (LFCSP)

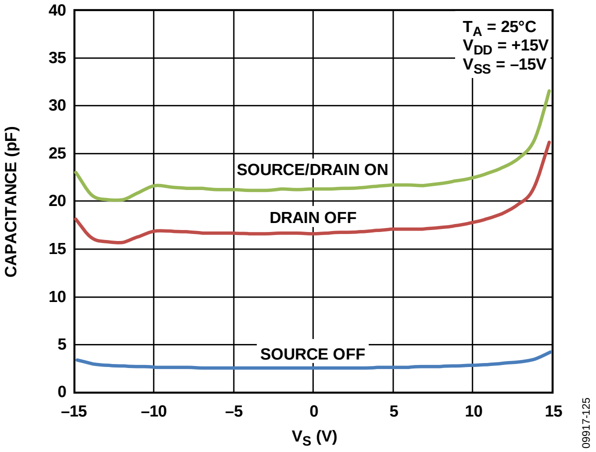


Figure 31. ADG5209 Capacitance vs. Source Voltage, ±15 V Dual Supply (TSSOP)

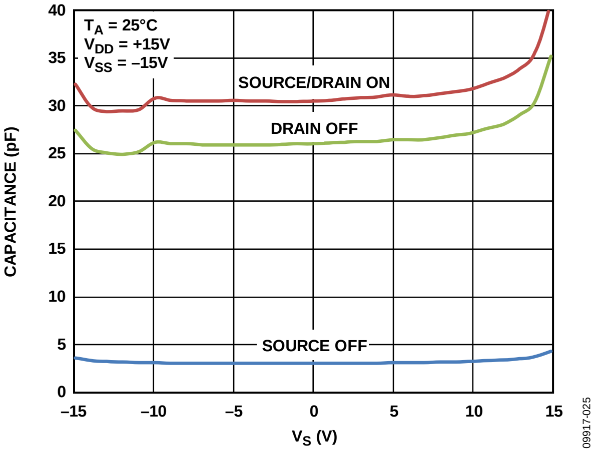


Figure 34. ADG5209 Capacitance vs. Source Voltage, ±15 V Dual Supply (LFCSP)

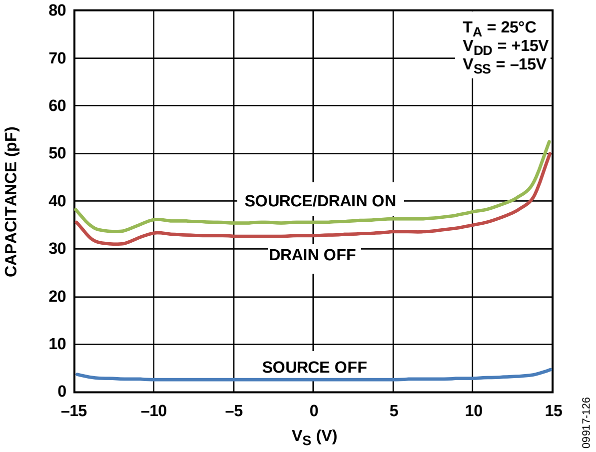


Figure 32. ADG5208 Capacitance vs. Source Voltage, ±15 V Dual Supply (TSSOP)

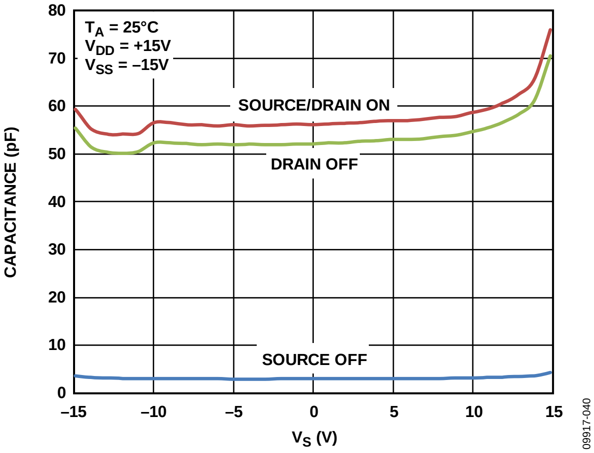


Figure 35. ADG5208 Capacitance vs. Source Voltage, ±15 V Dual Supply (LFCSP)

TEST CIRCUITS

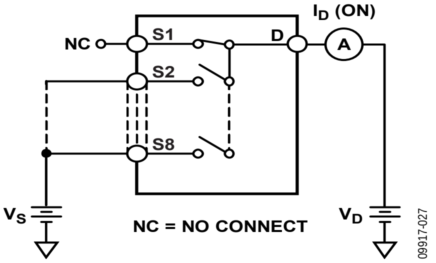


Figure 36. On Leakage

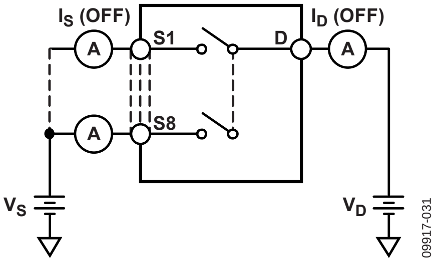


Figure 39. Off Leakage

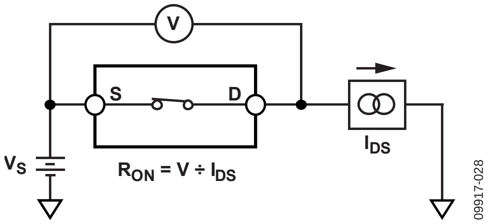


Figure 37. On Resistance

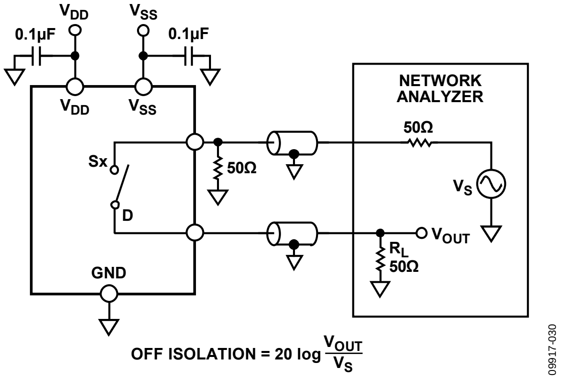


Figure 40. Off Isolation

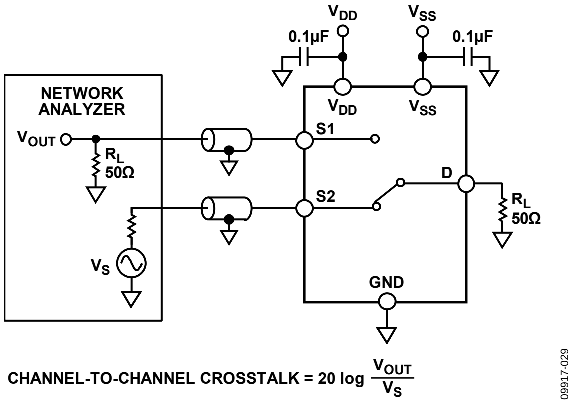


Figure 38. Channel-to-Channel Crosstalk

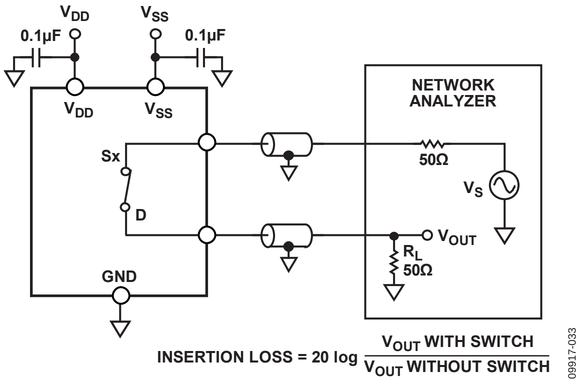
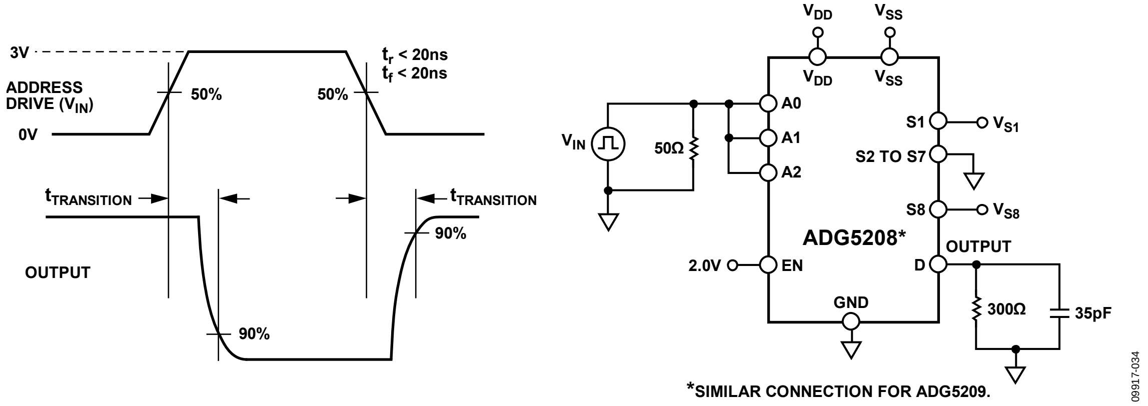
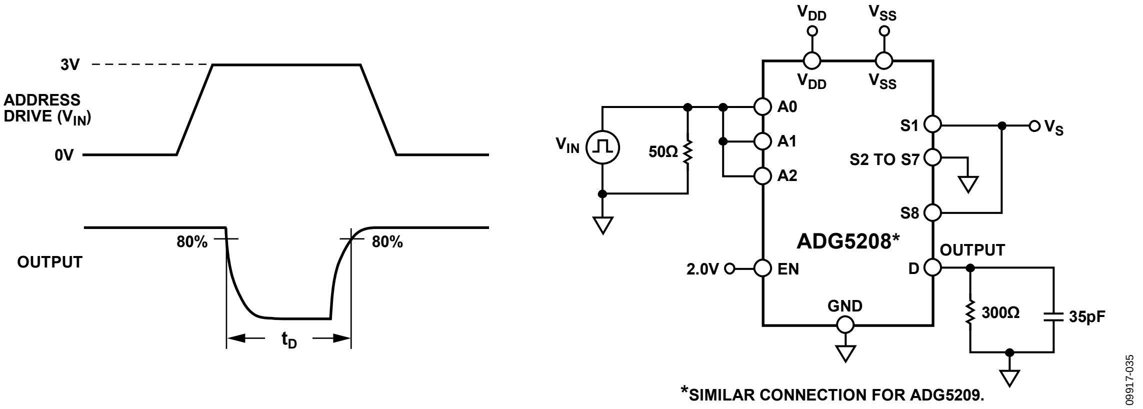


Figure 41. Bandwidth



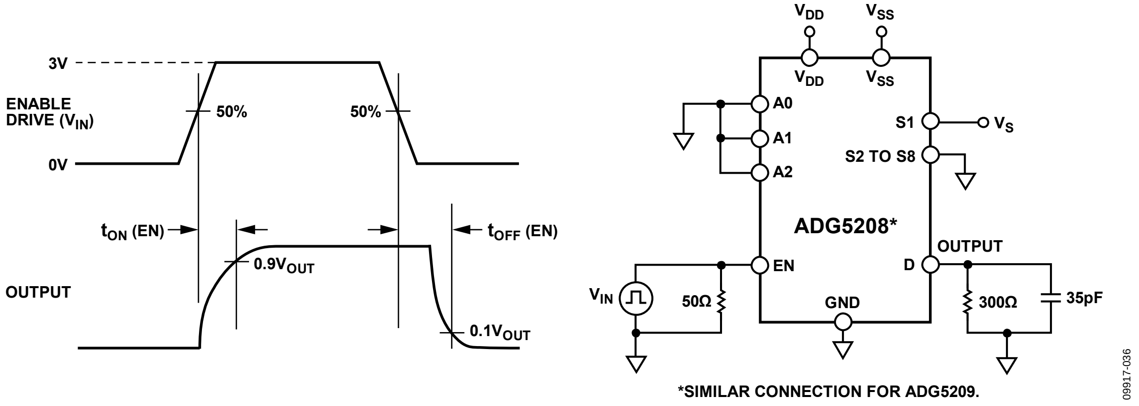
*SIMILAR CONNECTION FOR ADG5209.

Figure 42. Address to Output Switching Times, $t_{TRANSITION}$



*SIMILAR CONNECTION FOR ADG5209.

Figure 43. Break-Before-Make Time Delay, t_D



*SIMILAR CONNECTION FOR ADG5209.

Figure 44. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

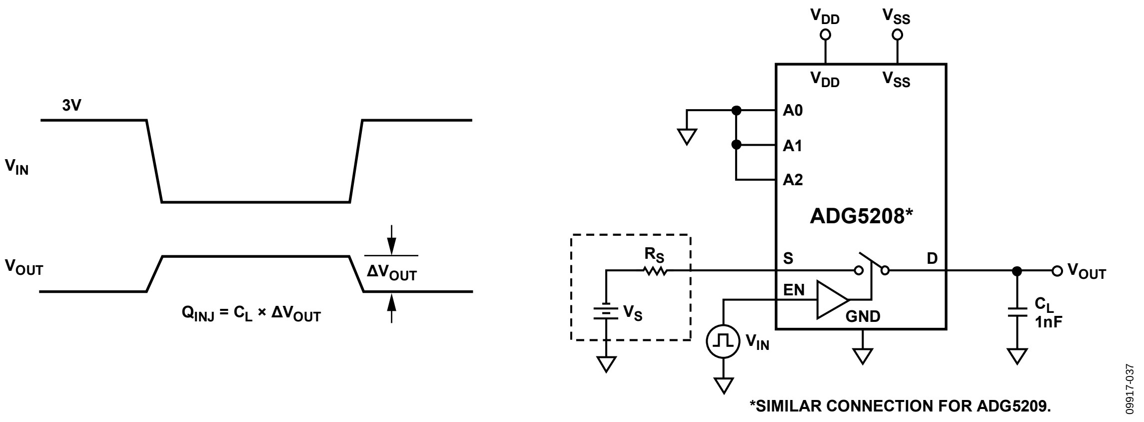


Figure 45. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

t_{ON} (EN)

t_{ON} (EN) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

t_{OFF} (EN) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

Break-Before-Make Time Delay (t_D)

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is a measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the ADG5208/ADG5209, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

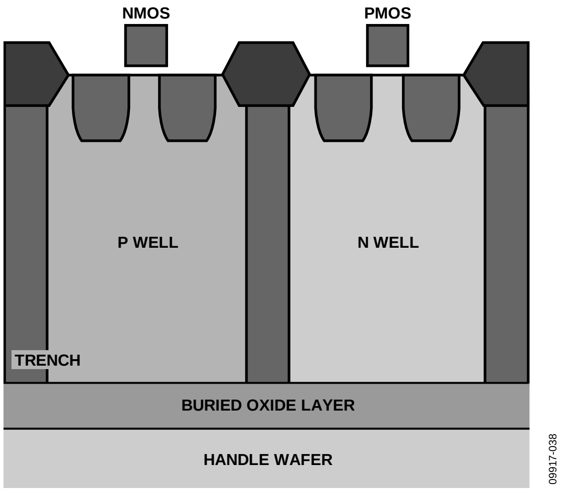
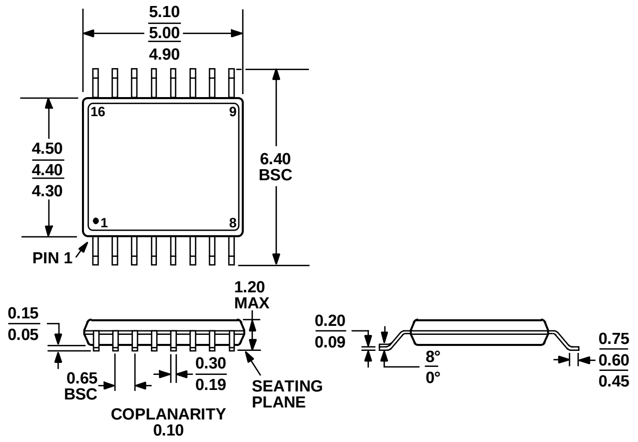


Figure 46. Trench Isolation

APPLICATIONS INFORMATION

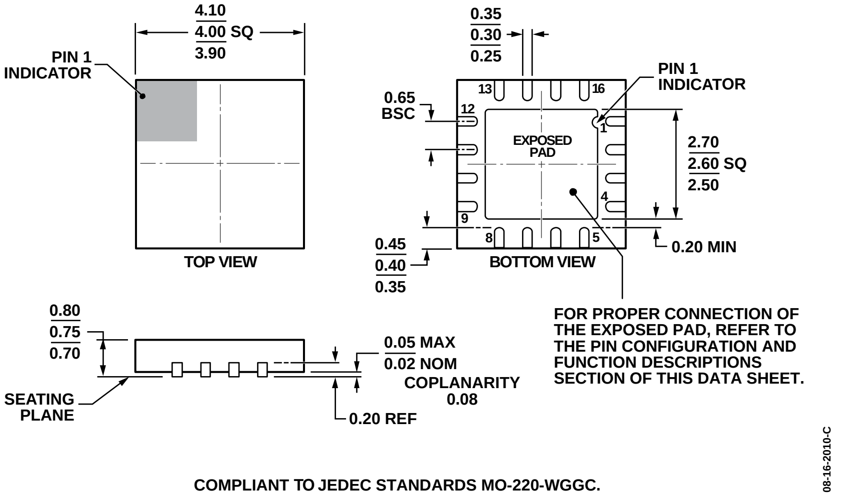
The ADG52xx family of switches and multiplexers provides a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persist until the power supply is turned off. The ADG5208/ADG5209 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 47. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5208BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
ADG5208BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5208BRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5209BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
ADG5209BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5209BRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

[1] Z = RoHS Compliant Part.

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