Panasonic

AN32051A

http://www.semicon.panasonic.co.jp/en/

7 x 7 Dots Matrix LED Driver LSI

FEATURES

- 7 x 7 LED Matrix Driver
  (Total LED that can be driven = 49)
- Built-in memory (ROM, RAM)
- LDO : 2-ch
- SPI interface : 1-ch
- LED driver for RGB : 1-ch
- 35 pin Wafer Level Chip Size Package (WLCSP)

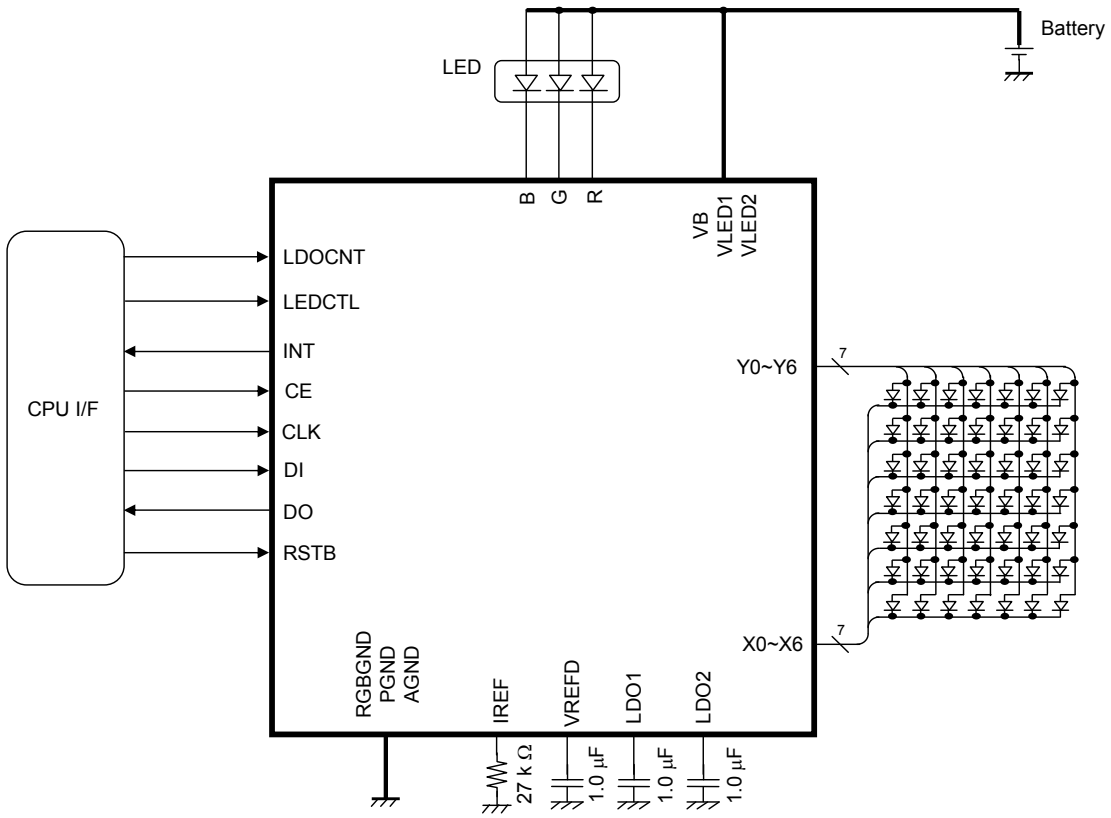
DESCRIPTION

AN32051A is a 49 Dots Matrix LED Driver. It can drive up to 16 RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	LEDCTL, RSTB, CE, CLK, DI	– 0.3 to 3.4	V	—
	LDOCNT	– 0.3 to 6.0	V	—
Output Voltage Range	INT, DO	– 0.3 to 3.4	V	—
	R, G, B, LDO1, LDO2, X0, X1, X2, X3, X4, X5, X6, Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3 to 6.5	V	—
ESD	HBM	2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: VB_{MAX} = VB, $VLED_{MAX}$ = VLED.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
35 pin Wafer Level Chip Size Package (WLCSP)	141.5 °C /W	0.706 W	0.304 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VB	3.1	3.7	4.6	V	*1
	VLED	3.1	5.0	5.6	V	*1
Input Voltage Range	LEDCTL, RSTB, CE, CLK, DI	– 0.3	—	3.0	V	—
	LDOCNT	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	INT, DO	– 0.3	—	3.0	V	—
	R, G, B, LDO1, LDO2, X0, X1, X2, X3, X4, X5, X6, Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, RGBGND and PGND.
VB is voltage for VB. VLED is voltage for VLED1 and VLED2.
*2: (VB + 0.3) V must not exceed 6 V. (VLED + 0.3) V must not exceed 6.5 V.

ELECTRICAL CHARACTERISTICS

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1)	ICC1	At OFF mode LDOCNT = Low	—	0	1	μA	—
Current consumption (2)	ICC2	At Standby mode LDOCNT = Low LDO2 is active.	—	8	12	μA	—
Current consumption (3)	ICC3	LDOCNT = High LDO1 and LDO2 are active.	—	18	24	μA	—
Reference voltage							
Output voltage	VREF	I_{VREF} = 0 μA	1.22	1.25	1.28	V	—
Reference current							
Output voltage	VIREF	I_{IREF} = 0 μA	0.44	0.54	0.64	V	—
Voltage regulator (LDO1)							
Output voltage	VL1	I_{LDO1} = – 30 mA	1.79	1.85	1.91	V	—
Short circuit protection current	IPT1	LDOCNT = High REG18 = High V_{LDO1} = 0 V, IPT1 = I_{LDO1}	50	100	200	mA	—
Ripple rejection (1)	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO1} = – 15 mA PSL11 = 20log (acV_{LDO1} / 0.2)	—	– 45	– 40	dB	—
Ripple rejection (2)	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO1} = – 15 mA PSL12 = 20log (acV_{LDO1} / 0.2)	—	– 35	– 25	dB	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO2)							
Output voltage	VL2	I_{LDO2} = – 30 mA	2.76	2.85	2.94	V	—
Short circuit protection current	IPT2	LDOCNT = High V_{LDO2} = 0V IPT2 = I_{LDO2}	50	100	300	mA	—
Ripple rejection (1)	PSL21	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO2} = – 15 mA PSL21 = 20log (acV_{LDO2} / 0.2)	—	– 40	– 30	dB	—
Ripple rejection (2)	PSL22	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO2} = – 15 mA PSL22 = 20log (acV_{LDO2} / 0.2)	—	– 25	– 15	dB	—
Oscillator							
Oscillation frequency	FDC	—	0.96	1.20	1.44	MHz	—
SCAN Switch							
Resistance at the Switch ON	RSCAN	$I_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ = 5 mA RSCAN = $V_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ / 5 mA	—	2	4.8	Ω	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For 7 × 7 dots matrix LED)							
Output current (1)	IMX1	At 1mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX1 = $I_{X0, X1, X2, X3, X4, X5, X6}$	0.952	1.035	1.118	mA	*1
Output current (2)	IMX2	At 2 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX2 = $I_{X0, X1, X2, X3, X4, X5, X6}$	1.923	2.090	2.258	mA	*1
Output current (3)	IMX4	At 4 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX4 = $I_{X0, X1, X2, X3, X4, X5, X6}$	3.843	4.177	4.512	mA	*1
Output current (4)	IMX8	At 8 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX8 = $I_{X0, X1, X2, X3, X4, X5, X6}$	7.692	8.361	9.030	mA	*1
Output current (5)	IMX15	At 15 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX15 = $I_{X0, X1, X2, X3, X4, X5, X6}$	14.399	15.651	16.903	mA	*1
Leakage Current when matrix LED turns off	IMXOFF	Current OFF setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 4.75 V IMXOFF = $I_{X0, X1, X2, X3, X4, X5, X6}$	—	—	1	μA	—
The error between channels	IMXCH	The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*1 : Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For RGB color unit)							
Output current (1)	IRGB1	At 1mA setup $V_{R, G, B}$ = 1 V	0.949	1.031	1.114	mA	*1
Output current (2)	IRGB2	At 2 mA setup $V_{R, G, B}$ = 1 V	1.901	2.066	2.231	mA	*1
Output current (3)	IRGB4	At 4 mA setup $V_{R, G, B}$ = 1 V	3.781	4.110	4.438	mA	*1
Output current (4)	IRGB8	At 8 mA setup $V_{R, G, B}$ = 1 V	7.554	8.210	8.867	mA	*1
Leakage Current when RGB turn off	IRGBOFF	Current OFF setup $V_{R, G, B}$ = 4.75 V IRGBOFF = $I_{R, G, B}$	—	—	1	μA	—
The error between channels	IRGBCH	The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*1 : Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI I/F, LEDCTL, RSTB							
Input voltage range of High-level	VIH	High-level recognition voltage	1.38	—	LDO2 + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	–0.3	—	0.4	V	—
Input current of High-level	IIH	$V_{LEDCTL, RSTB, CE, CLK, DI}$ = 1.85 V IIH = $I_{LEDCTL, RSTB, CE, CLK, DI}$	—	0	1	µA	—
Input current of Low-level	IIL	$V_{LEDCTL, RSTB, CSB, CLK, DI}$ = 0 V IIL = $I_{LEDCTL, RSTB, CE, CLK, DI}$	—	0	1	µA	—
INT							
Output voltage of High-level (1)	VOH1	I_{INT} = – 2 mA VDDSEL = LDO2	LDO2 × 0.8	—	—	V	—
Output voltage of Low-level (1)	VOL1	I_{INT} = 2 mA VDDSEL = LDO2 (I_{INT} = 0.5 mA)	—	—	LDO2 × 0.2	V	—
Output voltage of High-level (2)	VOH2	I_{INT} = – 2 mA VDDSEL = LDO1	LDO1 × 0.8	—	—	V	—
Output voltage of Low-level (2)	VOL2	I_{INT} = 2 mA VDDSEL = LDO1 (I_{INT} = 0.5 mA)	—	—	LDO1 × 0.3	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LDOCNT							
Input voltage range of High-level	VIH	High-level recognition voltage	VB × 0.7	—	VB + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	V_{LDOCNT} = 3.6 V IIH = I_{LDOCNT}	—	0	1	µA	—
Input current of Low-level	IIL	V_{LDOCNT} = 0 V IIL = I_{LDOCNT}	—	0	1	µA	—
DO							
Output voltage of High-level	VOH	I_{DO} = – 2 mA	LDO1 × 0.8	—	—	V	—
Output voltage of Low-level	VOL	I_{DO} = 2 mA	—	—	LDO1 × 0.2	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO1) Output capacitor 1 µF, Output capacitor's ESR less than 0.1 Ω							
Rise time	Tsu1	Time until output voltage reaches to 0 V to 90%	—	0.25	—	ms	*2 *3
Fall time	Tsd1	Time until output voltage reaches to 10%	—	5	—	ms	*2 *3
Maximum load current	IOMAX1	—	—	15	—	mA	*3
Load transient response (1)	Vtr11	I_{LDO1} = – 50 µA → – 15 mA (1 µs)	—	70	—	mV	*3
Load transient response (2)	Vtr12	I_{LDO1} = – 15 mA → – 50 µA (1 µs)	—	70	—	mV	*3
Voltage regulator (LDO2) Output capacitor 1 µF, Output capacitor's ESR less than 0.1 Ω							
Rise time	Tsu2	Time until output voltage reaches to 0 V to 90%	—	0.25	—	ms	*2 *3
Fall time	Tsd2	Time until output voltage reaches to 10%	—	5	—	ms	*2 *3
Maximum load current	IOMAX2	—	—	15	—	mA	*3
Load transient response (1)	Vtr21	I_{LDO2} = – 50 µA → – 15 mA (1 µs)	—	70	—	mV	*3
Load transient response (2)	Vtr22	I_{LDO2} = – 15 mA → – 50 µA (1 µs)	—	70	—	mV	*3
TSD (Thermal shutdown circuit)							
Detection temperature	Tdet	Temperature which LDO1, LDO2, Constant current circuit, Matrix SW and RGB turns off.	—	160	—	°C	*3 *4
Return temperature	Tsd11	Returning temperature	—	110	—	°C	*3 *5

Note) *2 : Rise time and Fall time are defined as below.

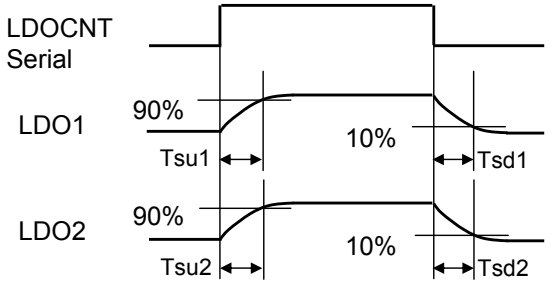
Actual evaluation result of rise time : LDO1 : 290 to 400 µs, LDO2 : 220 to 310 µs

Actual evaluation result of fall time : LDO1 : 6.2 to 8.5 ms, LDO2 : 5.8 to 7.9 ms

*3 : Typical Design Value

*4 : LDO1, LDO2, Constant current circuit, and Matrix SW and RGB are turned off when TSD is High. When TSD is High, the register is set as 14hD1 = 1. However, data can be read only when the register is read immediately after INT occurs since internal regulator is turned off.

*5 : Only LDO1 and LDO2 return after ON state of TSD. A logic part will be in Reset state.



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ELECTRICAL CHARACTERISTICS (continued)

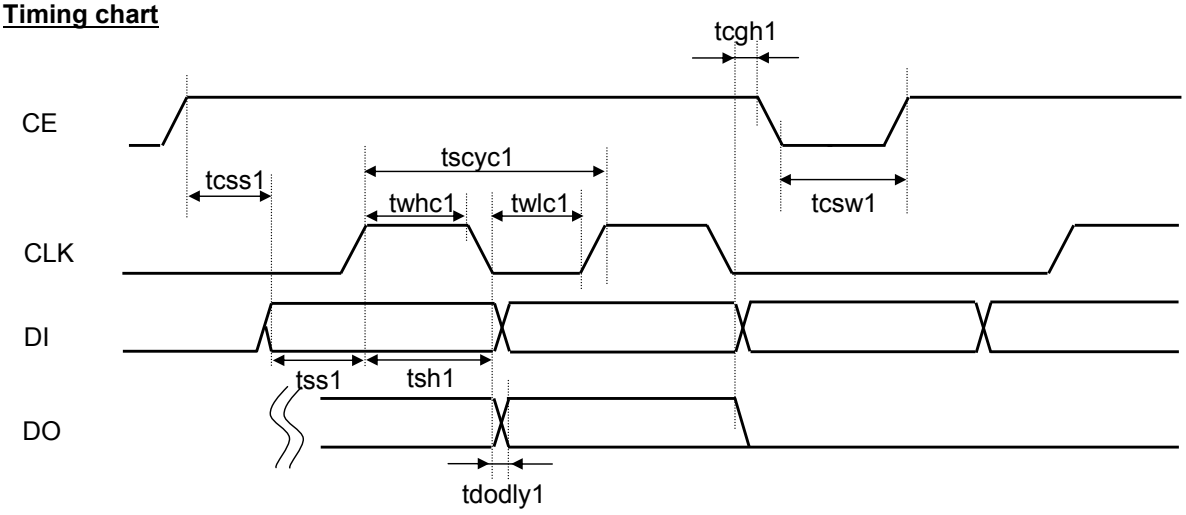
VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Microcomputer interface characteristic (Vdd = 1.85 V ± 3 %) Write access Timing							
CLK cycle time	tscyc1	—	—	125	—	ns	*3
CLK cycle time High period	twhc1	—	—	60	—	ns	*3
CLK cycle time Low period	twlc1	—	—	60	—	ns	*3
Serial-data setup time	tss1	—	—	62	—	ns	*3
Serial-data hold time	tsh1	—	—	62	—	ns	*3
Transceiver interval	tcsw1	—	—	62	—	ns	*3
Chip enable setup time	tcss1	—	—	5	—	ns	*3
Chip enable hold time	tcgh1	—	—	5	—	ns	*3
Microcomputer interface characteristic (Vdd = 1.85 V ± 3 %) Read access Timing							
CLK cycle time	tscyc1	—	—	125	—	ns	*3
CLK cycle time High period	twhc1	—	—	60	—	ns	*3
CLK cycle time Low period	twlc1	—	—	60	—	ns	*3
Serial-data setup time	tss1	—	—	62	—	ns	*3
Serial-data hold time	tsh1	—	—	62	—	ns	*3
Transceiver interval	tcsw1	—	—	62	—	ns	*3
Chip enable setup time	tcss1	—	—	5	—	ns	*3
Chip enable hold time	tcgh1	—	—	5	—	ns	*3
DC delay time	tdodly1	Only read mode	—	25	—	ns	*3

Note) *3 : Typical Design Value

Timing chart



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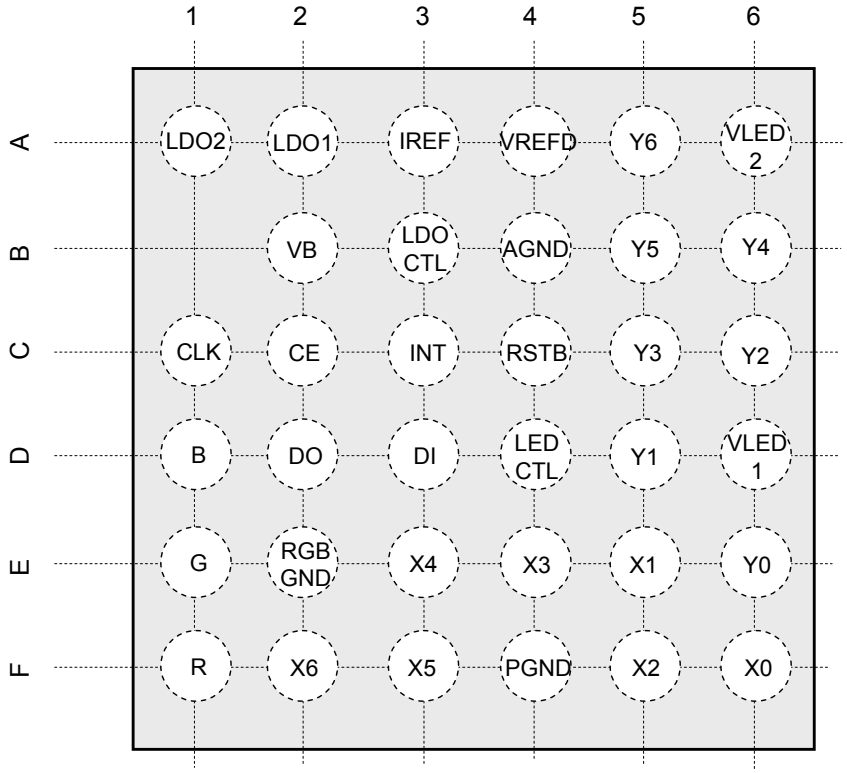
PIN CONFIGURATION

Top View



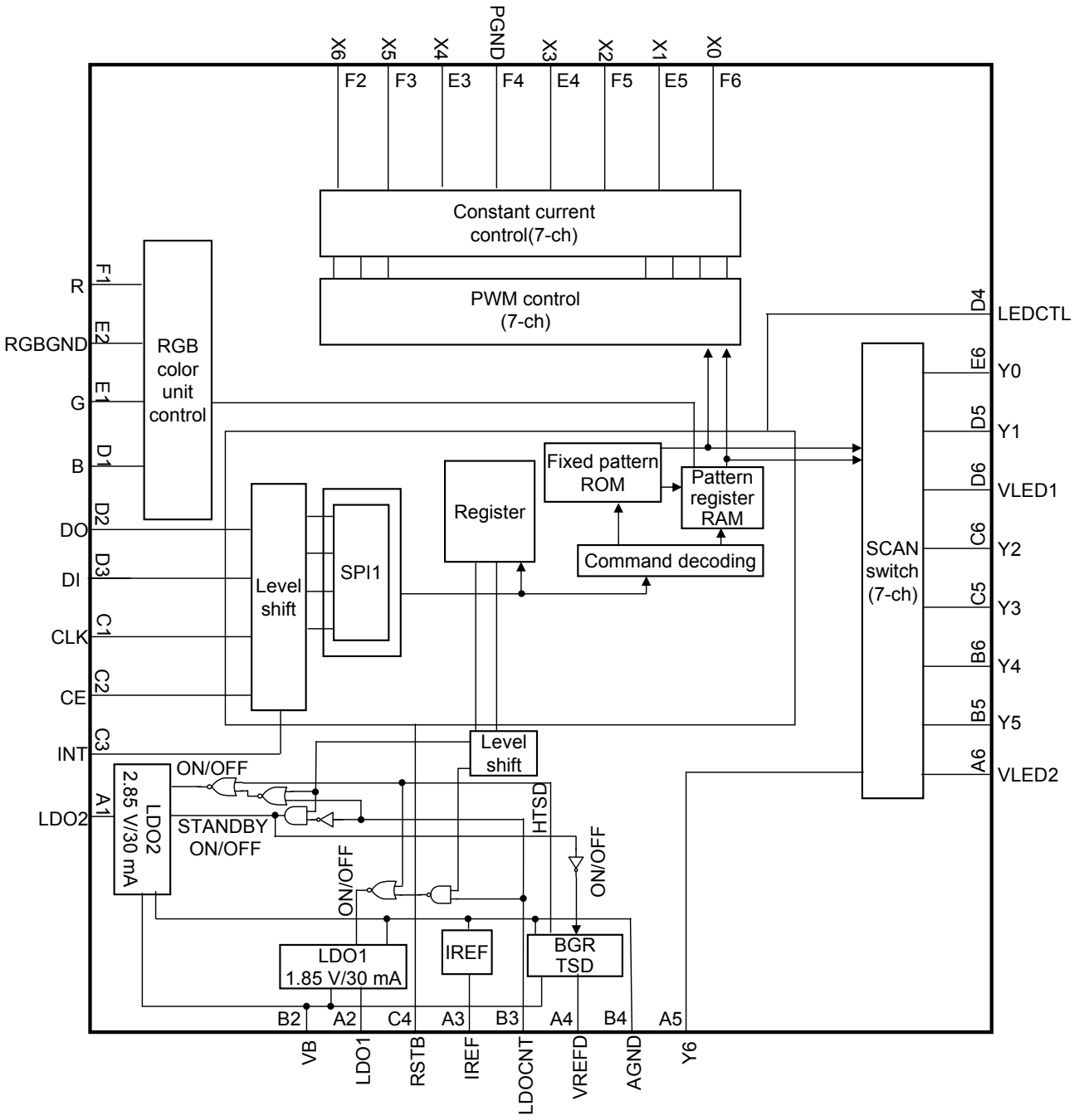
PIN FUNCTIONS

Pin No.	Pin name	Type	Description
B2	VB	Power supply	Power supply for Bandgap circuit and LDO circuit
A2	LDO1	Output	LDO1 (1.85 V) output pin
C4	RSTB	Input	Reset input (Active : High)
A3	IREF	Output	Resistor connection pin for constant current setup
B3	LDOCNT	Input	ON/OFF control pin for LDO1 and LDO2
A4	VREFD	Output	Bandgap circuit output
B4	AGND	Ground	GND for analog block
A5	Y6	Output	Constant current circuit, output pin of PWM control It connects with the G column of matrix LED.
B5	Y5	Output	Constant current circuit, output pin of PWM control It connects with the F column of matrix LED.
B6	Y4	Output	Constant current circuit, output pin of PWM control It connects with the E column of matrix LED.
C5	Y3	Output	Constant current circuit, output pin of PWM control It connects with the D column of matrix LED.
C6	Y2	Output	Constant current circuit, output pin of PWM control It connects with the C column of matrix LED.

PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
D6 A6	VLED1 VLED2	Power supply	Power supply connection pin for matrix LED
D5	Y1	Output	Constant current circuit, output pin of PWM control It connects with the B column of matrix LED.
E6	Y0	Output	Constant current circuit, output pin of PWM control It connects with the A column of matrix LED.
D4	LEDCTL	Input	ON/OFF operation control of LED lighting (by serial address 0Ah)
F6	X0	Output	Constant current circuit, output pin of PWM control It connects with the 1st row of matrix LED.
E5	X1	Output	Constant current circuit, output pin of PWM control It connects with the 2nd row of matrix LED.
F5	X2	Output	Constant current circuit, output pin of PWM control It connects with the 3rd row of matrix LED.
E4	X3	Output	Constant current circuit, output pin of PWM control It connects with the 4th row of matrix LED.
F4	PGND	Ground	GND for matrix LED
E3	X4	Output	Constant current circuit, output pin of PWM control It connects with the 5th row of matrix LED.
F3	X5	Output	Constant current circuit, output pin of PWM control It connects with the 6th row of matrix LED.
F2	X6	Output	Constant current circuit, output pin of PWM control It connects with the 7th row of matrix LED.
F1	R	Output	LED connection pin
E2	RGBGND	Ground	GND for RGB pin
E1	G	Output	LED connection pin
D1	B	Output	LED connection pin
D2	DO	Output	SPI interface data output
D3	DI	Input	SPI interface data input
C1	CLK	Input	SPI interface clock input
C2	CE	Input	SPI interface chip enable (Active : High)
C3	INT	Output	Interrupt output
A1	LDO2	Output	LDO2 (2.85 V) output

FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Explanation of each mode (Power supply startup sequence)

Mode	LDOCNT	REG18	REG28	Note
OFF mode	Low	0	0	- LDOCNT should be set to High in order to recover from OFF mode.
OFF mode → Normal mode	Low → High	0/1	0/1	- Serial signal is not received at LDOCNT = Low and REG28 = [0] or REG18 = [0]. - This LSI shifts to Standby mode at LDOCNT = Low, REG28 = [1] and REG18 = [0]. - Serial signal is not received at Standby mode. (Power supplies for logic are LDO1 and LDO2.) Therefore, Standby mode cannot be released by serial signal. - When LDOCNT is changed from Low to High, it is impossible to shift Standby mode to Normal mode. - It is impossible to shift Standby mode to OFF mode. Once returning to Normal mode, shift to OFF mode.
	High	0/1	0/1	
Normal mode → OFF mode	High → Low	0	0	- At LDOCNT = High, LDO1 turns on regardless of REG18. - At LDOCNT = High, LDO2 turns on regardless of REG28. - At RSTB = Low, serial signal is not received. - It is possible to receive the serial signal at 5 ms or more after LDOCNT is set to High. - The Low interval of RSTB should be one internal clock or more. - Don't input a signal except rectangle wave to RSTB pin. - All register's settings become default values if RSTB is set to Low. (The default value of REG18 and REG28 bit is [1]. Note that LDO1 and LDO2 don't turn off when RSTB is set to Low before LDOCNT is set to Low.) - All register's settings are reset when LDO2 turns off. (Register setting initialization) - The setup step to OFF mode is as follows. REG18, 28 = [0] → LDOCNT = Low → RSTB = Low
Normal mode → Standby mode		0	1	

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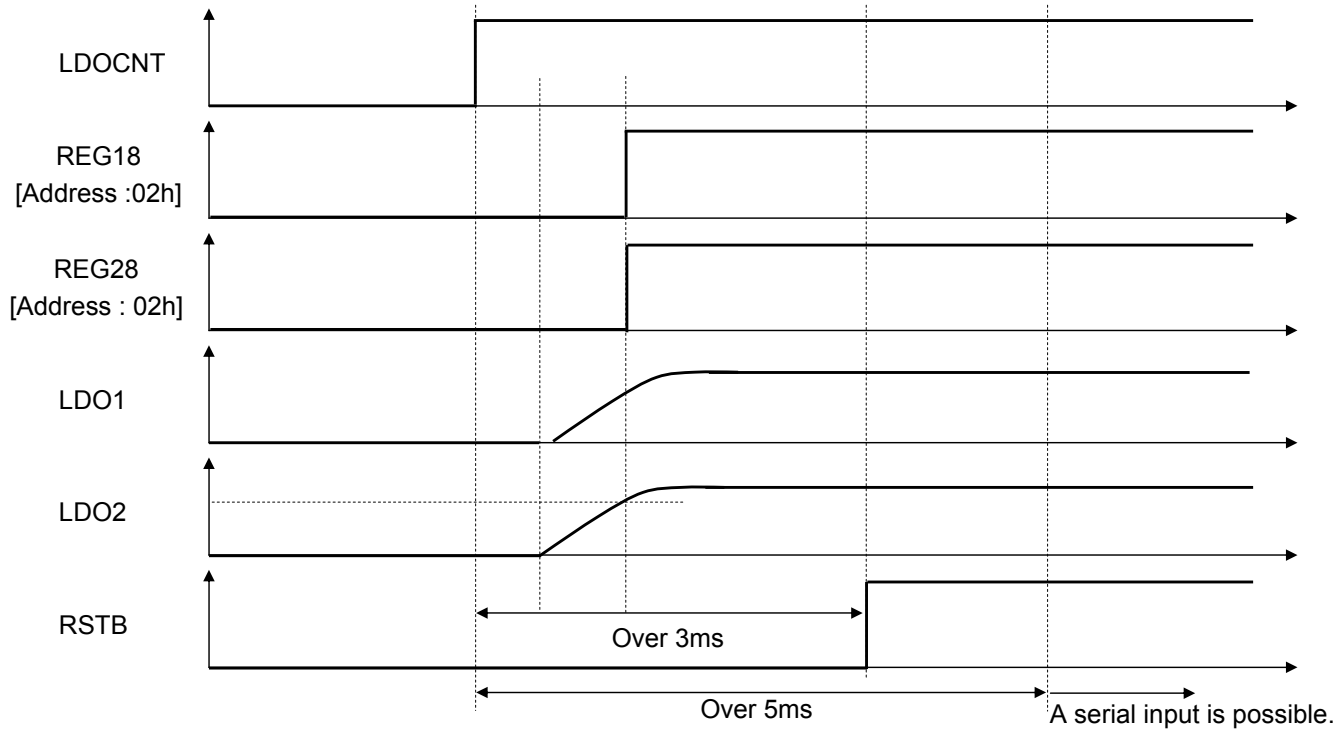
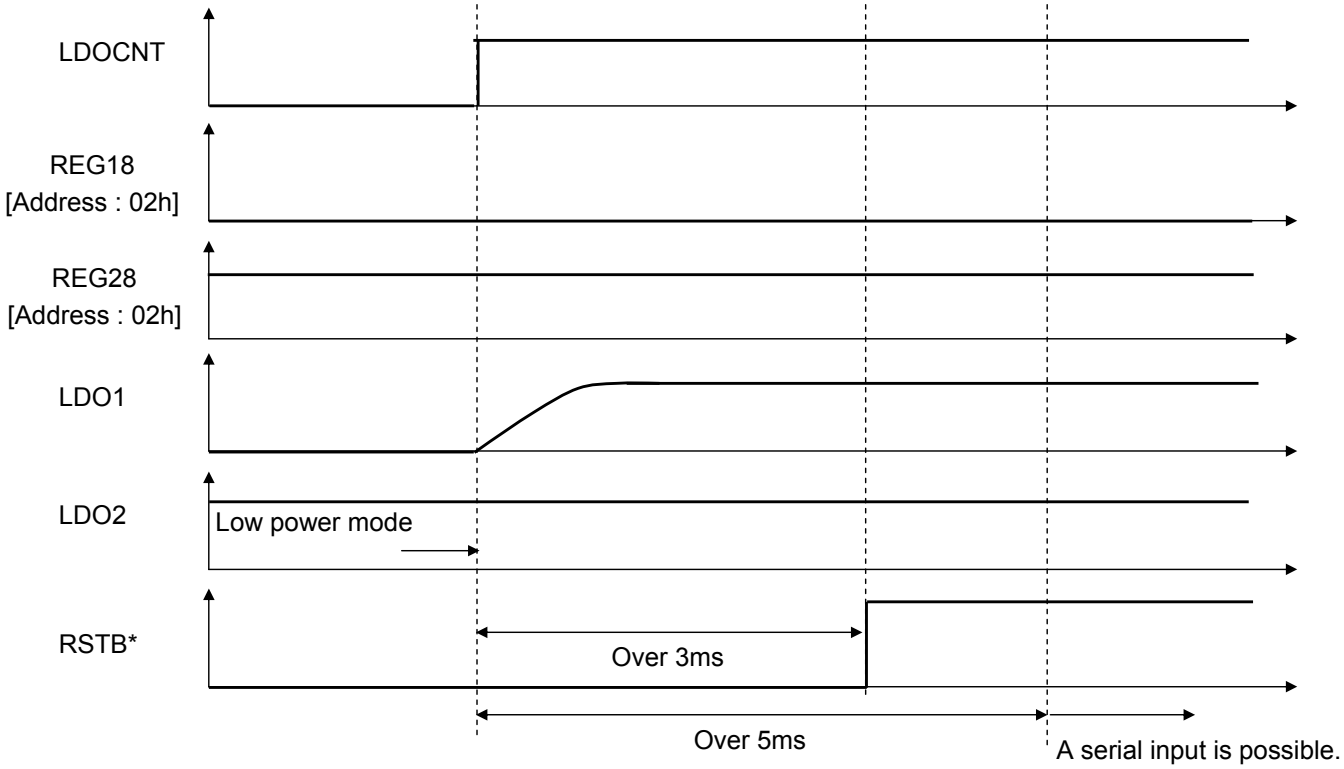
OPERATION (continued)

1. Explanation of each mode (Power supply startup sequence) (continued)

- Shift to Normal mode from OFF mode



- Shift to Normal mode from Standby mode



Note) The above waveform is under the condition that the register setup is reset in standby mode.
Maintain the state of RSTB = High to hold the register setup.

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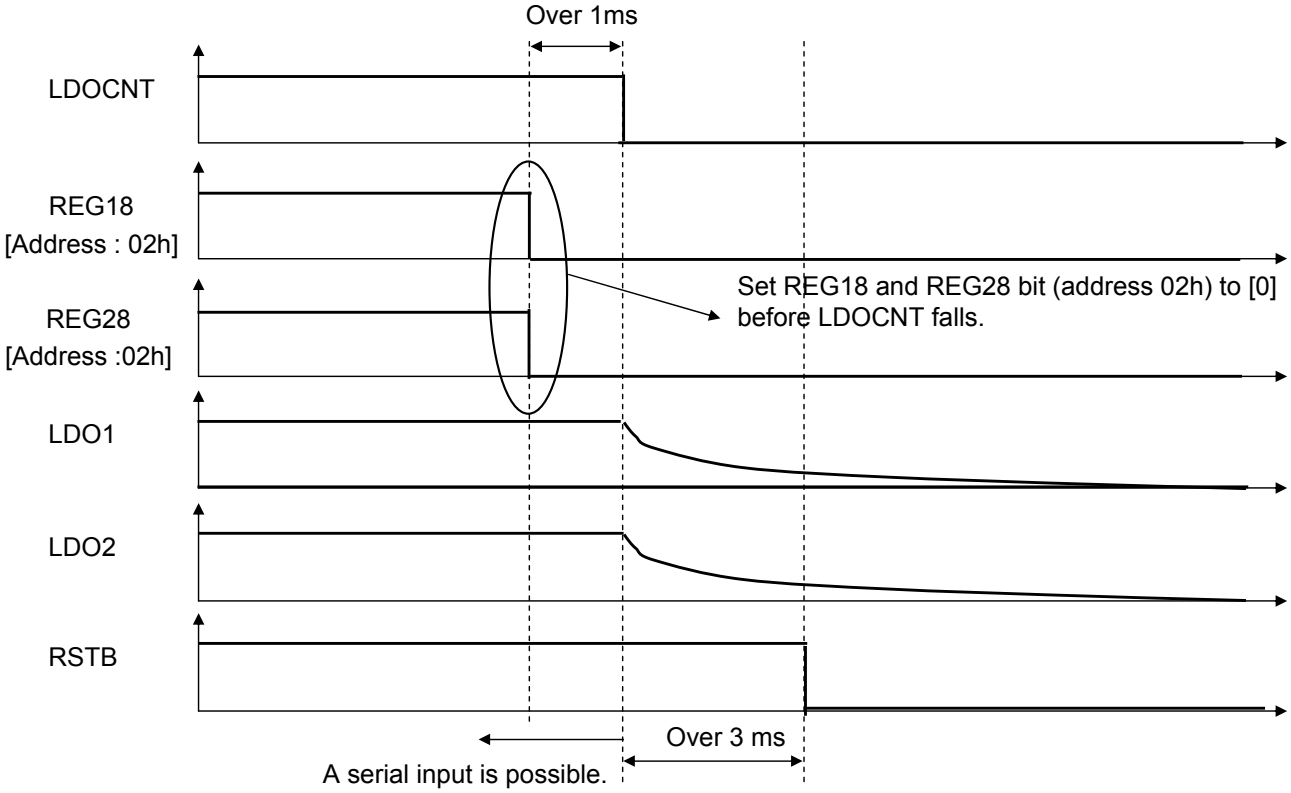
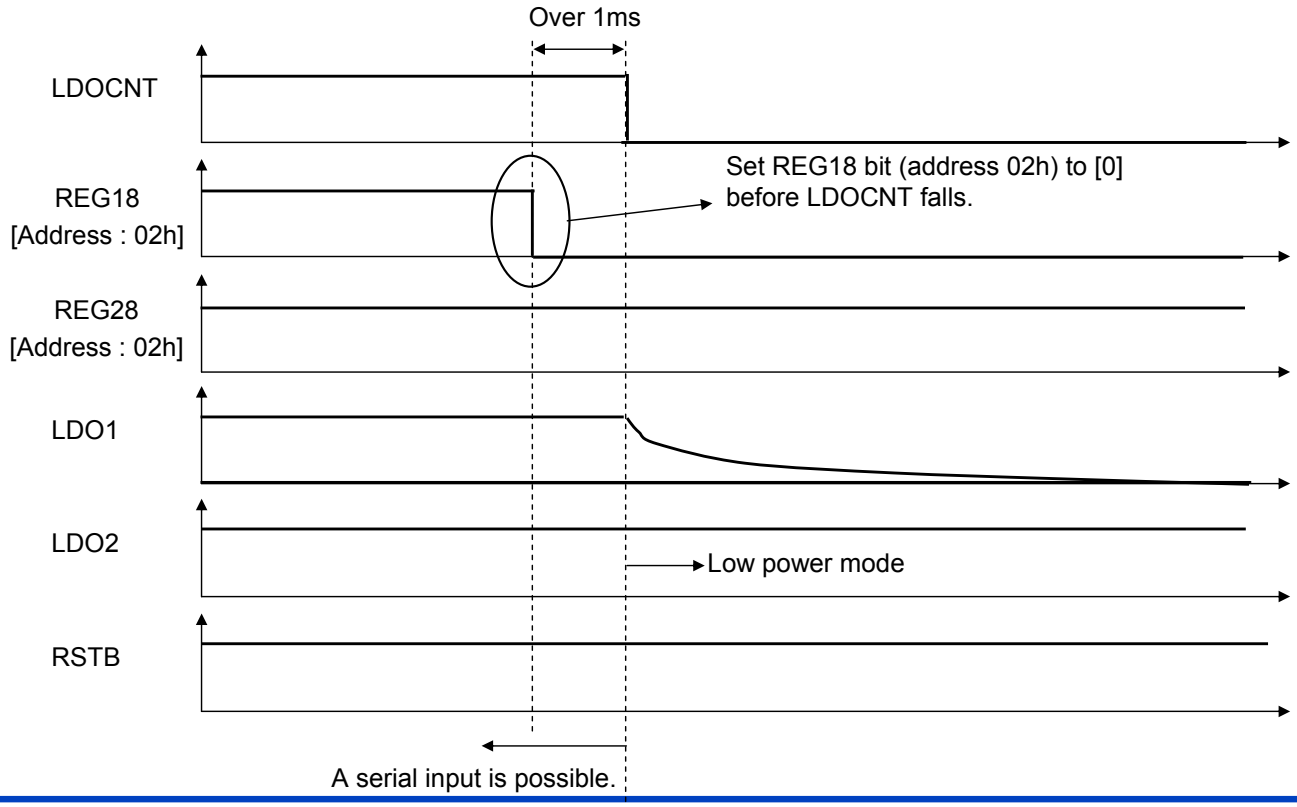
OPERATION (continued)

1. Explanation of each mode (Power supply startup sequence) (continued)

- Shift to OFF mode from Normal mode



- Shift to Standby mode from Normal mode



Established : 2009-11-18
Revised : 2013-04-18

OPERATION (continued)

1. Explanation of each mode (Power supply startup sequence) (continued)

Mode which is specified by VBAT / LDOCNT

VBAT	LDOCNT	MODE
Low	Low	OFF
Low	High	Prohibition
High	Low	OFF
High	High	ON

Note) "Low" in column of VBAT and LDOCNT means 0 V.
"High" in column of VBAT and LDOCNT means 3.1 V to 4.6 V (operation supply voltage range).

Logic pin conditions

The following setting is common for OFF, Standby and Normal mode.
The pin setting when RSTB = Low, under Normal mode is as follows.

Pin name	Pin state	Logic state*
INT	Output	Low
CE	Input	Low
CLK	Input	Low
DI	Input	Low
DO	Output	Low
LEDCTL	Input	Low
LDOCNT	Input	Depends on each mode setup

Note)*: Logic state for pins indicated as “Output” under Pin state shows the output level.
Logic state for pins indicated as “Input” under Pin state shows the input level to be set to the pins.

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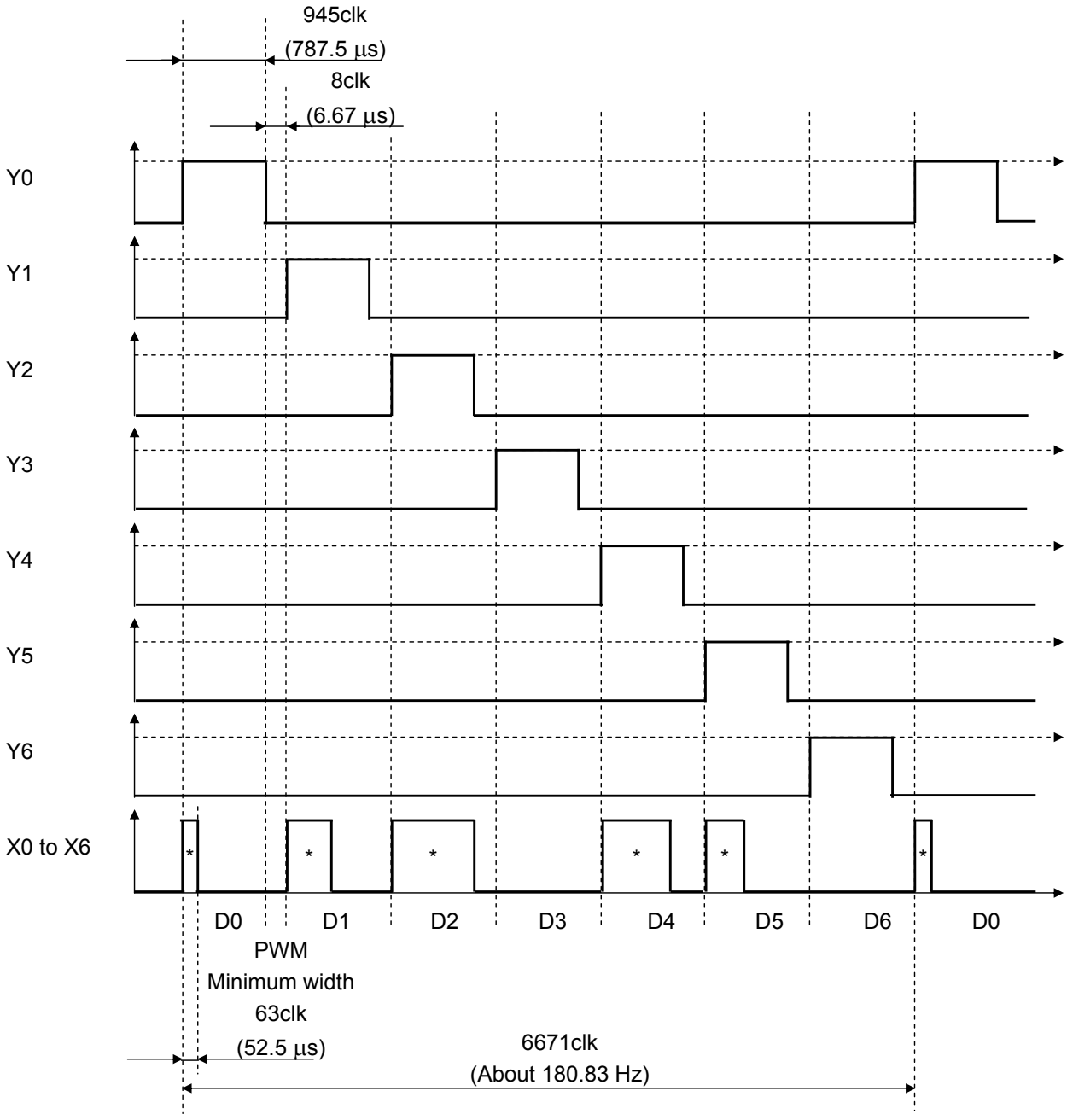
OPERATION (continued)

2. Explanation of operation

Matrix part operation waveform

The following waveform is a timing chart example at operation.
It is controlled by internal 1.2 MHz clock under the default condition.
Y side switches from Y0 to Y6 in that order. The ON period of each pin is constant 945clk (787.5 μs).
The ON period includes an 8clk(6.67 μs) interval.
In the case of the following figure, "*" mark shows ON period. Therefore, D3 and D4 are OFF period.
7 × 7 matrix display is controlled by the lines of X1 to X6.
The following waveforms are internal signals. The actual waveform of Yx pin becomes Hi-Z at Yx = Xx = Low.



Established : 2009-11-18
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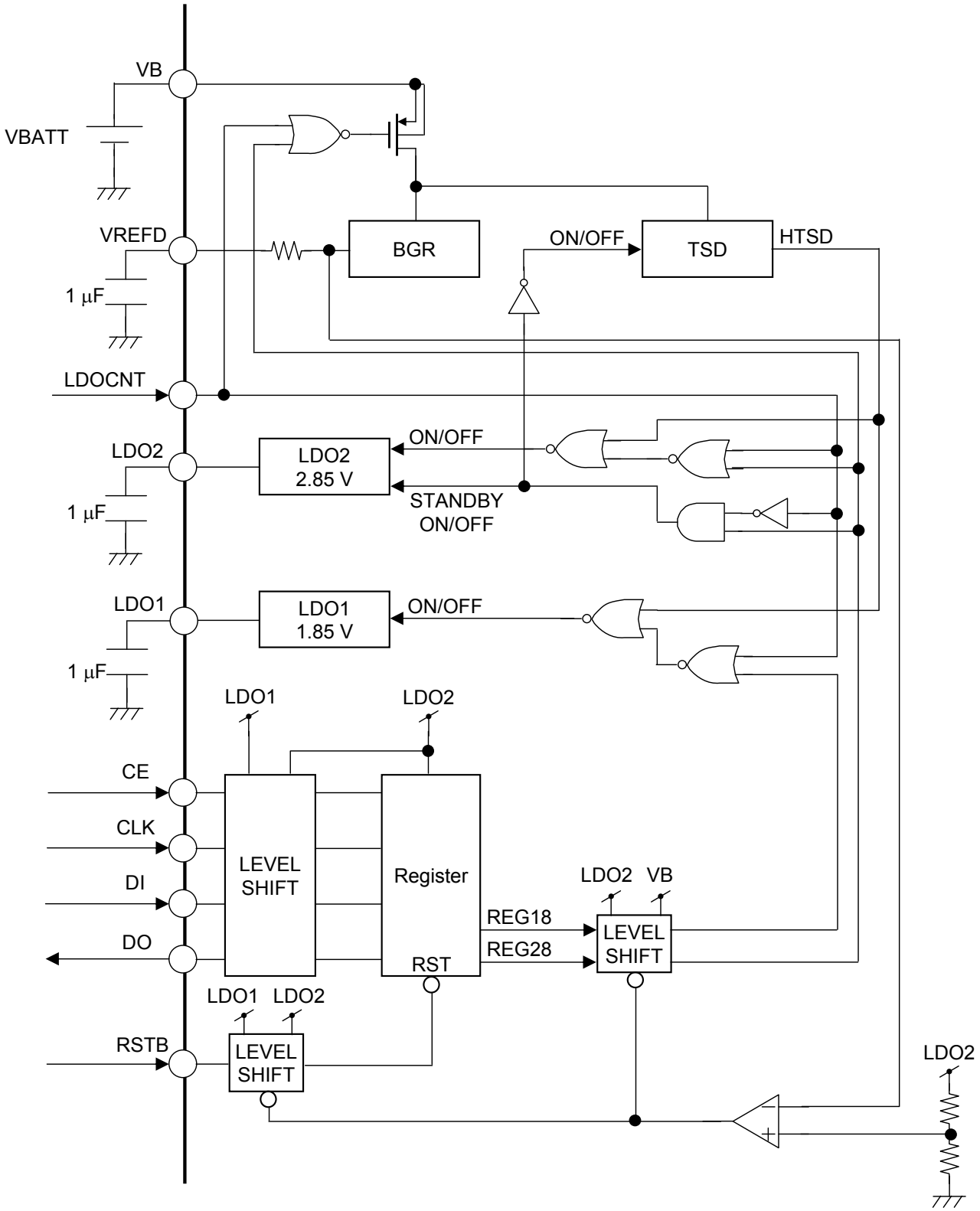
OPERATION (continued)

3. Block configuration

RESET part block configuration



Note) All the logic portions and blocks to which the power supply is not connected are supplied from VB.

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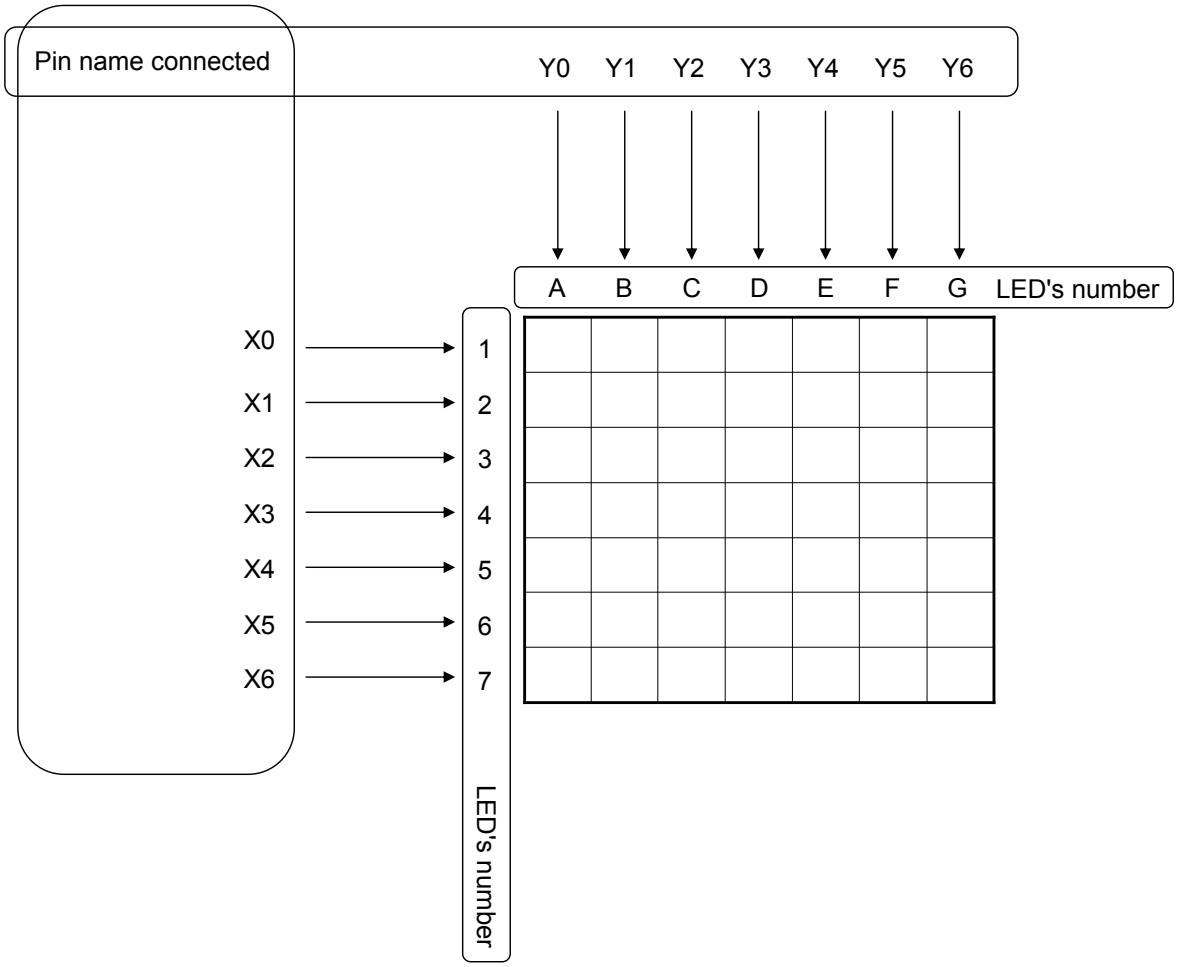
OPERATION (continued)

3. Block configuration (continued)

Explanation of matrix LED part, matrix LED's number

LED matrix driver can display characters and patterns by controlling 7 × 7 matrix LED individually.
In this product standards, LED's number controlled by each pin is as the following figure.
An internal logic circuit is controlled by internal clock.
In scroll mode, the display of character specified in the following arrangement is moved from right to left.



Established : 2009-11-18
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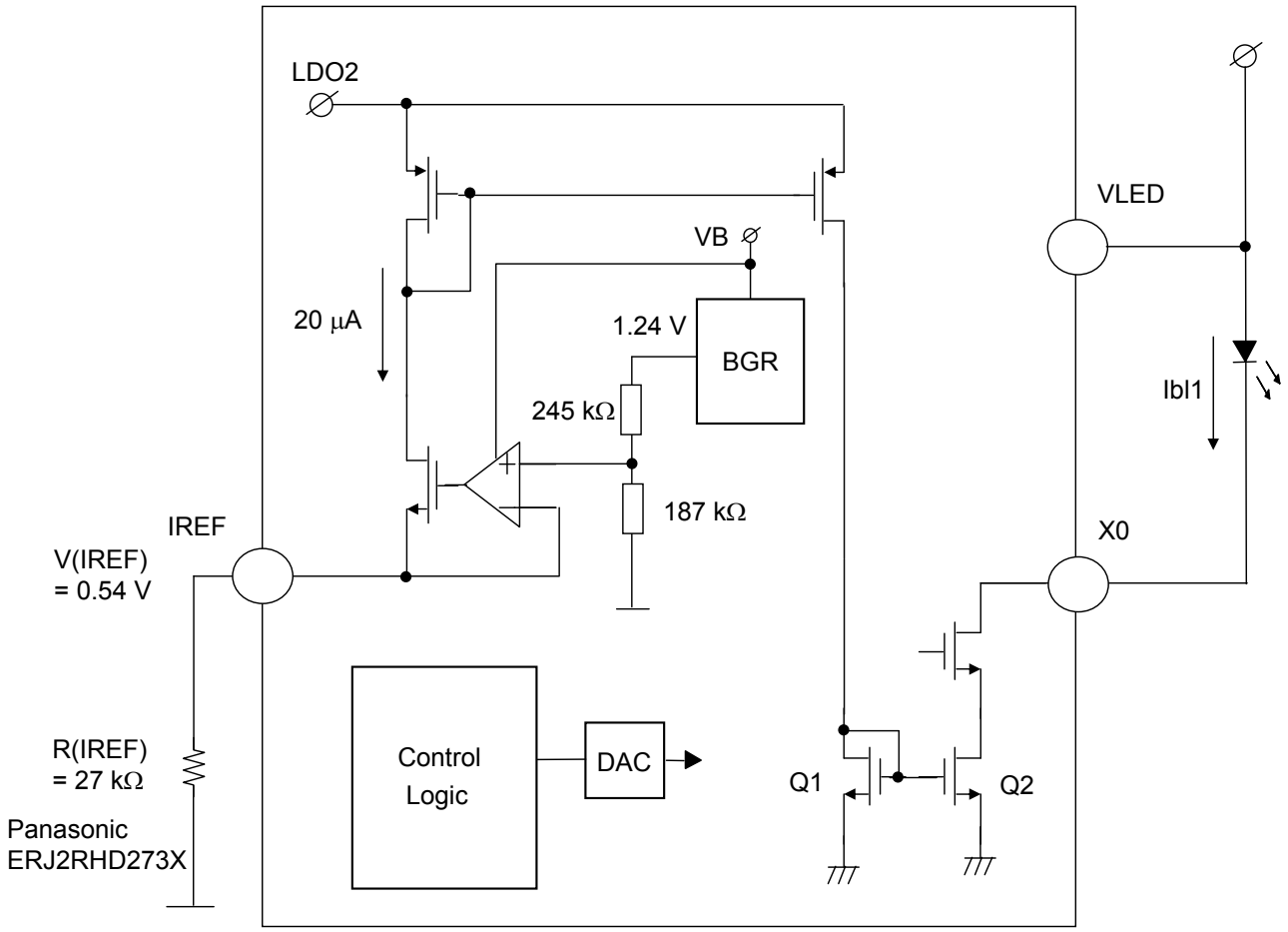
OPERATION (continued)

3. Block configuration (continued)

Equivalent circuit example of constant current driver

In case of X0 pin



The constant current equivalent circuit example (X0 pin) for LED driver is shown in the above figure.
The reference current for constant current driver is calculated by the following formula.

V(IREF) / R(IREF) = 0.54 V / 27 kΩ = 20 μA

The LED driver current can be set to the range of 0 mA to 30 mA by setting the mirror ratio between Q1 and Q2 by DAC via serial interface.
The constant current can be changed by the resistor connected to IREF pin, but the accuracy in case of this setting is not guaranteed.
It is recommended that ERJ2RHD273X is used as R(IREF) to keep the accuracy of constant current of LED driver.

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OPERATION (continued)

4. Register and Address

Register map

Sub address	R/W	Data name	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	W	POWERCNT	—	—	—	—	—	OSCEN	—	—
02h	W	LDOCNT	—	—	—	—	—	—	REG18	REG28
03h	For test									
04h	For test									
05h	For test									
06h	For test									
07h	For test									
08h	For test									
09h	For test									
0Ah	W	LEDCTL	LEDACT	—	—	—	—	DISMTX	DISRGB	—
⋮										
10h	For test									
11h	For test									
12h	For test									
13h	For test									
14h	R	IOFACTOR	FACGD1	—	—	—	RAM ACT	FRMINT	CPUWRER	TSD
15h	For test									
16h	For test									
17h	For test									
18h	For test									
19h	For test									
1Ah	W/R	VDDSEL	INTVSEL	—	—	—	—	—	—	—

Established : 2009-11-18
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OPERATION (continued)

4. Register and Address (continued)

Register map (continued)

Sub address	R/W	Data name	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
21h	R/W	MTXDATA	MTXDATA[7 : 0]							
22h	R/W	FFROM	—	—	—	—	—	—	ROM77[1 : 0]	
23h	R/W	ROMSEL	SELROM[7 : 0]							
24h	R/W	RAMCOPY	—	—	—	—	—	—	SELRAM	COPY START
25h	R/W	SETFROM	SETFROM[7 : 0]							
26h	R/W	SETTO	SETTO[7 : 0]							
27h	R/W	REPON	—	—	—	—	—	—	—	REPON
28h	R/W	SETTIME	—	—	—	—	—	—	SETTIME[1 : 0]	
29h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
2Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
2Bh	For test									
2Ch	R/W	RGBON	—	—	—	—	—	—	—	RGBON
2Dh	R/W	RGBDATA	—	—	RGBDATA[5 : 0]					
2Eh	For test									
30h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM
⋮										
6Bh	For test									
6Dh	For test									
6Fh	For test									
70h	For test									
71h	For test									
72h	For test									
73h	For test									
74h	For test									
75h	For test									
76h	For test									
77h	For test									

Note) Don't access to the address 6Bh to 77h.

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OPERATION (continued)

4. Register and Address (continued)

RAM address map

Sub address	Data name	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	A1	BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
32h	A2	BLA2[3 : 0]				FRA2[1 : 0]		DLA2[1 : 0]	
33h	A3	BLA3[3 : 0]				FRA3[1 : 0]		DLA3[1 : 0]	
34h	A4	BLA4[3 : 0]				FRA4[1 : 0]		DLA4[1 : 0]	
35h	A5	BLA5[3 : 0]				FRA5[1 : 0]		DLA5[1 : 0]	
36h	A6	BLA6[3 : 0]				FRA6[1 : 0]		DLA6[1 : 0]	
37h	A7	BLA7[3 : 0]				FRA7[1 : 0]		DLA7[1 : 0]	
38h	B1	BLB1[3 : 0]				FRB1[1 : 0]		DLB1[1 : 0]	
39h	B2	BLB2[3 : 0]				FRB2[1 : 0]		DLB2[1 : 0]	
3Ah	B3	BLB3[3 : 0]				FRB3[1 : 0]		DLB3[1 : 0]	
3Bh	B4	BLB4[3 : 0]				FRB4[1 : 0]		DLB4[1 : 0]	
3Ch	B5	BLB5[3 : 0]				FRB5[1 : 0]		DLB5[1 : 0]	
3Dh	B6	BLB6[3 : 0]				FRB6[1 : 0]		DLB6[1 : 0]	
3Eh	B7	BLB7[3 : 0]				FRB7[1 : 0]		DLB7[1 : 0]	
3Fh	C1	BLC1[3 : 0]				FRC1[1 : 0]		DLC1[1 : 0]	
40h	C2	BLC2[3 : 0]				FRC2[1 : 0]		DLC2[1 : 0]	
41h	C3	BLC3[3 : 0]				FRC3[1 : 0]		DLC3[1 : 0]	
42h	C4	BLC4[3 : 0]				FRC4[1 : 0]		DLC4[1 : 0]	
43h	C5	BLC5[3 : 0]				FRC5[1 : 0]		DLC5[1 : 0]	
44h	C6	BLC6[3 : 0]				FRC6[1 : 0]		DLC6[1 : 0]	
45h	C7	BLC7[3 : 0]				FRC7[1 : 0]		DLC7[1 : 0]	
46h	D1	BLD1[3 : 0]				FRD1[1 : 0]		DLD1[1 : 0]	
47h	D2	BLD2[3 : 0]				FRD2[1 : 0]		DLD2[1 : 0]	
48h	D3	BLD3[3 : 0]				FRD3[1 : 0]		DLD3[1 : 0]	
49h	D4	BLD4[3 : 0]				FRD4[1 : 0]		DLD4[1 : 0]	
4Ah	D5	BLD5[3 : 0]				FRD5[1 : 0]		DLD5[1 : 0]	
4Bh	D6	BLD6[3 : 0]				FRD6[1 : 0]		DLD6[1 : 0]	
4Ch	D7	BLD7[3 : 0]				FRD7[1 : 0]		DLD7[1 : 0]	

Established : 2009-11-18
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OPERATION (continued)

4. Register and Address (continued)

RAM address map (continued)

Sub address	Data name	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
4Dh	E1	BLE1[3 : 0]				FRE1[1 : 0]		DLE1[1 : 0]	
4Eh	E2	BLE2[3 : 0]				FRE2[1 : 0]		DLE2[1 : 0]	
4Fh	E3	BLE3[3 : 0]				FRE3[1 : 0]		DLE3[1 : 0]	
50h	E4	BLE4[3 : 0]				FRE4[1 : 0]		DLE4[1 : 0]	
51h	E5	BLE5[3 : 0]				FRE5[1 : 0]		DLE5[1 : 0]	
52h	E6	BLE6[3 : 0]				FRE6[1 : 0]		DLE6[1 : 0]	
53h	E7	BLE7[3 : 0]				FRE7[1 : 0]		DLE7[1 : 0]	
54h	F1	BLF1[3 : 0]				FRF1[1 : 0]		DLF1[1 : 0]	
55h	F2	BLF2[3 : 0]				FRF2[1 : 0]		DLF2[1 : 0]	
56h	F3	BLF3[3 : 0]				FRF3[1 : 0]		DLF3[1 : 0]	
57h	F4	BLF4[3 : 0]				FRF4[1 : 0]		DLF4[1 : 0]	
58h	F5	BLF5[3 : 0]				FRF5[1 : 0]		DLF5[1 : 0]	
59h	F6	BLF6[3 : 0]				FRF6[1 : 0]		DLF6[1 : 0]	
5Ah	F7	BLF7[3 : 0]				FRF7[1 : 0]		DLF7[1 : 0]	
5Bh	G1	BLG1[3 : 0]				FRG1[1 : 0]		DLG1[1 : 0]	
5Ch	G2	BLG2[3 : 0]				FRG2[1 : 0]		DLG2[1 : 0]	
5Dh	G3	BLG3[3 : 0]				FRG3[1 : 0]		DLG3[1 : 0]	
5Eh	G4	BLG4[3 : 0]				FRG4[1 : 0]		DLG4[1 : 0]	
5Fh	G5	BLG5[3 : 0]				FRG5[1 : 0]		DLG5[1 : 0]	
60h	G6	BLG6[3 : 0]				FRG6[1 : 0]		DLG6[1 : 0]	
61h	G7	BLG7[3 : 0]				FRG7[1 : 0]		DLG7[1 : 0]	
62h	LEDR	BLLEDR[3 : 0]				FRLEDR[1 : 0]		DLLEDR[1 : 0]	
63h	LEDG	BLLEDG[3 : 0]				FRLEDG[1 : 0]		DLLEDG[1 : 0]	
64h	LEDB	BLLEDB[3 : 0]				FRLEDB[1 : 0]		DLLEDB[1 : 0]	

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OPERATION (continued)

4. Register and Address (continued)

ROM address map

[00000000] – [10010101] : ROM (Luminance only) 7 × 7 pattern No.0 (default) to pattern No.149

Pattern No.	Contents of pattern	Display	Pattern No.	Contents of pattern	Display
0	All lights out	Nothing	31	Alphabetic character	U
1	Number	0	32	Alphabetic character	V
2	Number	1	33	Alphabetic character	W
3	Number	2	34	Alphabetic character	X
4	Number	3	35	Alphabetic character	Y
5	Number	4	36	Alphabetic character	Z
6	Number	5	37	Alphabetic character	a
7	Number	6	38	Alphabetic character	b
8	Number	7	39	Alphabetic character	c
9	Number	8	40	Alphabetic character	d
10	Number	9	41	Alphabetic character	e
11	Alphabetic character	A	42	Alphabetic character	f
12	Alphabetic character	B	43	Alphabetic character	g
13	Alphabetic character	C	44	Alphabetic character	h
14	Alphabetic character	D	45	Alphabetic character	i
15	Alphabetic character	E	46	Alphabetic character	j
16	Alphabetic character	F	47	Alphabetic character	k
17	Alphabetic character	G	48	Alphabetic character	l
18	Alphabetic character	H	49	Alphabetic character	m
19	Alphabetic character	I	50	Alphabetic character	n
20	Alphabetic character	J	51	Alphabetic character	o
21	Alphabetic character	K	52	Alphabetic character	p
22	Alphabetic character	L	53	Alphabetic character	q
23	Alphabetic character	M	54	Alphabetic character	r
24	Alphabetic character	N	55	Alphabetic character	s
25	Alphabetic character	O	56	Alphabetic character	t
26	Alphabetic character	P	57	Alphabetic character	u
27	Alphabetic character	Q	58	Alphabetic character	v
28	Alphabetic character	R	59	Alphabetic character	w
29	Alphabetic character	S	60	Alphabetic character	x
30	Alphabetic character	T	61	Alphabetic character	y

Established : 2009-11-18
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OPERATION (continued)

4. Register and Address (continued)

ROM address map (continued)

[00000000] – [10010101] : ROM (Luminance only) 7 × 7 pattern No.0 (default) to pattern No.149

Pattern No.	Contents of pattern	Display	Pattern No.	Contents of pattern	Display
62	Alphabetic character	z	93	Number	30
63	Number	00	94	Number	31
64	Number	01	95	Number	32
65	Number	02	96	Number	33
66	Number	03	97	Number	34
67	Number	04	98	Number	35
68	Number	05	99	Number	36
69	Number	06	100	Number	37
70	Number	07	101	Number	38
71	Number	08	102	Number	39
72	Number	09	103	Number	40
73	Number	10	104	Number	41
74	Number	11	105	Number	42
75	Number	12	106	Number	43
76	Number	13	107	Number	44
77	Number	14	108	Number	45
78	Number	15	109	Number	46
79	Number	16	110	Number	47
80	Number	17	111	Number	48
81	Number	18	112	Number	49
82	Number	19	113	Number	50
83	Number	20	114	Number	51
84	Number	21	115	Number	52
85	Number	22	116	Number	53
86	Number	23	117	Number	54
87	Number	24	118	Number	55
88	Number	25	119	Number	56
89	Number	26	120	Number	57
90	Number	27	121	Number	58
91	Number	28	122	Number	59
92	Number	29	123	Number	60

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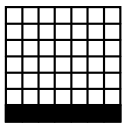
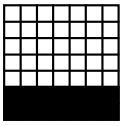
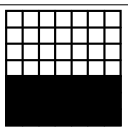
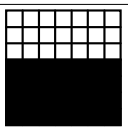
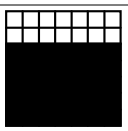
OPERATION (continued)

4. Register and Address (continued)

ROM address map (continued)

[00000000] – [10010101] : ROM (Luminance only) 7 × 7 pattern No.0 (default) to pattern No.149

Pattern No.	Contents of pattern	Display
124	Symbol	Zero antenna
125	Symbol	One antenna
126	Symbol	Two antenna
127	Symbol	Three antenna
128	Symbol	▶
129	Symbol	■
130	Symbol	||
131	Symbol	>>
132	Symbol	<<
133	Symbol	:
134	Symbol	!
135	Symbol	?
136	Symbol	▲
137	Symbol	▼
138	Symbol	←
139	Symbol	→
140	Symbol	+
141	Symbol	–
142	Symbol	/
143	Symbol	

Pattern No.	Contents of pattern	Display
144	Symbol	
145	Symbol	
146	Symbol	
147	Symbol	
148	Symbol	
149	Symbol	

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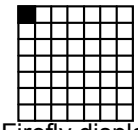
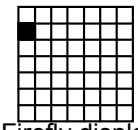
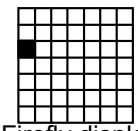
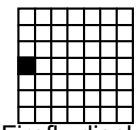
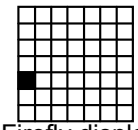
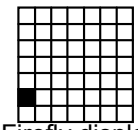
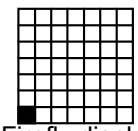
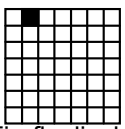
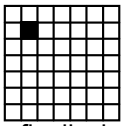
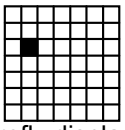
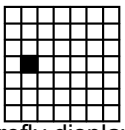
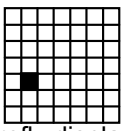
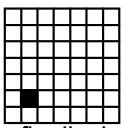
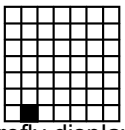
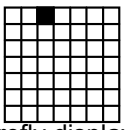
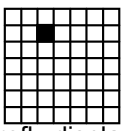
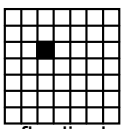
OPERATION (continued)

4. Register and Address (continued)

ROM address map (continued)

[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to pattern No.208

Pattern No.	Contents of pattern	Display
150	Symbol	 Firefly display
151	Symbol	 Firefly display
152	Symbol	 Firefly display
153	Symbol	 Firefly display
154	Symbol	 Firefly display
155	Symbol	 Firefly display
156	Symbol	 Firefly display
157	Symbol	 Firefly display
158	Symbol	 Firefly display

Pattern No.	Contents of pattern	Display
159	Symbol	 Firefly display
160	Symbol	 Firefly display
161	Symbol	 Firefly display
162	Symbol	 Firefly display
163	Symbol	 Firefly display
164	Symbol	 Firefly display
165	Symbol	 Firefly display
166	Symbol	 Firefly display
167	Symbol	 Firefly display

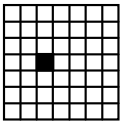
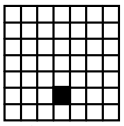
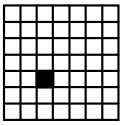
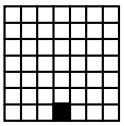
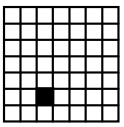
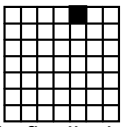
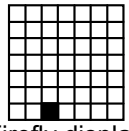
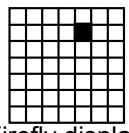
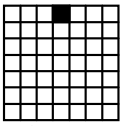
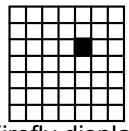
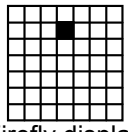
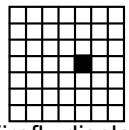
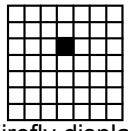
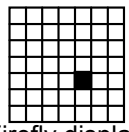
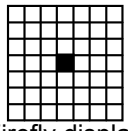
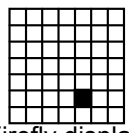
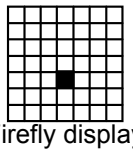
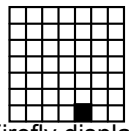
Established : 2009-11-18
Revised : 2013-04-18

OPERATION (continued)

4. Register and Address (continued)

ROM address map (continued)

[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to pattern No.208

Pattern No.	Contents of pattern	Display	Pattern No.	Contents of pattern	Display
168	Symbol	 Firefly display	177	Symbol	 Firefly display
169	Symbol	 Firefly display	178	Symbol	 Firefly display
170	Symbol	 Firefly display	179	Symbol	 Firefly display
171	Symbol	 Firefly display	180	Symbol	 Firefly display
172	Symbol	 Firefly display	181	Symbol	 Firefly display
173	Symbol	 Firefly display	182	Symbol	 Firefly display
174	Symbol	 Firefly display	183	Symbol	 Firefly display
175	Symbol	 Firefly display	184	Symbol	 Firefly display
176	Symbol	 Firefly display	185	Symbol	 Firefly display

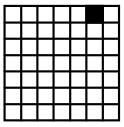
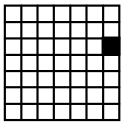
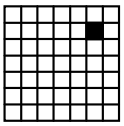
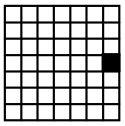
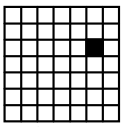
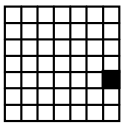
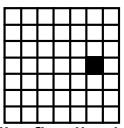
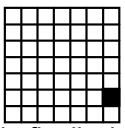
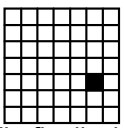
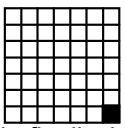
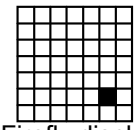
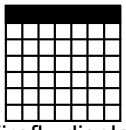
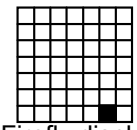
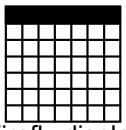
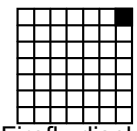
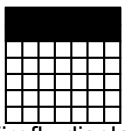
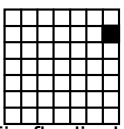
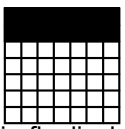
Established : 2009-11-18
Revised : 2013-04-18

OPERATION (continued)

4. Register and Address (continued)

ROM address map (continued)

[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to pattern No.208

Pattern No.	Contents of pattern	Display	Pattern No.	Contents of pattern	Display
186	Symbol	 Firefly display	195	Symbol	 Firefly display
187	Symbol	 Firefly display	196	Symbol	 Firefly display
188	Symbol	 Firefly display	197	Symbol	 Firefly display
189	Symbol	 Firefly display	198	Symbol	 Firefly display
190	Symbol	 Firefly display	199	Symbol	 Firefly display
191	Symbol	 Firefly display	200	Symbol	 Firefly display
192	Symbol	 Firefly display	201	Symbol	 Firefly display
193	Symbol	 Firefly display	202	Symbol	 Firefly display
194	Symbol	 Firefly display	203	Symbol	 Firefly display

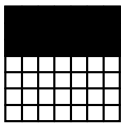
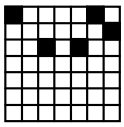
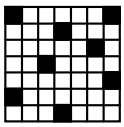
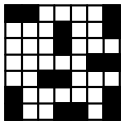
Established : 2009-11-18
Revised : 2013-04-18

OPERATION (continued)

4. Register and Address (continued)

ROM address map (continued)

[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to pattern No.208

Pattern No.	Contents of pattern	Display
204	Symbol	 Firefly display
205	Symbol	 Firefly display
206	Symbol	 Firefly display
207	Symbol	 Firefly display
208	Symbol	 Firefly display

Established : 2009-11-18
Revised : 2013-04-18

OPERATION (continued)

4. Register and Address (continued)

Register list which needs a clock

The following addresses can be read / written even if there is not an internal clock or an external clock.
However, it is impossible to achieve the operation finally needed.

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	W	POWERCNT	—	—	—	—	—	OSCEN	—	—
14h	R	IOFACTOR	FACG D1	—	—	—	RAM ACT	FRMINT	CPU WRER	TSD
20h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
21h	R/W	MTXDATA	MTXDATA[7:0]							
22h	R/W	FFROM	—	—	—	—	—	—	ROM77[1:0]	
23h	R/W	ROMSEL	SELROM[7:0]							
24h	R/W	RAMCOPY	—	—	—	—	—	—	SELRAM	COPY START
25h	R/W	SETFROM	SETFROM[7:0]							
26h	R/W	SETTO	SETTO[7:0]							
27h	R/W	REPON	—	—	—	—	—	—	—	REPON
28h	R/W	SETTIME	—	—	—	—	—	—	SETTIME[1:0]	
29h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
2Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
2Bh	R/W	SCLTIME	—	—	—	—	—	—	SCLTIME[1:0]	
2Ch	R/W	RGBON	—	—	—	—	—	—	—	RGBON
2Dh	R/W	RGBDATA	—	—	RGBDATA[5:0]					
30h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM

Established : 2009-11-18
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OPERATION (continued)

4. Register and Address (continued)

Register list which needs a clock (continued)

The following addresses can not be read / written if there is not an internal clock or an external clock.

Sub address	Data name	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	A1	BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
32h	A2	BLA2[3 : 0]				FRA2[1 : 0]		DLA2[1 : 0]	
33h	A3	BLA3[3 : 0]				FRA3[1 : 0]		DLA3[1 : 0]	
34h	A4	BLA4[3 : 0]				FRA4[1 : 0]		DLA4[1 : 0]	
35h	A5	BLA5[3 : 0]				FRA5[1 : 0]		DLA5[1 : 0]	
36h	A6	BLA6[3 : 0]				FRA6[1 : 0]		DLA6[1 : 0]	
37h	A7	BLA7[3 : 0]				FRA7[1 : 0]		DLA7[1 : 0]	
38h	B1	BLB1[3 : 0]				FRB1[1 : 0]		DLB1[1 : 0]	
39h	B2	BLB2[3 : 0]				FRB2[1 : 0]		DLB2[1 : 0]	
3Ah	B3	BLB3[3 : 0]				FRB3[1 : 0]		DLB3[1 : 0]	
3Bh	B4	BLB4[3 : 0]				FRB4[1 : 0]		DLB4[1 : 0]	
3Ch	B5	BLB5[3 : 0]				FRB5[1 : 0]		DLB5[1 : 0]	
3Dh	B6	BLB6[3 : 0]				FRB6[1 : 0]		DLB6[1 : 0]	
3Eh	B7	BLB7[3 : 0]				FRB7[1 : 0]		DLB7[1 : 0]	
3Fh	C1	BLC1[3 : 0]				FRC1[1 : 0]		DLC1[1 : 0]	
40h	C2	BLC2[3 : 0]				FRC2[1 : 0]		DLC2[1 : 0]	
41h	C3	BLC3[3 : 0]				FRC3[1 : 0]		DLC3[1 : 0]	
42h	C4	BLC4[3 : 0]				FRC4[1 : 0]		DLC4[1 : 0]	
43h	C5	BLC5[3 : 0]				FRC5[1 : 0]		DLC5[1 : 0]	
44h	C6	BLC6[3 : 0]				FRC6[1 : 0]		DLC6[1 : 0]	
45h	C7	BLC7[3 : 0]				FRC7[1 : 0]		DLC7[1 : 0]	
46h	D1	BLD1[3 : 0]				FRD1[1 : 0]		DLD1[1 : 0]	
47h	D2	BLD2[3 : 0]				FRD2[1 : 0]		DLD2[1 : 0]	
48h	D3	BLD3[3 : 0]				FRD3[1 : 0]		DLD3[1 : 0]	
49h	D4	BLD4[3 : 0]				FRD4[1 : 0]		DLD4[1 : 0]	
4Ah	D5	BLD5[3 : 0]				FRD5[1 : 0]		DLD5[1 : 0]	
4Bh	D6	BLD6[3 : 0]				FRD6[1 : 0]		DLD6[1 : 0]	
4Ch	D7	BLD7[3 : 0]				FRD7[1 : 0]		DLD7[1 : 0]	

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OPERATION (continued)

4. Register and Address (continued)

Register list which needs a clock (continued)

The following addresses can not be read / written if there is not an internal clock or an external clock.

Sub address	Data name	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
4Dh	E1	BLE1[3 : 0]				FRE1[1 : 0]		DLE1[1 : 0]	
4Eh	E2	BLE2[3 : 0]				FRE2[1 : 0]		DLE2[1 : 0]	
4Fh	E3	BLE3[3 : 0]				FRE3[1 : 0]		DLE3[1 : 0]	
50h	E4	BLE4[3 : 0]				FRE4[1 : 0]		DLE4[1 : 0]	
51h	E5	BLE5[3 : 0]				FRE5[1 : 0]		DLE5[1 : 0]	
52h	E6	BLE6[3 : 0]				FRE6[1 : 0]		DLE6[1 : 0]	
53h	E7	BLE7[3 : 0]				FRE7[1 : 0]		DLE7[1 : 0]	
54h	F1	BLF1[3 : 0]				FRF1[1 : 0]		DLF1[1 : 0]	
55h	F2	BLF2[3 : 0]				FRF2[1 : 0]		DLF2[1 : 0]	
56h	F3	BLF3[3 : 0]				FRF3[1 : 0]		DLF3[1 : 0]	
57h	F4	BLF4[3 : 0]				FRF4[1 : 0]		DLF4[1 : 0]	
58h	F5	BLF5[3 : 0]				FRF5[1 : 0]		DLF5[1 : 0]	
59h	F6	BLF6[3 : 0]				FRF6[1 : 0]		DLF6[1 : 0]	
5Ah	F7	BLF7[3 : 0]				FRF7[1 : 0]		DLF7[1 : 0]	
5Bh	G1	BLG1[3 : 0]				FRG1[1 : 0]		DLG1[1 : 0]	
5Ch	G2	BLG2[3 : 0]				FRG2[1 : 0]		DLG2[1 : 0]	
5Dh	G3	BLG3[3 : 0]				FRG3[1 : 0]		DLG3[1 : 0]	
5Eh	G4	BLG4[3 : 0]				FRG4[1 : 0]		DLG4[1 : 0]	
5Fh	G5	BLG5[3 : 0]				FRG5[1 : 0]		DLG5[1 : 0]	
60h	G6	BLG6[3 : 0]				FRG6[1 : 0]		DLG6[1 : 0]	
61h	G7	BLG7[3 : 0]				FRG7[1 : 0]		DLG7[1 : 0]	
62h	LEDR	BLLEDR[3 : 0]				FRLEDR[1 : 0]		DLLEDR[1 : 0]	
63h	LEDG	BLLEDG[3 : 0]				FRLEDG[1 : 0]		DLLEDG[1 : 0]	
64h	LEDB	BLLEDB[3 : 0]				FRLEDB[1 : 0]		DLLEDB[1 : 0]	

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
01h	Data Name	—	—	—	—	—	OSCEN	—	—
	Default	0	0	0	0	0	0	0	0
	Mode	W	W	W	W	W	W	W	W

D2 : OSCEN ON/OFF bit for internal oscillator
[0] : Internal oscillator is OFF (default)
[1] : Internal oscillator is ON

- The frequency variation of an internal oscillator is 0.96 MHz to 1.44 MHz.
- The internal clock variation of an internal oscillator is 694.4 ns to 1042 ns.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
02h	Data Name	—	—	—	—	—	—	REG18	REG28
	Default	0	0	0	0	0	0	1	1
	mode	W	W	W	W	W	W	W	W

D1 : REG18 The ON/OFF control for LDO1(When LDOCNT terminal is Low)
[0] : LDO1 OFF
[1] : LDO1 ON (default)

D0 : REG28 The ON/OFF control for LDO2(When LDOCNT terminal is Low)
[0] : LDO2 OFF
[1] : LDO2 ON (default)

- When LDOCNT terminal is High, regardless of the state of REG18, LDO1 will be activated.
- When LDOCNT terminal is High, regardless of the state of REG28, LDO2 will be activated.
- Set LDOCNT to Low after setting REG28 to Low to put into OFF mode.

OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
03h	Data name	For test							
	Default	0	0	0	0	0	0	0	0
	Mode	W	W	W	W	W	W	W	W

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
04h	Data name	For test							
	Default	0	0	0	0	0	0	0	0
	Mode	R	R	R	R	R	R	R	R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
05h	Data name	For test							
	Default	0	0	0	0	0	0	0	0
	Mode	W	W	W	W	W	W	W	W

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
06h	Data name	For test							
	Default	0	0	0	0	0	0	0	0
	Mode	W	W	W	W	W	W	W	W

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
07h	Data name	For test							
	Default	0	0	0	0	0	0	0	0
	Mode	W	W	W	W	W	W	W	W

- Don't access to the address 03h to 07h because these addresses are for test.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
08h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
09h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

*Don't access to address from 08h to 09h.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
0Ah	Data Name	LEDACT	—	—	—	—	DISMTX	DISRGB	—
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D7 : LEDACT A putting-out-lights setup of LED by LEDCTL terminal.
[0] : The light is switched on at LEDCTL = Low(default)
[1] : The light is switched on at LEDCTL = High

D2 : DISMTX A putting-out-lights ON/OFF setup of 7 × 7 dots matrix LED by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D1 : DISRGB A putting-out-lights ON/OFF setup of R, G and B terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
11h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
12h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
13h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

- Don't access to the address 10h to 13h because these addresses are for test.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
14h	Data name	FACGD1	—	—	—	RAMACT	FRMINT	CPUWRER	TSD
	Default	0	0	0	0	0	0	0	0
	Mode	R	R	R	R	R	R	R	R

D7 : FACGD1
[0] : Normal operation (default)
[1] : No read clearance

D3 : RAMACT Internal RAM access judgment
[0] : RAM is not accessed. (default)
[1] : RAM is accessed.

D2 : FRMINT Frame display end judgment during scroll display
[0] : Under frame display (default)
[1] : Frame display end

D1 : CPUWRER CPU access error judgment
[0] : CPU access error does not occur. (default)
[1] : CPU access error occurs.

D0 : TSD Abnormal detection of TSD error
[0] : TSD abnormal detection does not occur. (default)
[1] : TSD abnormal detection occurs.

- When CPU writes the data to RAM1 or RAM2 (31h to 64h) during copying to RAM1 or RAM2 from ROM, CPUWRER indicates the error, and [1] is read.
- The contents written by CPU are not reflected in this LSI at CPUWRER = [1]. The write by CPU should be performed again.
- The interval of FACGD1 = [1] is maximum 1.93 μs (at internal clock operation) after data is updated.
- At FACGD1 = [0], if data of address 14h is read, data of D0 to D6 are cleared.
- At RAMACT = [1], RAM access cannot be performed.
- When each register of address 14h is set to [1], the pulse with a cycle of 4 ms is output.
- The pulse from INT continues to be output until address 14h is read.
- Set RSTB pin to Low in order to stop the INT pulse output in the case that a serial read function is not used.
- The state at RAMACT = [1] is as follows.
  (1) While copying to RAM from ROM
  (2) While clearing RAM

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
15h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	R	R	R	R	R	R	R	R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
16h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
17h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
18h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
19h	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

• Don't access to the address 15h to 19h because these addresses are for test.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
1Ah	Data name	INTVSEL	—	—	—	—	—	—	—
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7 : INTVSEL Voltage setup of INT pin
[0] : 1.85 V (default)
[1] : 2.85 V

OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
20h	Data name	—	—	—	—	—	—	—	MTXON
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : MTXON ON/OFF setup of matrix LED control
[0] : OFF (default)
[1] : ON

- During MTXON = [1], the control contents to subsequent ROM, RAM, and registers are sequentially processed and lit up.
- Set MTXON to [1] at 5 ms after OSCEN (address 01h) is set to [1].
- To display the matrix part, set MTXON to [1], and then set the other addresses.

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
21h	Data name	MTXDATA[7 : 0]							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : MTXDATA[7 : 0] Address setup of ROM / RAM which read the data
[00000000] – [10010101] : ROM (Luminance only)
7 × 7 pattern 0 (default) to pattern No.149
[10010110] – [11010000] : ROM (Luminance + Cycle + Delay)
7 × 7 pattern No.150 to No.208
[11010001] – [11010010] : RAM (Luminance + Cycle + Delay)
7 × 7 pattern RAM No.1, 2

- The pattern No.0 of ROM is all [0] data of matrix LED.
- Access to 21h is disabled while copying to RAM from ROM (COPYSTART 24h = [1]).

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
22h	Data name	—	—	—	—	—	—	ROM77[1 : 0]	
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : ROM77[1 : 0] Lighting control of 7 × 7(LED number : A1 to G7) fixed pattern of RPM

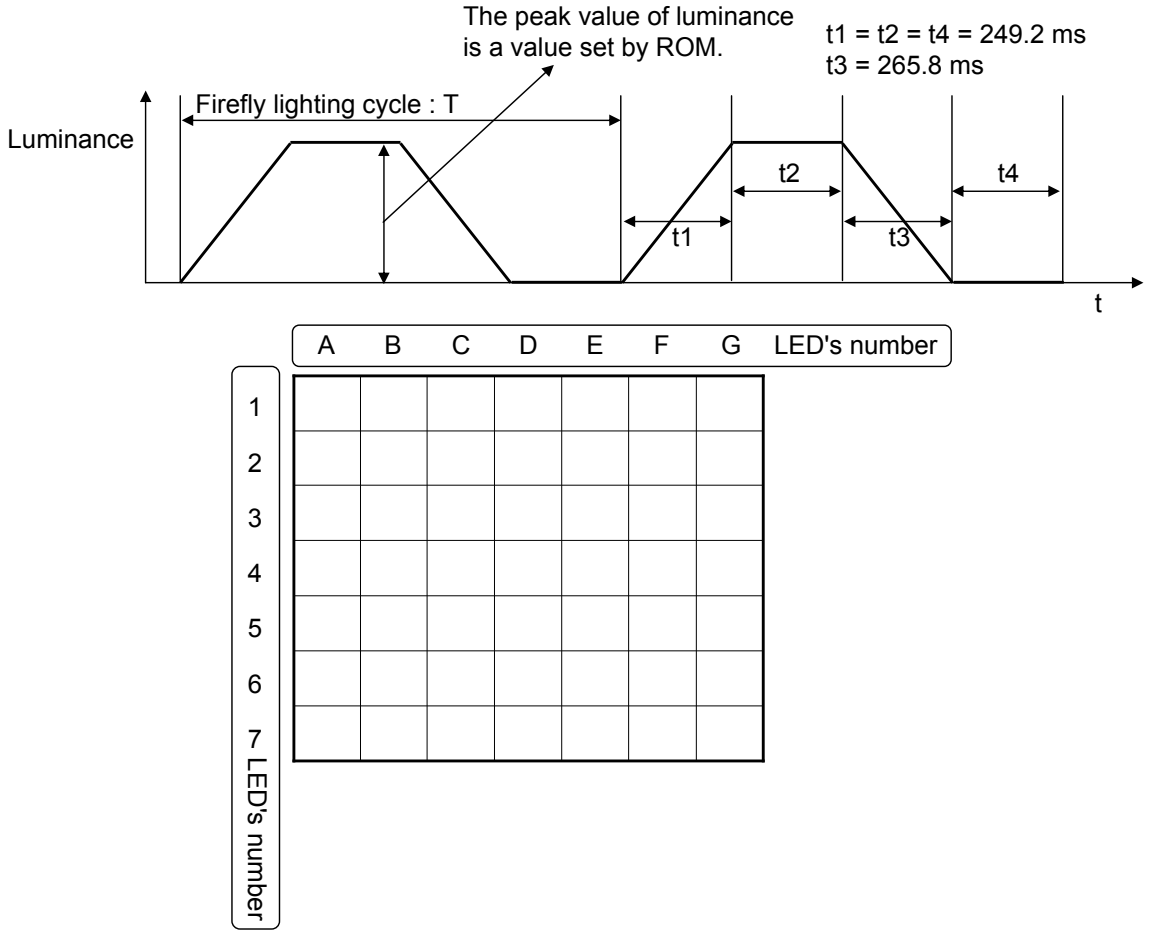
[00] : ROM data is displayed.

[01] : ROM data is displayed by firefly lighting in 1 s.

[10] : ROM data is displayed by firefly lighting in 2 s.

[11] : ROM data is displayed by firefly lighting in 3 s.

• During repetition display (REPON = [1]), ROM77 must not be changed.



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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
23h	Data name	SELROM[7 : 0]							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SELROM[7 : 0] Address setup of ROM copied to RAM
[00000000] – [10010101] : ROM (Luminance only) 7 × 7 pattern 0 (default) to pattern No.149
[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to No.208

- Access to 23h is disabled while copying to RAM from ROM (COPYSTART 24h = [1]).

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
24h	Data name	—	—	—	—	—	—	SELRAM	COPYSTART
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : SELRAM RAM number setup of copy destination
[0] : RAM No.1
[1] : RAM No.2

D0 : COPYSTART Copy start ON/OFF control of RAM from ROM
[0] : OFF
[1] : The copy set by SELROM and SELRAM is started. (It returns to [0] after internal 51clk)

- Address 24h is only for copying data to RAM. LED display never starts by address 24h.
  (However, LED display is updated when this RAM is copied during RAM display.)
- The write to address 21h-MTXDATA, 2Ah-SCLON, and 27h-REPON is disabled while copying.
  (RAMACT flag is raised.)
- Access to SELRAM is disabled while copying to RAM from ROM (COPYSTART 24h = [1]).
- Don't set RAM clear of address 29h while copying.
  (The waiting time for over 1 ms is required after COPYSTART.)

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
25h	Data name	SETFROM[7 : 0]							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SETFROM[7 : 0] ROM frame data address setup when repetition display starts
[00000000] – [10010101] : ROM (Luminance only) 7 × 7 pattern 0 (default) to pattern No.149
[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to No.208

- During repetition display (REPON = [1]), SETFROM setup must not be changed.

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
26h	Data name	SETTO[7 : 0]							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SETTO[7 : 0] ROM frame data address setup when repetition display ends.
[00000000] – [10010101] : ROM (Luminance only) 7 × 7 pattern 0 (default) to pattern No.149
[10010110] – [11010000] : ROM (Luminance + Cycle + Delay) 7 × 7 pattern No.150 to No.208

- During repetition display (REPON = [1]), SETTO setup must not be changed.

OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
27h	Data name	—	—	—	—	—	—	—	REPON
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : REPON Repetition display ON/OFF control
[0] : Repetition display OFF (default)
[1] : Repetition display ON

- During repetition display, display of setup ROM continues.
- Repetition display starts at MTXON = [1] and REPON = [1].
- Access to 27h is disabled while copying to RAM from ROM (COPYSTART 24h = [1]).
- When SCLON changes to [1] while REPON = [1], REPON changes to [0], and this LSI shifts to a scroll function.
- During repetition display (REPON = [1]), the setting of SETFROM and SETTO must not be changed.

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
28h	Data name	—	—	—	—	—	—	SETTIME[1 : 0]	
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : SETTIME[1 : 0] Frame display time setup of repetition display
[00] : 1 s (default)
[01] : 2 s
[10] : 3 s
[11] : 4 s

OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
29h	Data name	—	—	—	—	—	—	RAM1	RAM2
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : RAM1 The data in 7 × 7 RAM1 is cleared.
[0] : Overwrite is possible. (default)
[1] : The data in 7 × 7 RAM1 is cleared. (It returns to [0] by internal 2clk.)

D0 : RAM2 The data in 7 × 7 RAM2 is cleared.
[0] : Overwrite is possible. (default)
[1] : The data in 7 × 7 RAM2 is cleared. (It returns to [0] by internal 2clk.)

- Don't set the RAM-clear operation of RAM1 or RAM2 during scroll display (SCLON = [1]).
- Don't set the RAM-clear operation of address 29h during the copy operation of address 24h.
  (The waiting time for over 1 ms is required after COPYSTART.)

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
2Ah	Data name	—	—	—	—	—	—	—	SCLON
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : SCLON ON/OFF setup of scroll display
[0] : OFF (default)
[1] : ON

- Scroll display displays the data in RAM No.1 to 2 of 7 × 7 in order of A to G column. The display travel time of columns is a setup value of SCLTIME.
- During the scroll display, data can be written to RAM without specifying RAM number.
  (The write to empty RAM is performed.)
- The scroll display is started in the state of MTXON = [1] and SCLON.
- Access to 2Ah is disabled while copying to RAM from ROM (COPYSTART 24h = [1]).
- When REPON changes to [1] at SCLON = [1], SCLON changes to [0], and the scroll display shifts to repetition display function.
- During scroll display (SCLON = [1]), don't clear RAM (RAM1, RAM2).
- To restart the scroll display after the scroll display stops at SCLON= [0] or MTXON= [0], RSTB pin should be set to Low and be reset.

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
2Bh	Data name	—	—	—	—	—	—	SCLTIME[1 : 0]	
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : SCLTIME[1 : 0] Frame display time setup of scroll display
[00] : 0.1 s (default)
[01] : 0.2 s
[10] : 0.4 s
[11] : 0.8 s

- The display travel time of the column is the setup value of SCLTIME.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
2Ch	Data name	—	—	—	—	—	—	—	RGBON
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : RGBON ON/OFF setup of RGB lighting
[0] : OFF (default)
[1] : ON

• Set RGBON to [1] at 5 ms after address 01h OSCEN is set to [1].

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Data name	—	—	RGBDATA[5:0]					
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D5-0 : RGBDATA[5 : 0] Address setup of ROM and register which read RGB data
[000000] : Register display
[000001] – [101010] : ROM (RGB pattern, Luminance + Cycle + Delay) pattern No.1 to No.42

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
2Eh	Data name	Test mode							
	Default	0	0	0	0	0	0	0	0
	Mode	R	R	R	R	R	R	R	R

• Don't access to this address because it is for test.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
30h	Data name	—	—	—	—	—	—	—	RAMNUM
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : RAMNUM RAM number setup at CPU access (read, write)
[0] : RAM No.1
[1] : RAM No.2

• Access to 30h is disabled during scroll display (SCLON 2Ah = [1]).

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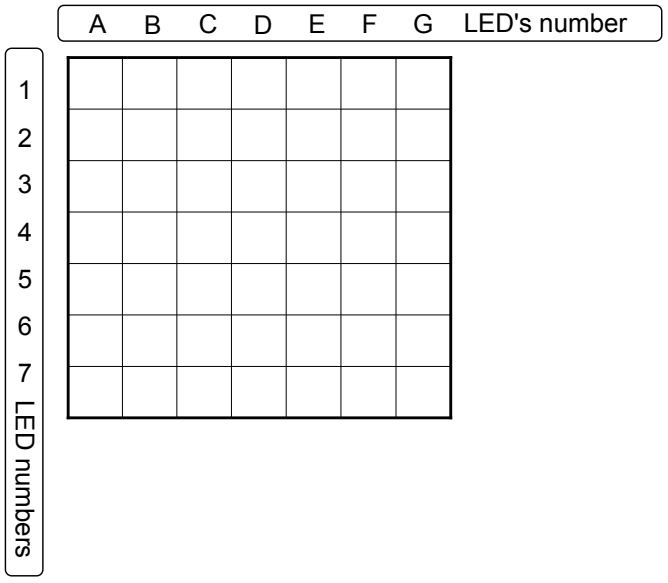
OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	Data name	BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLA1[3 : 0] Luminance setup of LED No. A1
[0000] : 0 mA (default)
[0001] : 1 mA
[0010] : 2 mA
[0011] : 3 mA
[0100] : 4 mA
[0101] : 5 mA
[0110] : 8 mA
[0111] : 11 mA
[1000] : 15 mA
[1001] : 17 mA
[1010] : 19 mA
[1011] : 21 mA
[1100] : 24 mA
[1101] : 26 mA
[1110] : 28 mA
[1111] : 30 mA



D3-2 : FRA1[1 : 0] Firefly operation and cycle setup of LED No.A1
[00] : Always lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLA1[1 : 0] Firefly operation delay setup of LED No.A1
[00] : No delay (default)
[01] : Delay 25%
[10] : Delay 50%
[11] : Delay 75%

- As for the addresses to 61h, the operation corresponding to each LED number is the same as above.
- The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 31h to 61h is written in. Please input other serial commands after that.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
62h	Data name	BLLEDR[3 : 0]				FRLEDR[1 : 0]		DLLEDR[1 : 0]	
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLLEDR[3 : 0] Luminance setup of LED which is connected to R pin
[0000] : 0 mA (default)
[0001] : 1 mA
[0010] : 2 mA
:
:
[1110] : 14 mA
[1111] : 15 mA

D3-2 : FRLEDR[1 : 0] Firefly operation and cycle setup of LED which is connected to R pin
[00] : Always lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLLEDR[1 : 0] Firefly operation delay setup of LED which is connected to R pin
[00] : No delay (default)
[01] : Delay 25%
[10] : Delay 50%
[11] : Delay 75%

- As for the addresses to 62h, the operation corresponding to G and B pin is the same as above.
- The waiting time for 2 or more internal clocks (2 µs or more) is required after the data from address 62h to 64h is written in. Please input other serial commands after that.

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OPERATION (continued)

4. Register and Address (continued)

Register map detail descriptions (continued)

Sub address		Data							
		D7	D6	D5	D4	D3	D2	D1	D0
6Bh	Data name	For test							
	Default	0	0	0	0	0	0	0	0
	Mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

- Address from 6Bh onwards are registers for test. Don't write into these addresses.

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OPERATION (continued)

5. Serial interface format

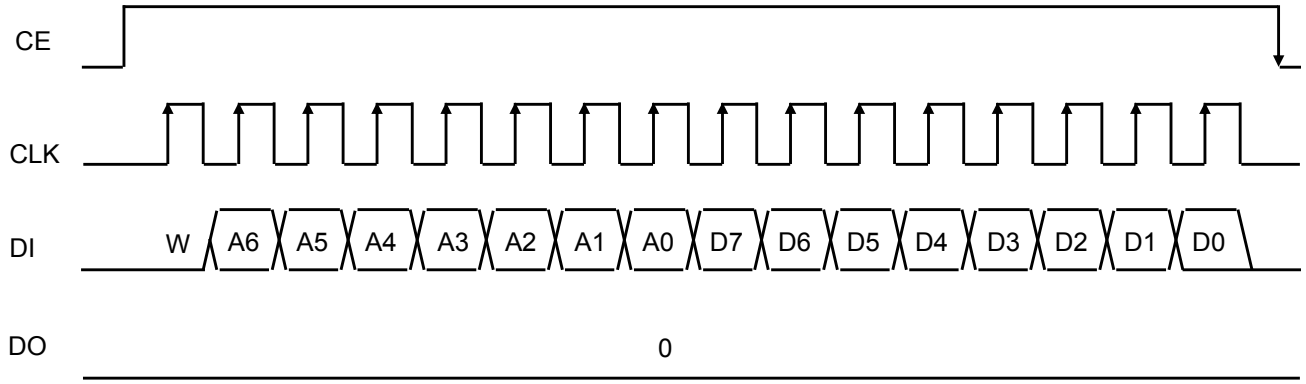
SPI format

- The interface with microcomputer consists of 16-bit serial register (8-bit of command, 8-bit of address), address decoder and transmitting register (8-bit).
- Serial interface consists of 4pins, which are serial clock pin (CLK), serial data input pin (DI), serial data output pin (DO) and chip enable input pin (CE).

(1) Write operation

- Data is taken into an internal shift register at the rising edge of CLK. (CTL frequency can be used within 13 MHz.)
- The reception of data becomes enable in High interval of CE. (active : High)
- Data is transmitted at MSB first in order of control register address (8-bit) and control command (8-bit).

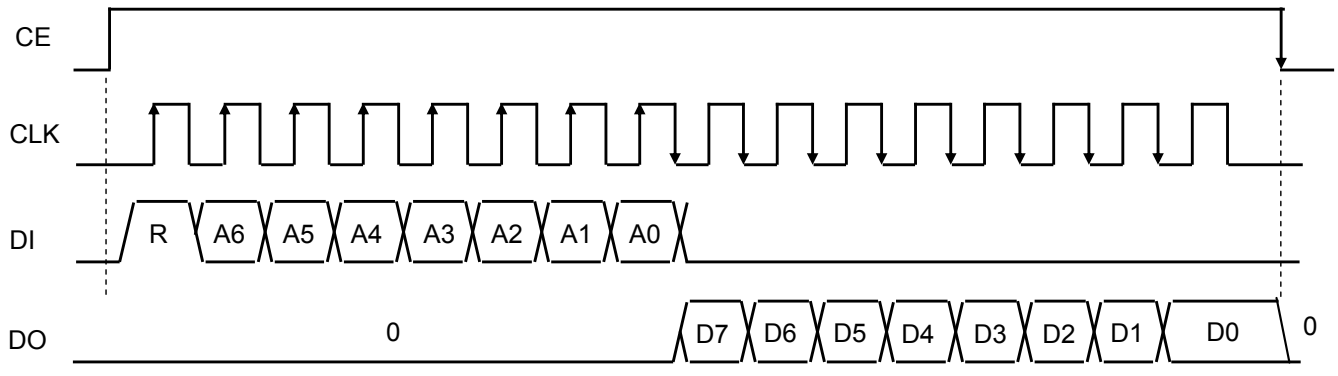
Write access timing



(2) Transmission operation

- Data is taken into an internal shift register at the rising edge of CLK. (CLK frequency can be used within 6 MHz.)
  * RAM cannot be read.
- The reception of data becomes enable in High interval of CE. (active : High)
- Data is transmitted at MSB first in order of register address (8-bit) and control command (max 8-bit).

Read access timing



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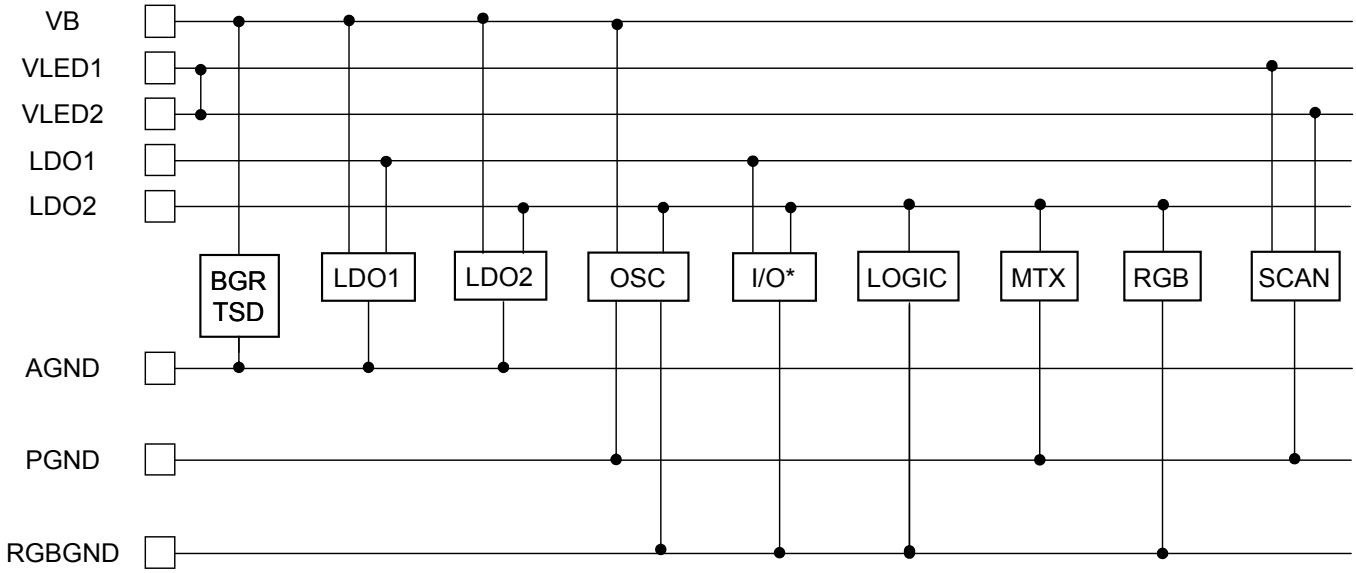
OPERATION (continued)

6. Signal distribution diagram

Power supply distribution diagram



Note) * : CLK, CE, DI, DO, LEDCTL

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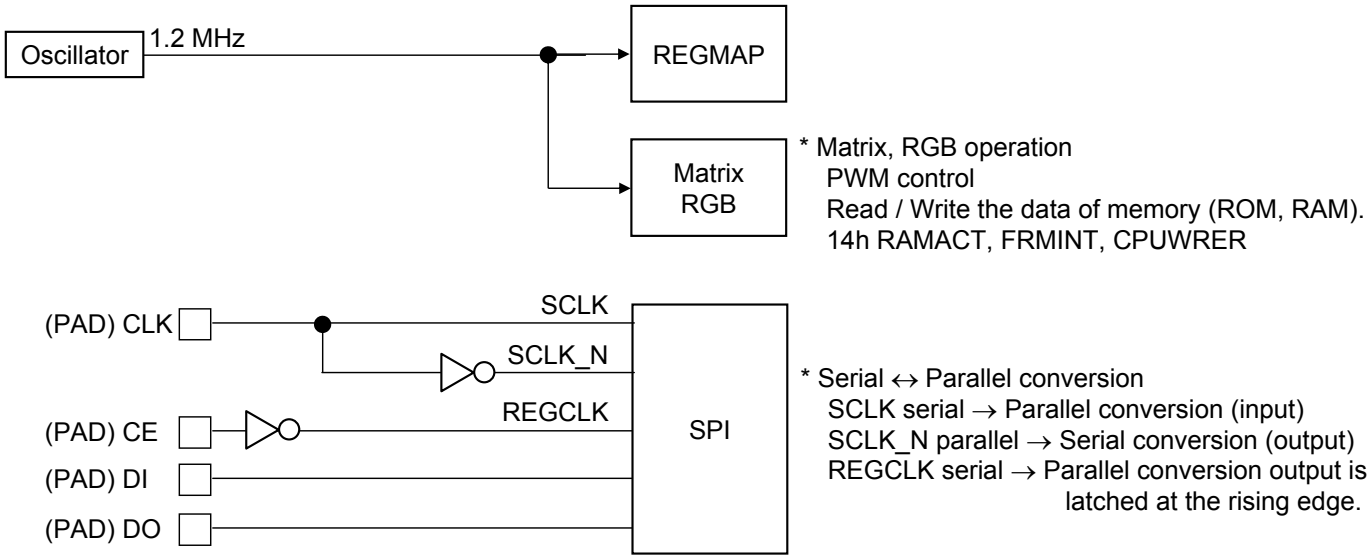
OPERATION (continued)

6. Signal distribution diagram (continued)

Control / Clock distribution diagram



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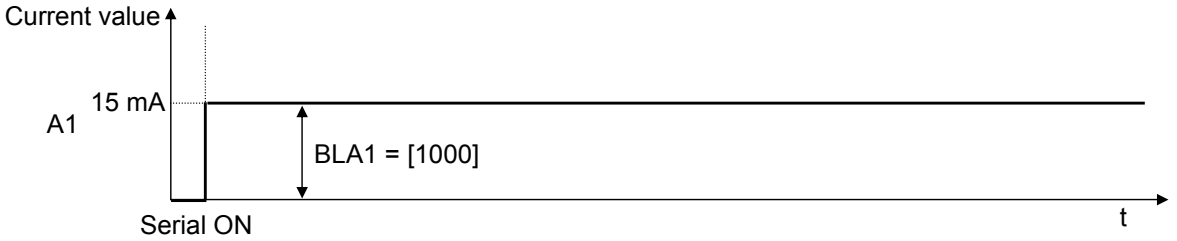
OPERATION (continued)

7. Firefly lighting example

Firefly lighting example 1

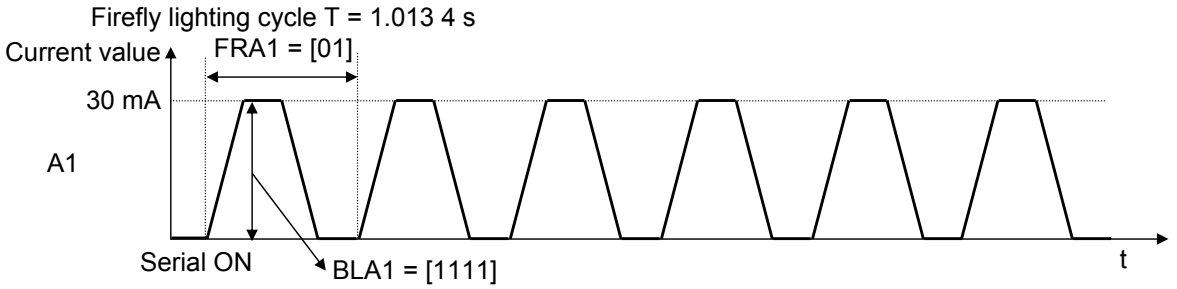
Initial setup example for always lighting

BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
1	0	0	0	0	0	0	0



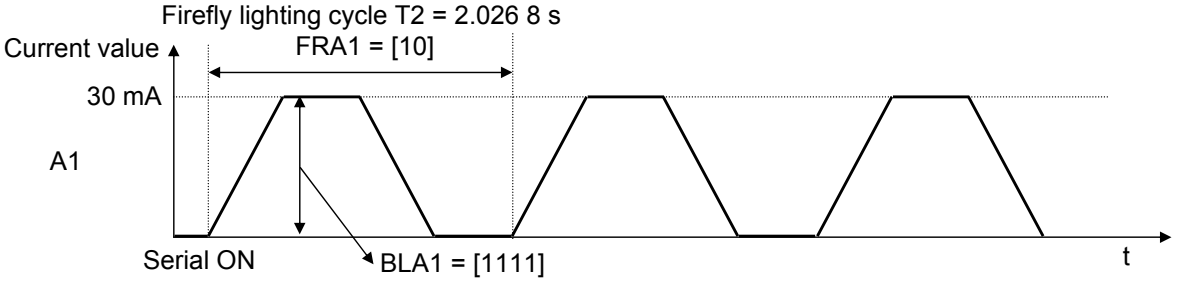
Firefly lighting setup 1 s

BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
1	1	1	1	0	1	0	0



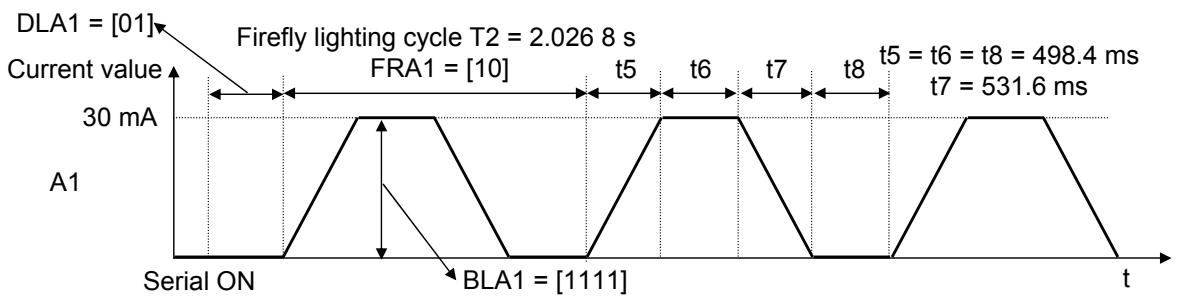
Cycle change 1 s → 2 s

BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
1	1	1	1	1	0	0	0



Delay change Nothing → 25%

BLA1[3 : 0]				FRA1[1 : 0]		DLA1[1 : 0]	
1	1	1	1	1	0	0	1



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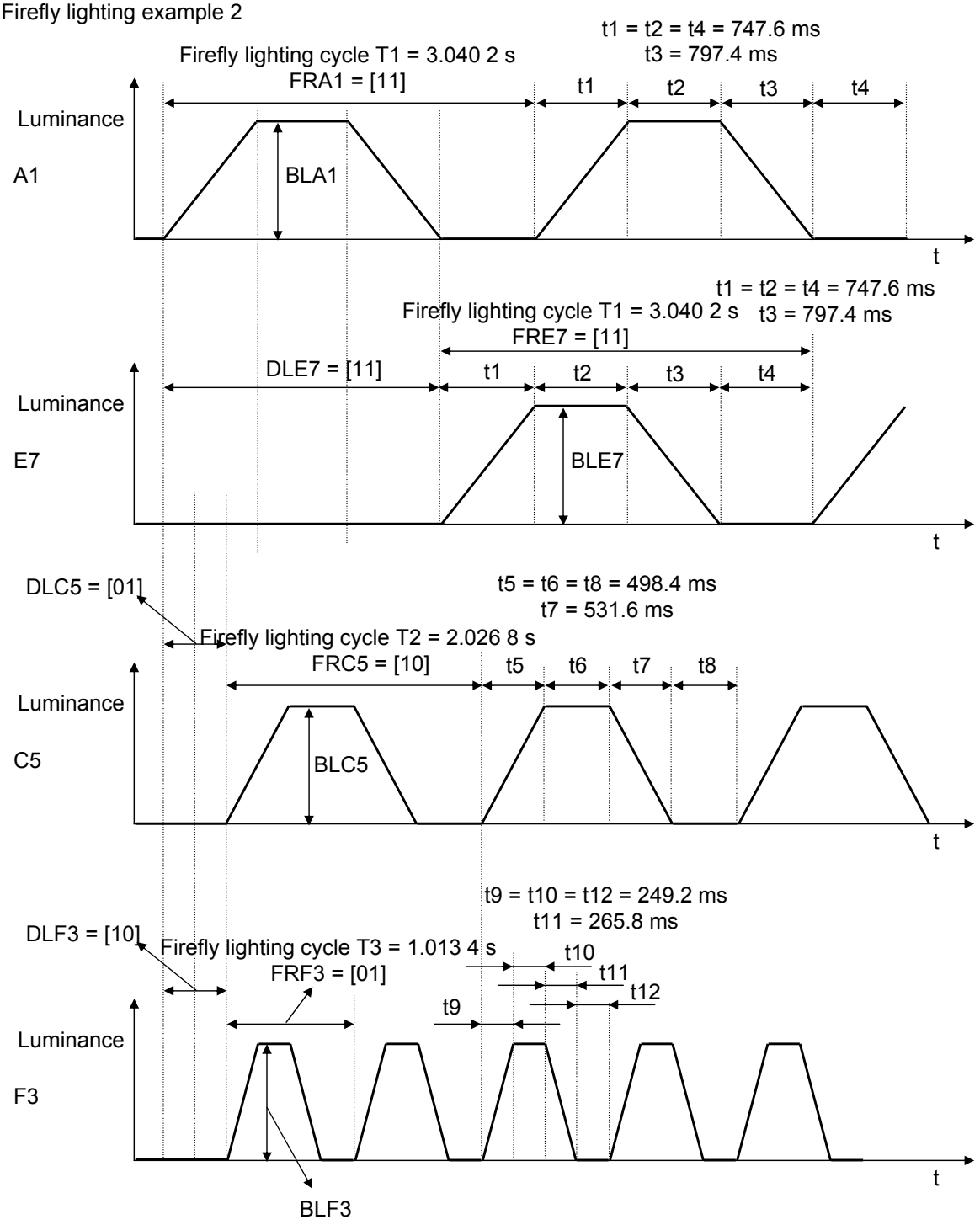
OPERATION (continued)

7. Firefly lighting example (continued)

Firefly lighting example 2

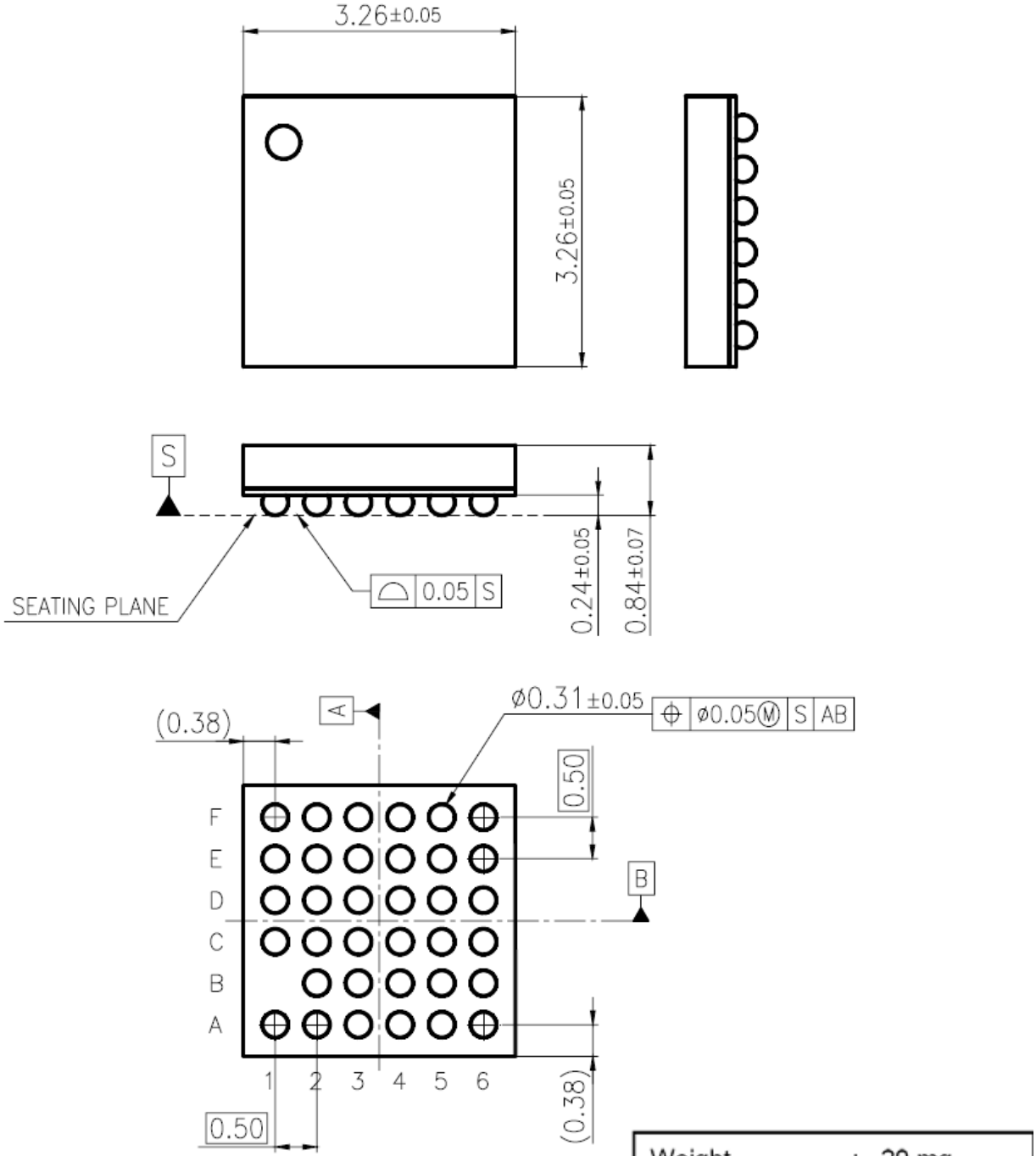


1. Normally, it is not possible to control data when RGBGND pin voltage is undefined. Therefore, please keep the RGBGND pin voltage at the lowest voltage.
2. Please check the input waveform to the CLK pin. When inputting clock into the CLK pin, if the input clock is ringing with input voltage between 0.4 V to LDO1 × 0.8 V (input voltage indefinite range), it will result in serial data not able to be written to or be read out from a register. (It is recommended to smooth the rising and falling edge of the input clock by connecting input capacitance (a capacitor, etc.) to the CLK pin.)

PACKAGE INFORMATION (Reference Data)

UBGA035-W-3333AEA

Unit:mm



Weight	:	20 mg
Body Material	:	Epoxy Resin
Reroute Material	:	Cu
Terminal Material	:	SnAgCu

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IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
4. This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the LSI being used in automotive application, unless our company agrees to such application in this book.
5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.
13. Due to the unshielded structure of this LSI, functions and characteristics of the product cannot be guaranteed under the exposure of light. During normal operation or even under testing condition, please ensure that the LSI is not exposed to light.
14. Please ensure that your design does not have metal shield parts touching the chip surface as the surface potential is GND voltage.

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Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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